What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx154f128b-v-so

TABLE 5: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN SOIC (TOP VIEW)[1,2,3]

1   28

SOIC

PIC32MX255F128B
PIC32MX275F256B

Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	VBUS
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1	19	VSS
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	VCAP
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3	21	D+
8	VSS	22	D-
9	OSC1/CLKI/RPA2/RA2	23	VUSB3V3
10	OSC2/CLKO/RPA3/PMA0/RA3	24	VBAT
11	SOSCI/RPB4/CTED11/RB4[4]	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	TMS/RPB5/USBID/PMRD/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This is an input-only pin.

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The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr[1]	Reports the address for the most recent address-related exception.
9	Count[1]	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
11	Compare[1]	Timer interrupt control.
12	Status[1]	Processor status and control.
12	IntCtl[1]	Interrupt system status and control.
12	SRSCtl[1]	Shadow register set status and control.
12	SRSMap[1]	Provides mapping from vectored interrupt to a shadow set.
13	Cause[1]	Cause of last general exception.
14	EPC[1]	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration Register 1.
16	Config2	Configuration Register 2.
16	Config3	Configuration Register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
23	Debug[2]	Debug control and exception status.
24	DEPC[2]	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
30	ErrorEPC[1]	Program counter at last error.
31	DESAVE[2]	Debug handler scratchpad register.

Note 1: Registers used in exception processing.
　　　2: Registers used during debug.

REGISTER 4-2: **BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

REGISTER 6-1:   RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	RW-0, HC	R/W-0, HC	U-0	U-0
	—	—	—	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
	—	—	—	—	—	—	VBPOR(2)	VBAT(2)
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
	—	—	—	—	—	DPSLP(1)	CMR	—
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR(1)	POR(1)

Legend:		HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit   **Unimplemented:** Read as '0'

bit 27   **BCFGERR:** Primary Configuration Registers Error Flag bit
           1 = An error occurred during a read of the primary configuration registers
           0 = No error occurred during a read of the primary configuration registers

bit 26   **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit
           1 = An error occurred during a read of the primary and alternate configuration registers
           0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-18 **Unimplemented:** Read as '0'

bit 17   **VBPOR:** VBPOR Mode Flag bit[2]
           1 = A VBAT domain POR has occurred
           0 = A VBAT domain POR has not occurred

bit 16   **VBAT:** VBAT Mode Flag bit[2]
           1 = A POR exit from VBAT has occurred (a true POR must be established with the valid VBAT voltage on the VBAT pin)
           0 = A POR exit from VBAT has not occurred

bit 15-11 **Unimplemented:** Read as '0'

bit 10   **DPSLP:** Deep Sleep Mode Flag bit[1]
           1 = Deep Sleep mode has occurred
           0 = Deep Sleep mode has not occurred

bit 9   **CMR:** Configuration Mismatch Reset Flag bit
           1 = A Configuration Mismatch Reset has occurred
           0 = A Configuration Mismatch Reset has not occurred

bit 8   **Unimplemented:** Read as '0'

bit 7   **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
           1 = Master Clear (pin) Reset has occurred
           0 = Master Clear (pin) Reset has not occurred

bit 6   **SWR:** Software Reset Flag bit
           1 = Software Reset was executed
           0 = Software Reset was not executed

bit 5   **Unimplemented:** Read as '0'

Note 1:   User software must clear this bit to view the next detection.
    2:   This bit is only available on devices with VBAT.

TABLE 12-2:   OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA0	RPA0R	RPA0R<3:0>	0000 = No Connect
RPB3	RPB3R	RPB3R<3:0>	0001 = U1TX
RPB15	RPB15R	RPB15R<3:0>	0010 = U2RTS
			0011 = SS1
			0100 = VBUSON[4]
RPB7	RPB7R	RPB7R<3:0>	0101 = OC1
RPC7[1]	RPC7R	RPC7R<3:0>	0110 = Reserved
RPC0[1]	RPC0R	RPC0R<3:0>	0111 = C2OUT
			1000 = Reserved
RPC5[1]	RPC5R	RPC5R<3:0>	•
			•
			1111 = Reserved
RPA1	RPA1R	RPA1R<3:0>	0000 = No Connect
RPB5	RPB5R	RPB5R<3:0>	0001 = Reserved
RPB1	RPB1R	RPB1R<3:0>	0010 = Reserved
			0011 = SDO1
RPB11[2]	RPB11R	RPB11R<3:0>	0100 = SDO2
RPB8	RPB8R	RPB8R<3:0>	0101 = OC2
RPA8[1]	RPA8R	RPA8R<3:0>	0110 = Reserved
RPC8[1]	RPC8R	RPC8R<3:0>	0111 = C3OUT
			•
RPA9[1]	RPA9R	RPA9R<3:0>	•
			1111 = Reserved
RPA2	RPA2R	RPA2R<3:0>	0000 = No Connect
RPB6[2]	RPB6R	RPB6R<3:0>	0001 = Reserved
			0010 = Reserved
RPB13[3]	RPB13R	RPB13R<3:0>	0011 = SDO1
			0100 = SDO2
RPB2	RPB2R	RPB2R<3:0>	0101 = OC4
RPC6[1]	RPC6R	RPC6R<3:0>	0110 = OC5
RPC1[1]	RPC1R	RPC1R<3:0>	0111 = REFCLKO
			1000 = Reserved
RPC3[1]	RPC3R	RPC3R<3:0>	•
			•
			1111 = Reserved
RPA3	RPA3R	RPA3R<3:0>	0000 = No Connect
RPB14	RPB14R	RPB14R<3:0>	0001 = U1RTS
			0010 = U2TX
RPB0	RPB0R	RPB0R<3:0>	0011 = Reserved
			0100 = SS2
RPB10[2]	RPB10R	RPB10R<3:0>	0101 = OC3
RPB9	RPB9R	RPB9R<3:0>	0110 = Reserved
			0111 = C1OUT
RPC9[1]	RPC9R	RPC9R<3:0>	1000 = Reserved
RPC2[1]	RPC2R	RPC2R<3:0>	•
			•
RPC4[1]	RPC4R	RPC4R<3:0>	1111 = Reserved

Note 1:   This pin is only available on 44-pin devices.

2:   This pin is not available on USB devices.

3:   This pin is not available on VBAT devices.

4:   This pin is only available on USB devices.

REGISTER 12-3: **CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit

1 = CN is enabled
0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Idle mode halts CN operation
0 = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON[1]	—	—	RUNDIV<4:0>				
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	WDTWINEN

Legend:		
	y = Values set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to these bits using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit[1]

1 = The Watchdog Timer module is enabled
0 = The Watchdog Timer module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Watchdog Timer Postscaler Value in Run Mode bits

In Run mode, these bits are set to the values of the WDTPS<4:0> Configuration bits in DEVCFG1.

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when FWDTEN (DEVCFG1<23>) = 0.

17.0   INPUT CAPTURE

> **Note:**   This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
  - Capture timer value on every rising and falling edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 17-1 illustrates a general block diagram of the Input Capture module.

FIGURE 17-1:   INPUT CAPTURE BLOCK DIAGRAM
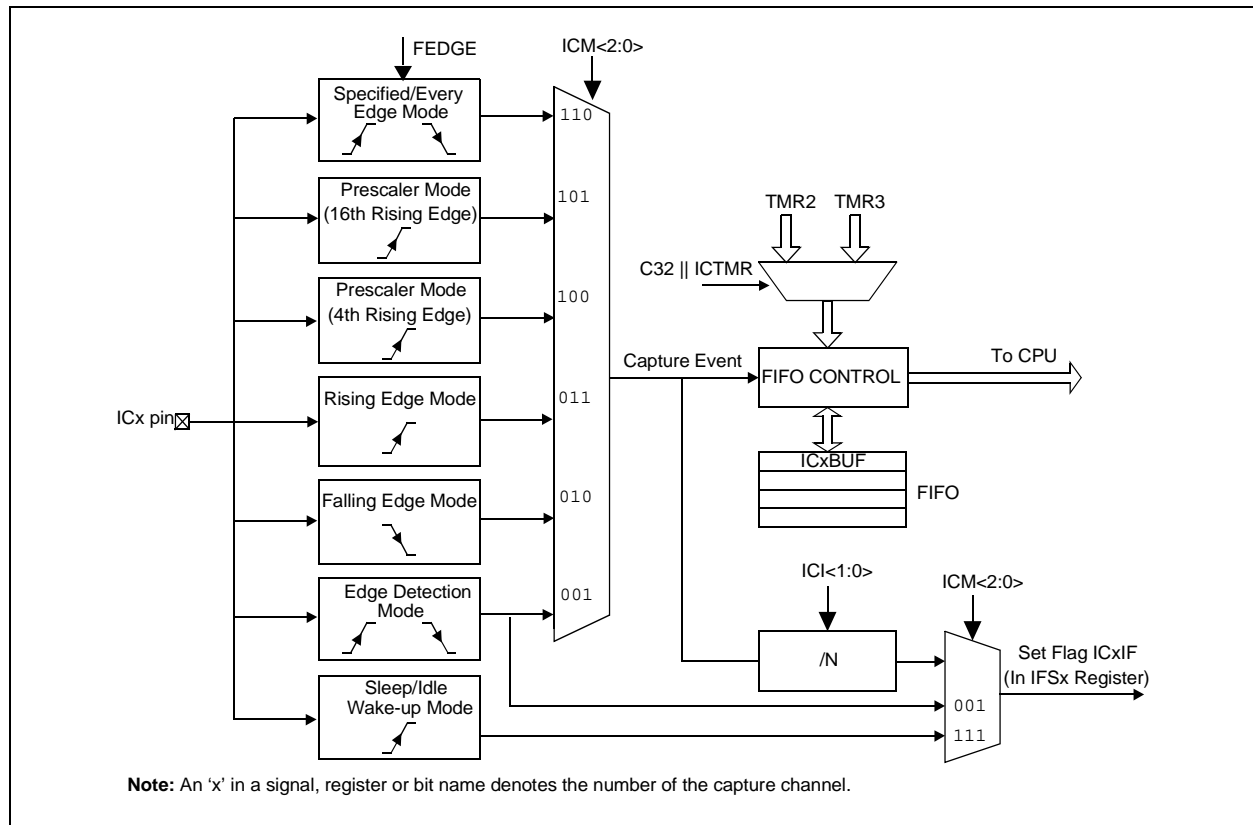
Note: An 'x' in a signal, register or bit name denotes the number of the capture channel.

NOTES:

Figure 21-2 and Figure 21-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 21-2: UART RECEPTION

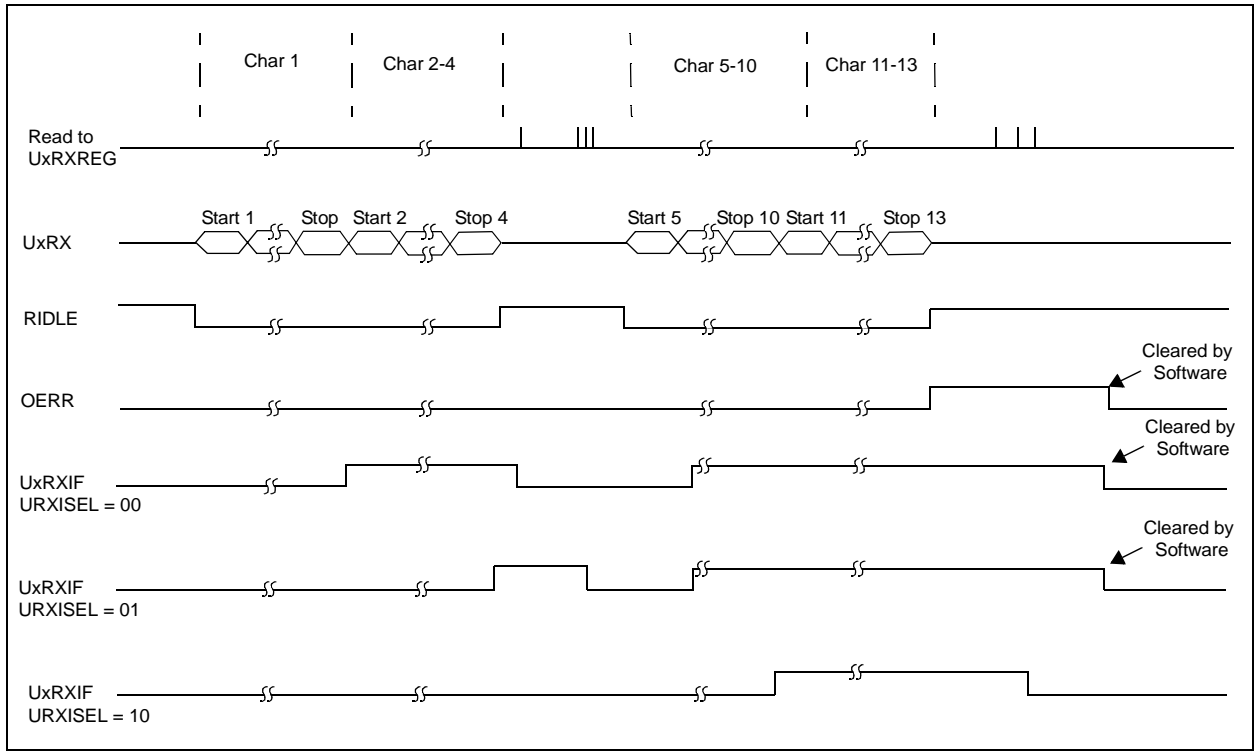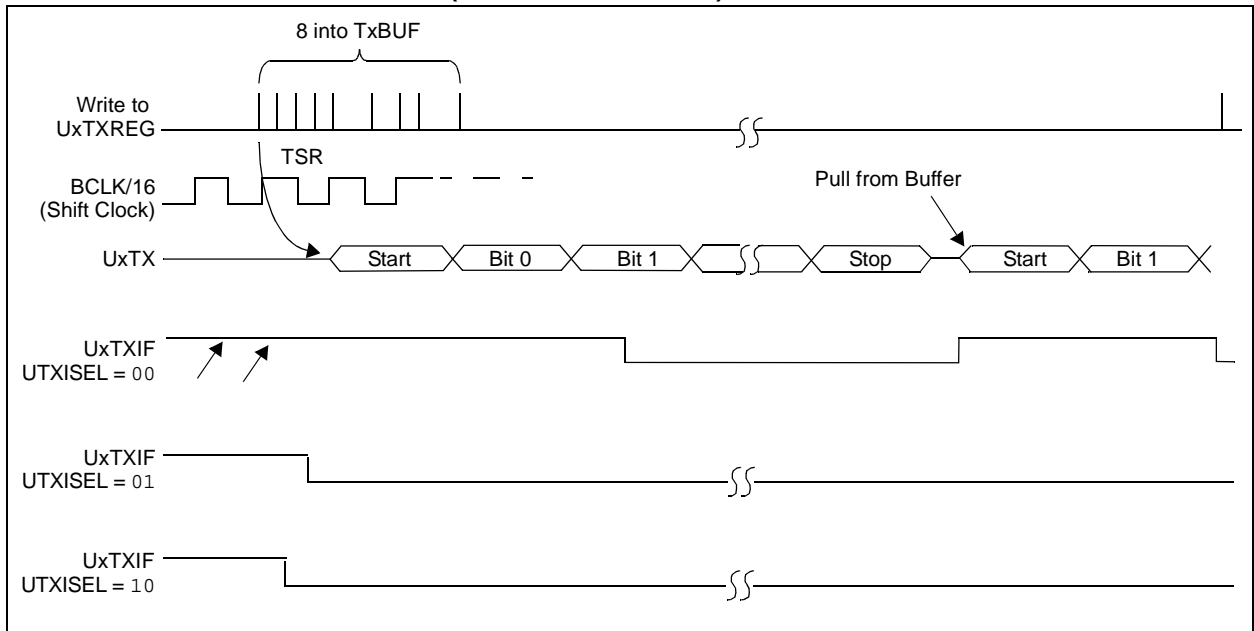**FIGURE 21-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**

REGISTER 22-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 7-6   **CSF<1:0>:** Chip Select Function bits[2]

     11 = Reserved
     10 = PMCS1 functions as Chip Select
     01 = PMCS1 functions as PMA<14>
     00 = PMCS1 functions as PMA<14>

bit 5   **ALP:** Address Latch Polarity bit[2]

     1 = Active-high (PMALL and PMALH)
     0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4   **Unimplemented:** Read as '0'

bit 3   **CS1P:** Chip Select 0 Polarity bit[2]

     1 = Active-high (PMCS1)
     0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2   **Unimplemented:** Read as '0'

bit 1   **WRSP:** Write Strobe Polarity bit

     For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
     1 = Write strobe active-high (PMWR)
     0 = Write strobe active-low ($\overline{\text{PMWR}}$)

     For Master mode 1 (MODE<1:0> = 11):
     1 = Enable strobe active-high (PMENB)
     0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0   **RDSP:** Read Strobe Polarity bit

     For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
     1 = Read Strobe active-high (PMRD)
     0 = Read Strobe active-low ($\overline{\text{PMRD}}$)

     For Master mode 1 (MODE<1:0> = 11):
     1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
     0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

     2: These bits have no effect when their corresponding pins are used as address lines.

NOTES:

TABLE 33-18: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	50	MHz	EC **(Note 3)**
OS13		Oscillator Crystal Frequency	10	—	25	MHz	HS **(Note 3)**
OS15			32	32.768	100	kHz	SOSC **(Note 3)**
OS20	TOSC	TOSC = 1/FOSC = TCY **(Note 2)**	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	—	ns	EC **(Note 3)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 3)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 3)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 3)**
OS42	GM	External Oscillator Transconductance (Primary Oscillator only)	14	16	18	mA/V	VDD = 3.3V, TA = +25°C **(Note 3)**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: This parameter is characterized, but not tested in manufacturing.

TABLE 33-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics[1]	Min.	Typical	Max.	Units	Conditions	
OS50	F_{IN}	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	4	—	5	MHz	ECPLL, HSPLL, and FRCPLL modes	
OS51	F_{SYS}	On-Chip VCO System Frequency	60	—	120	MHz	—	
OS52	T_{LOCK}	PLL Start-up Time (Lock Time)	—	—	2	ms	—	
OS53	D_{CLK}	CLKO Stability[2] (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

TABLE 33-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz[1]						
F20b	FRC	-0.9	—	+0.9	%	—

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 33-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
LPRC @ 31.25 kHz[1]						
F21	LPRC	-15	—	+15	%	—

Note 1: Change of LPRC frequency as VDD changes.

Advance Information

FIGURE 33-8: **OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**

OCx
(Output Compare
or PWM mode)

OC11   OC10

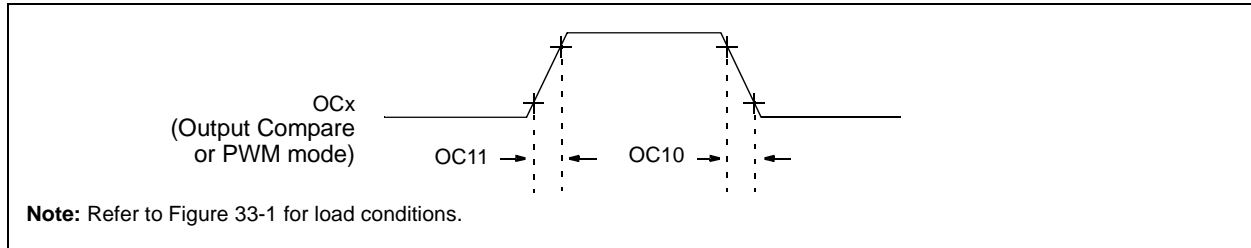**Note:** Refer to Figure 33-1 for load conditions.

TABLE 33-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

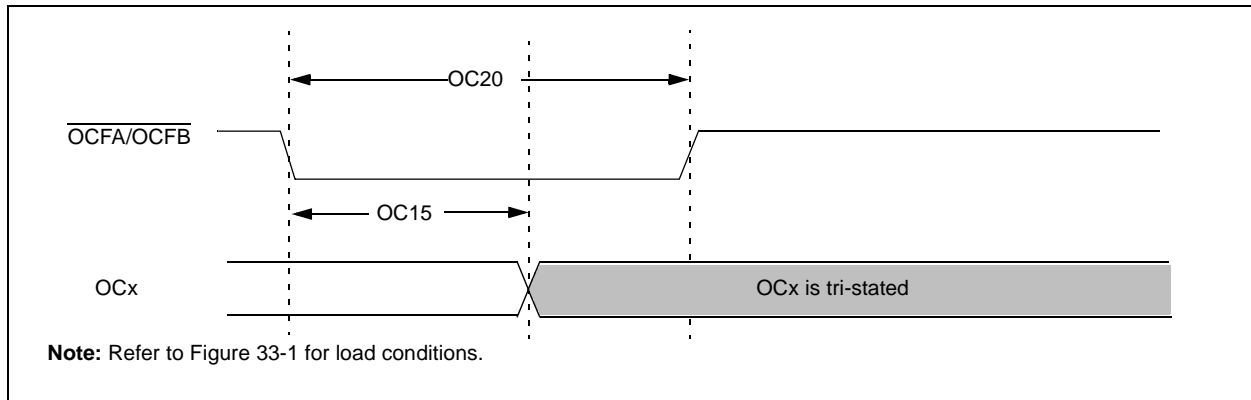**FIGURE 33-9:** **OCx/PWM MODULE TIMING CHARACTERISTICS**

OCFA/OCFB

OC20

OC15

OCx

OCx is tri-stated

Note: Refer to Figure 33-1 for load conditions.

TABLE 33-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	Symbol	Characteristics[1]	Min	Typical[2]	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 33-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	T$_{LO:SCL}$	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—
IS11	T$_{HI:SCL}$	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—
IS20	T$_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	C$_B$ is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C$_B$	300	ns	
			1 MHz mode **(Note 1)**	—	100	ns	
IS21	T$_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	C$_B$ is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C$_B$	300	ns	
			1 MHz mode **(Note 1)**	—	300	ns	
IS25	T$_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 1)**	100	—	ns	
IS26	T$_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode **(Note 1)**	0	0.3	μs	
IS30	T$_{SU:STA}$	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS31	T$_{HD:STA}$	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS33	T$_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	600	—	ns	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 33-35: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
ADC Accuracy – Measurements with Internal VREF+/VREF-							
AD20d	Nr	Resolution	10 data bits			bits	(Note 3)
AD21d	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)
AD22d	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Notes 2,3)
AD23d	GERR	Gain Error	> -4	—	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)
AD24d	EOFF	Offset Error	> -2	—	< 2	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)
AD25d	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD32b	SINAD	Signal to Noise and Distortion	55	58.5	—	dB	(Notes 3,4)
AD34b	ENOB	Effective Number of bits	9.0	9.5	—	bits	(Notes 3,4)

Note 1: These parameters are not characterized or tested in manufacturing.
    2: With no missing codes.
    3: These parameters are characterized, but not tested in manufacturing.
    4: Characterized with a 1 kHz sine wave.
    5: The ADC module is functional at VBORMIN < VDD < 2.0V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

34.0   DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

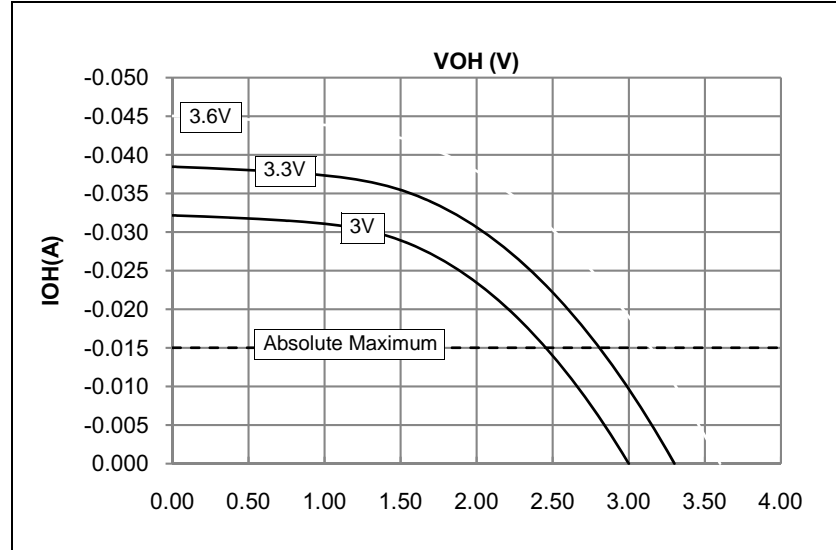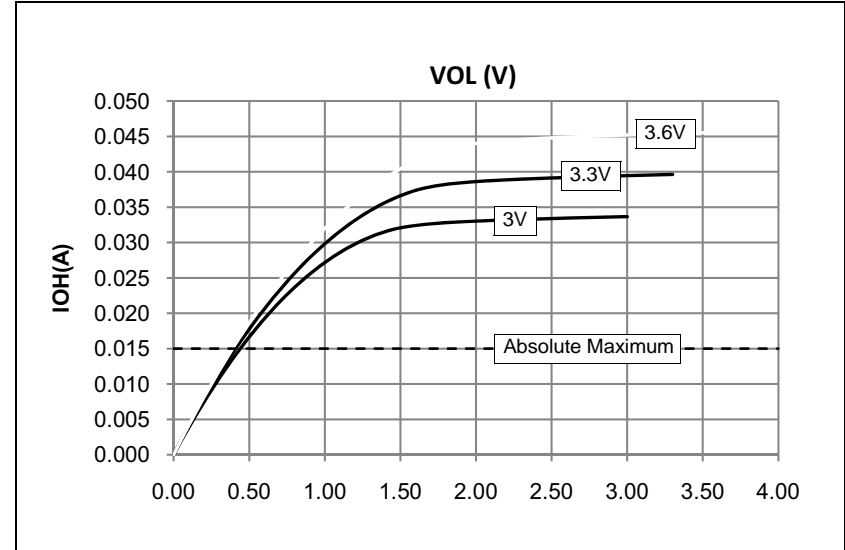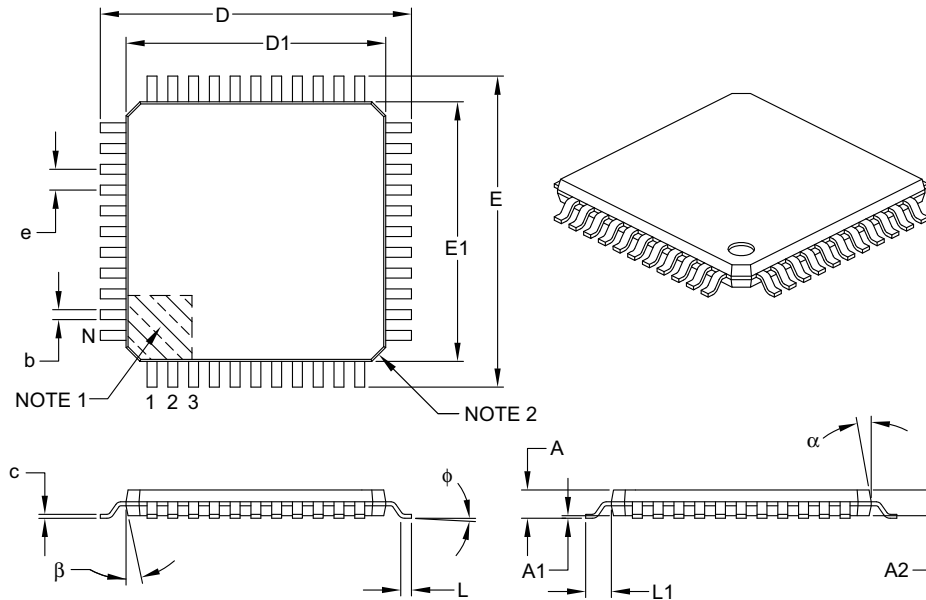**FIGURE 34-1:**   **I/O OUTPUT VOLTAGE HIGH (V$_{OH}$)**

FIGURE 34-2:   **I/O OUTPUT VOLTAGE LOW (V$_{OL}$)**

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units		MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B