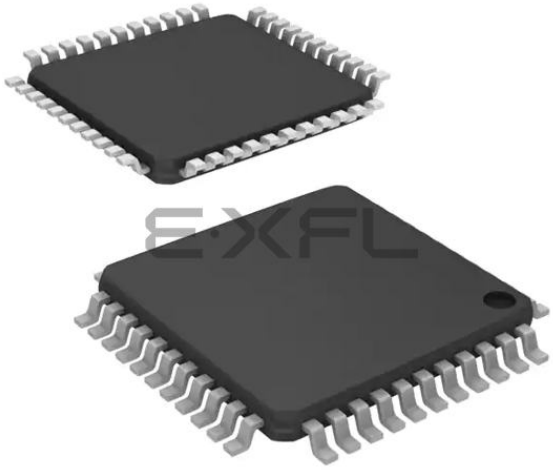

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 3.6V |
| Data Converters | A/D 13x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx154f128d-i-ml |

**TABLE 5: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT**

**28-PIN SOIC (TOP VIEW)(1,2,3)**

1 28

**SOIC**

**PIC32MX255F128B**
**PIC32MX275F256B**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | $\overline{\text{MCLR}}$ | 15 | VBUS |
| 2 | PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0 | 16 | TDI/RPB7/CTED3/PMD5/INT0/RB7 |
| 3 | PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1 | 17 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 |
| 4 | PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 | 18 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 5 | PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1 | 19 | VSS |
| 6 | PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 20 | VCAP |
| 7 | PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3 | 21 | D+ |
| 8 | VSS | 22 | D- |
| 9 | OSC1/CLKI/RPA2/RA2 | 23 | VUSB3V3 |
| 10 | OSC2/CLKO/RPA3/PMA0/RA3 | 24 | VBAT |
| 11 | SOSCI/RPB4/CTED11/RB4(4) | 25 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14 |
| 12 | SOSCO/RPA4/T1CK/CTED9/RA4 | 26 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 13 | VDD | 27 | AVSS |
| 14 | TMS/RPB5/USBID/PMRD/RB5 | 28 | AVDD |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**4:** This is an input-only pin.

**TABLE 1-13: USB PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number(1,2) | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SOIC | 44-pin QFN/ TQFP | | | |
| **Universal Serial Bus** | | | | | | |
| VBUS | 12 | 15 | 42 | I | Analog | USB Bus Power Monitor |
| VUSB3V3 | 20 | 23 | 10 | P | — | USB Internal Transceiver Supply. This pin must be connected to VDD. |
| VBUSON | PPS | PPS | PPS | O | — | USB Host and OTG Bus Power Control Output |
| D+ | 18 | 21 | 8 | I/O | Analog | USB D+ |
| D- | 19 | 22 | 9 | I/O | Analog | USB D- |
| USBID | 11 | 14 | 41 | I | ST | USB OTG ID Detect |
| USBON | 14 | 17 | 44 | O | — | ON Signal for External VBUS Source |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** All pins are only available on USB devices.

**3:** Pin number for devices without VBAT.

**4:** Pin number for devices with USB only.

**5:** Pin number for devices without USB.

## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

## 2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

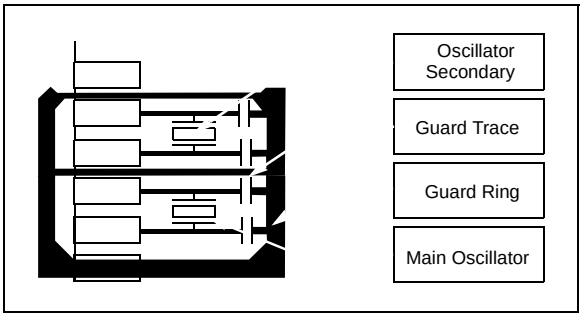
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

## 2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

**FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT**




## 2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

**TABLE 4-1: SFR MEMORY MAP**

| Peripheral | Virtual Address | |
|---|---|---|
| | Base | Offset Start |
| Deep Sleep Controller | 0xBF80 | 0x0000 |
| RTCC | | 0x0200 |
| Timer1-Timer5 | | 0x0600 |
| Input Capture 1-5 | | 0x2000 |
| Output Compare 1-5 | | 0x3000 |
| I2C1 and I2C2 | | 0x5000 |
| SPI1 and SPI2 | | 0x5800 |
| UART1 and UART2 | | 0x6000 |
| PMP | | 0x7000 |
| ADC | | 0x9000 |
| CVREF | | 0x9800 |
| Comparator | | 0xA000 |
| CTMU | | 0xA200 |
| Oscillator, Reset | | 0xF000 |
| Device and Revision ID | | 0xF220 |
| Peripheral Module Disable | | 0xF240 |
| Flash Controller | | 0xF400 |
| Watchdog Timer | | 0xF600 |
| PPS | | 0xFA00 |
| HLVD | | 0xFC00 |
| Interrupts | 0xBF88 | 0x1000 |
| Bus Matrix | | 0x2000 |
| DMA | | 0x3000 |
| Prefetch | | 0x4000 |
| USB | | 0x5000 |
| PORTA-PORTC | | 0x6000 |
| Configuration | 0xBFC0 | 0x2FF0 |

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | IRQ # | Vector # | Interrupt Bit Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-priority | |
| U1E – UART1 Fault | 39 | 32 | IFS1<7> | IEC1<7> | IPC8<4:2> | IPC8<1:0> | Yes |
| U1RX – UART1 Receive Done | 40 | 32 | IFS1<8> | IEC1<8> | IPC8<4:2> | IPC8<1:0> | Yes |
| U1TX – UART1 Transfer Done | 41 | 32 | IFS1<9> | IEC1<9> | IPC8<4:2> | IPC8<1:0> | Yes |
| I2C1B – I2C1 Bus Collision Event | 42 | 33 | IFS1<10> | IEC1<10> | IPC8<12:10> | IPC8<9:8> | Yes |
| I2C1S – I2C1 Slave Event | 43 | 33 | IFS1<11> | IEC1<11> | IPC8<12:10> | IPC8<9:8> | Yes |
| I2C1M – I2C1 Master Event | 44 | 33 | IFS1<12> | IEC1<12> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNA – PORTA Input Change Interrupt | 45 | 34 | IFS1<13> | IEC1<13> | IPC8<20:18> | IPC8<17:16> | Yes |
| CNB – PORTB Input Change Interrupt | 46 | 34 | IFS1<14> | IEC1<14> | IPC8<20:18> | IPC8<17:16> | Yes |
| CNC – PORTC Input Change Interrupt | 47 | 34 | IFS1<15> | IEC1<15> | IPC8<20:18> | IPC8<17:16> | Yes |
| PMP – Parallel Master Port | 48 | 35 | IFS1<16> | IEC1<16> | IPC8<28:26> | IPC8<25:24> | Yes |
| PMPE – Parallel Master Port Error | 49 | 35 | IFS1<17> | IEC1<17> | IPC8<28:26> | IPC8<25:24> | Yes |
| SPI2E – SPI2 Fault | 50 | 36 | IFS1<18> | IEC1<18> | IPC9<4:2> | IPC9<1:0> | Yes |
| SPI2RX – SPI2 Receive Done | 51 | 36 | IFS1<19> | IEC1<19> | IPC9<4:2> | IPC9<1:0> | Yes |
| SPI2TX – SPI2 Transfer Done | 52 | 36 | IFS1<20> | IEC1<20> | IPC9<4:2> | IPC9<1:0> | Yes |
| U2E – UART2 Error | 53 | 37 | IFS1<21> | IEC1<21> | IPC9<12:10> | IPC9<9:8> | Yes |
| U2RX – UART2 Receiver | 54 | 37 | IFS1<22> | IEC1<22> | IPC9<12:10> | IPC9<9:8> | Yes |
| U2TX – UART2 Transmitter | 55 | 37 | IFS1<23> | IEC1<23> | IPC9<12:10> | IPC9<9:8> | Yes |
| I2C2B – I2C2 Bus Collision Event | 56 | 38 | IFS1<24> | IEC1<24> | IPC9<20:18> | IPC9<17:16> | Yes |
| I2C2S – I2C2 Slave Event | 57 | 38 | IFS1<25> | IEC1<25> | IPC9<20:18> | IPC9<17:16> | Yes |
| I2C2M – I2C2 Master Event | 58 | 38 | IFS1<26> | IEC1<26> | IPC9<20:18> | IPC9<17:16> | Yes |
| CTMU – CTMU Event | 59 | 39 | IFS1<27> | IEC1<27> | IPC9<28:26> | IPC9<25:24> | Yes |
| DMA0 – DMA Channel 0 | 60 | 40 | IFS1<28> | IEC1<28> | IPC10<4:2> | IPC10<1:0> | No |
| DMA1 – DMA Channel 1 | 61 | 41 | IFS1<29> | IEC1<29> | IPC10<12:10> | IPC10<9:8> | No |
| DMA2 – DMA Channel 2 | 62 | 42 | IFS1<30> | IEC1<30> | IPC10<20:18> | IPC10<17:16> | No |
| DMA3 – DMA Channel 3 | 63 | 43 | IFS1<31> | IEC1<31> | IPC10<28:26> | IPC10<25:24> | No |
| Lowest Natural Order Priority | | | | | | | |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX1XX 28/44-Pin XLP (General Purpose) Family Features"** and **TABLE 2: "PIC32MX2XX 28/44-Pin XLP (USB) Family Features"** for the lists of available peripherals.

**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | FRCDIV<2:0> | | |
| 23:16 | R/W-0 | U-0 | R/W-y | U-0 | U-0 | U-0 | U-0 | U-0 |
| | DRMEN | — | SLP2SPD | — | — | — | — | — |
| 15:8 | U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
| | — | COSC<2:0> | | | — | NOSC<2:0> | | |
| 7:0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0, HS | R/W-y | R/W-y | R/W-y |
| | CLKLOCK | — | — | SLPEN | CF | UFRCEN | SOSCEN | OSWEN(1) |

| Legend: | y = Value set from Configuration bits on POR | | HS = Hardware Set |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2
- 000 = FRC divided by 1 (default setting)

bit 23 **DRMEN:** Dream Mode Enable bit
- 1 = Dream mode is enabled
- 0 = Dream mode is disabled

bit 22 **Unimplemented:** Read as '0'

bit 21 **SLP2SPD:** Sleep Two-speed Start-up Control bit
- 1 = Use FRC as SYSCLK until the selected clock is ready
- 0 = Use the selected clock directly

bit 20-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = Reserved
- 110 = Reserved
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 **Unimplemented:** Read as '0'

**Note 1:** The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 8-6: REFO0TRIM: REFERENCE OSCILLATOR TRIM REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ROTRIM<8:1> | | | | | | | |
| 23:16 | R/W-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ROTRIM<0> | — | — | — | — | — | — | — |
| 15:8 | U-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value
111111110 = 510/512 divisor added to RODIV value
•
•
•
100000000 = 256/512 divisor added to RODIV value
•
•
•
000000010 = 2/512 divisor added to RODIV value
000000001 = 1/512 divisor added to RODIV value
000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

**Note 1:** While the ON bit (REFO0CON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

**2:** Do not write to this register when the ON bit (REFO0CON<15>) is not equal to the ACTIVE bit (REFO0CON<8>).

**3:** Specified values in this register do not take effect if RODIV<14:0> bits (REFO0CON<30:16>) = 0.

**TABLE 12-4: PORTB REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | ANSELB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSB15 | ANSB14 | ANSB13(3) | ANSB12(2) | — | — | — | — | — | — | — | — | ANSB3 | ANSB2 | ANSB1 | ANSB0 | E00F |
| 6110 | TRISB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISB15 | TRISB14 | TRISB13(3) | TRISB12(2) | TRISB11(2) | TRISB10(2) | TRISB9 | TRISB8 | TRISB7 | TRISB6(2) | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| 6120 | PORTB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | | | | | | 0000 |
| | | 15:0 | RB15 | RB14 | RB13(3) | RB12(2) | RB11(2) | RB10(2) | RB9 | RB8 | RB7 | RC6(2) | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| 6130 | LATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATB15 | LATB14 | LATB13(3) | LATB12(2) | LATB11(2) | LATB10(2) | LATB9 | LATB8 | LATB7 | LATB6(2) | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| 6140 | ODCB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCB15 | ODCB14 | ODCB13(3) | ODCB12(2) | ODCB11(2) | ODCB10(2) | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |
| 6150 | CNPUB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUB15 | CNPUB14 | CNPUB13(3) | CNPUB12(2) | CNPUB11(2) | CNPUB10(2) | CNPUB9 | CNPUB8 | CNPUB7 | CNPUB6(2) | CNPUB5 | CNPUB4 | CNPUB3 | CNPUB2 | CNPUB1 | CNPUB0 | 0000 |
| 6160 | CNPDB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDB15 | CNPDB14 | CNPDB13 | CNPDB12(2) | CNPDB11(2) | CNPDB10(2) | CNPDB9 | CNPDB8 | CNPDB7 | CNPDB6(2) | CNPDB5 | CNPDB4 | CNPDB3 | CNPDB2 | CNPDB1 | CNPDB0 | 0000 |
| 6170 | CNCONB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6180 | CNENB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEB15 | CNIEB14 | CNIEB13(3) | CNIEB11(2) | CNIEB11(2) | CNIEB10(2) | CNIEB9 | CNIEB8 | CNIEB7 | CNIEB6(2) | CNIEB5 | CNIEB4 | CNIEB3 | CNIEB2 | CNIEB1 | CNIEB0 | 0000 |
| 6190 | CNSTATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATB15 | CN STATB14 | CN STATB13(3) | CN STATB12(2) | CN STATB11(2) | CN STATB10(2) | CN STATB9 | CN STATB8 | CN STATB7 | CN STATB6(2) | CN STATB5 | CN STATB4 | CN STATB3 | CN STATB2 | CN STATB1 | CN STATB0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **12.2 "CLR, SET and INV Registers"** for more information.

**2:** This bit is not available on USB devices.

**3:** This bit is not available on VBAT devices.

**REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | TWDIS | TWIP | — | TECS<1:0> | |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to Timer1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to the Timer1 register in progress
- 0 = Asynchronous write to Timer1 register is complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
- 11 = Reserved
- 10 = External clock comes from the LPRC
- 01 = External clock comes from the T1CK pin
- 00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 18.0 OUTPUT COMPARE

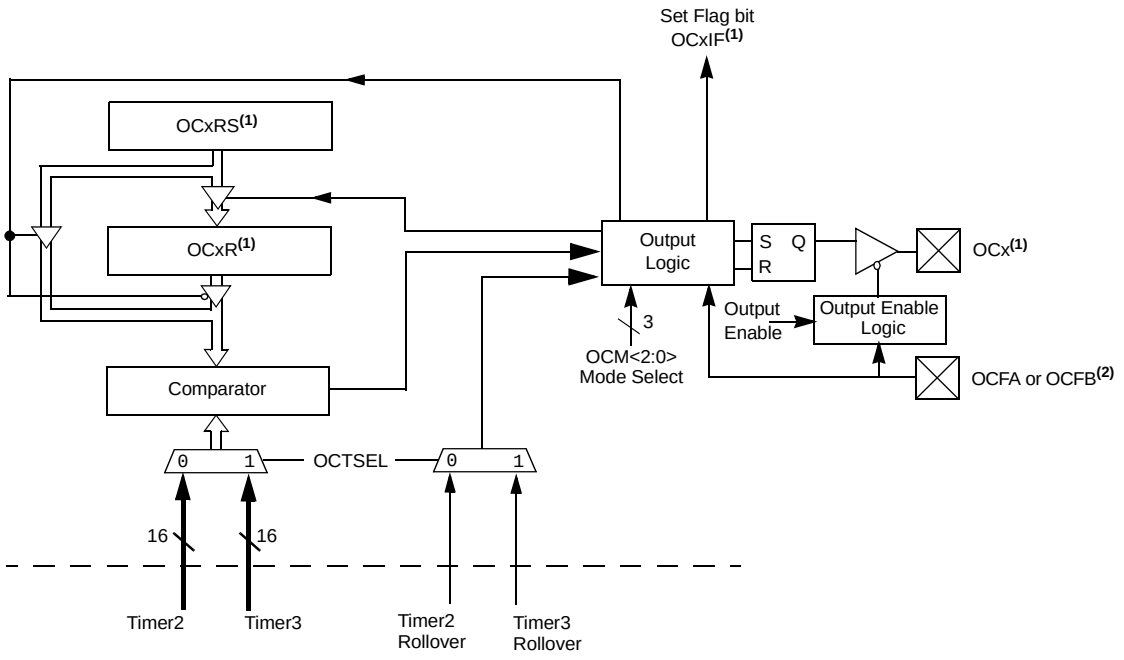
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features of the Output Compare module:

- Multiple Output Compare Modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 18-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**




**Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

**2:** The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

**REGISTER 22-3: PMADDR: PARALLEL PORT ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | CS1 | — | — | — | ADDR<10:8> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **CS1:** Chip Select 1 bit
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 13-11 **Unimplemented:** Read as '0'

bit 10-0 **ADDR<10:0>:** Destination Address bits

## 23.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The RTCC module can operate in VBAT mode when there is a power loss on the VDD pin. The RTCC will continue to operate if the VBAT pin is powered on (it is usually connected to the battery).

The following are some of the key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: day, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

**NOTES:**

**REGISTER 24-4: AD1CHS: ADC INPUT SELECT REGISTER (CONTINUED)**

bit 20-16 **CH0SA<4:0>:** Positive Input Select bits for Sample A Multiplexer Setting

11111 = Reserved
•
•
•
10010 = Reserved
10001 = Channel 0 positive input is $V_{DD}/2$
10000 = Channel 0 positive input is $V_{BAT}$
01111 = Reserved
01110 = Channel 0 positive input is $IV_{REF}$ **(1)**
01101 = Channel 0 positive input is CTMU temperature sensor (CTMUT) **(2)**
01100 = Channel 0 positive input is AN12 **(3)**
•
•
•
00001 = Channel 0 positive input is AN1
00000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

**Note 1:** See **26.0 "Comparator Voltage Reference ($CV_{REF}$)"** for more information.

**2:** See **28.0 "Charge Time Measurement Unit (CTMU)"** for more information.

**3:** AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

## 26.1 Comparator Voltage Reference Control Register

**TABLE 26-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9800 | CVRCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **12.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 29-1: DSCON: DEEP SLEEP CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | HC, R/W-y | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | DSEN(1) | — | DSGPREN | RTCDIS | — | — | — | RTCCWDIS |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | WAKEDIS | DSBOR(2) | RELEASE |

| Legend: | HC = Hardware Cleared | y = Value set from Configuration bits on POR | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **DSEN:** Deep Sleep Enable bit(1)
- 1 = Deep Sleep mode is entered on a WAIT command
- 0 = Sleep mode is entered on a WAIT command

bit 14 **Unimplemented:** Read as '0'

bit 13 **DSGPREN:** General Purpose Registers Enable bit
- 1 = General purpose register retention is enabled in Deep Sleep mode
- 0 = No general purpose register retention in Deep Sleep mode

bit 12 **RTCDIS:** RTCC Module Disable bit
- 1 = RTCC module is not enabled
- 0 = RTCC module is enabled

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RTCCWDIS:** RTCC Wake-up Disable bit
- 1 = Wake-up from RTCC is disabled
- 0 = Wake-up from RTCC is enabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **WAKEDIS:** Wake-up Source Disable bit
- 1 = External wake-up source is disabled
- 0 = External wake-up source is enabled

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
- 1 = DSBOREN was enabled and VDD dropped below the DSBOR threshold during Deep Sleep(2)
- 0 = DSBOREN was disabled, or VDD did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
- 1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
- 0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

**Note 1:** To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

**2:** Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.

**TABLE 33-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage (Note 2)** | 2.5 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage (Note 1)** | 2.0 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage (Note 3)** to Ensure Internal Power-on Reset Signal | 1.75 | — | 2.1 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.00005 | — | 0.115 | V/µs | — |
| DC18 | VBAT | **Battery Supply Voltage** | 1.94 | — | 3.6 | V | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 33-5 for BOR values.

**3:** VDD voltage must remain below VPOR for a minimum of 200 µs to ensure POR.

**TABLE 33-5: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.(1)** | **Typ.** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD transition high-to-low **(Note 2)** | 2.2 | — | 2.384 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

**TABLE 33-8: DC CHARACTERISTICS: IDLE CURRENT ($I_{IDLE}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current ($I_{IDLE}$): Core Off, Clock on Base Current (Notes 1, 4)** | | | | | | |
| DC30a | 0.6 | — | mA | 4 MHz **(Note 3)** | | |
| DC31a | 1.5 | — | mA | 10 MHz | | |
| DC32a | 4.5 | — | mA | 30 MHz **(Note 3)** | | |
| DC33a | 7.5 | — | mA | 50 MHz **(Note 3)** | | |
| DC34a | 10.5 | — | mA | 72 MHz | | |
| DC37a | 100 | — | µA | -40°C | 3.3V | LPRC (31 kHz) **(Note 3)** |
| DC37b | 250 | — | µA | +25°C | | |
| DC37c | 380 | — | µA | +85°C | | |

**Note 1:** The test conditions for $I_{IDLE}$ current measurements are as follows:

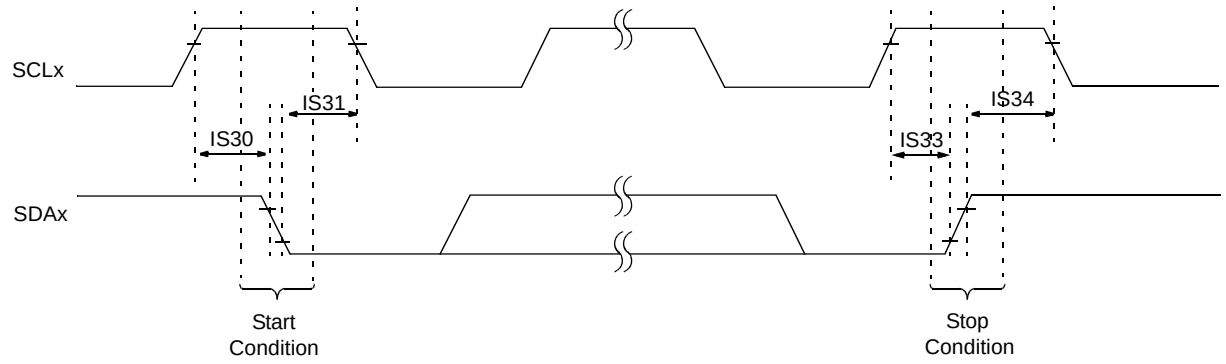
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

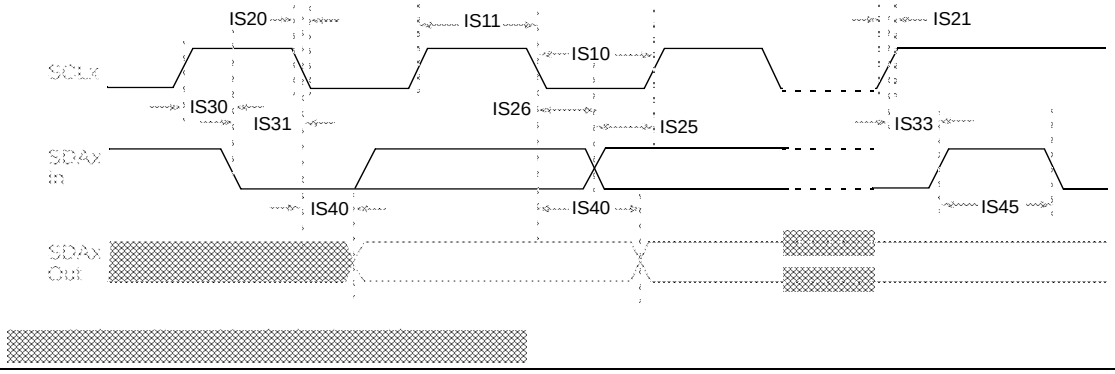
**4:** $I_{IDLE}$ electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

**FIGURE 33-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 33-1 for load conditions.

**FIGURE 33-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**



**NOTES:**