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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8×8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx174f256d-i-ml

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TABLE 5: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN	SOIC	(TOP	VIEW) ^(1,2,3)
--------	------	------	------	----------------------



28

PIC32MX255F128B PIC32MX275F256B

Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	VBUS
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1	19	Vss
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	VCAP
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3	21	D+
8	Vss	22	D-
9	OSC1/CLKI/RPA2/RA2	23	VUSB3V3
10	OSC2/CLKO/RPA3/PMA0/RA3	24	VBAT
11	SOSCI/RPB4/CTED11/RB4 ⁽⁴⁾	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	Vdd	27	AVss
14	TMS/RPB5/USBID/PMRD/RB5	28	AVdd

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

4: This is an input-only pin.

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

	Pi	in Number ⁽	1)								
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description					
					Oscillators	·					
CLKI 6 9 30 I ST/CMOS External clock source input. Always associated with OSC1 pin function.											
CLKO	7	10	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.					
OSC1	6	9	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.					
OSC2	7	10	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.					
SOSCI	8	11	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.					
SOSCO	9	12	34	0	_	32.768 kHz low-power oscillator crystal output.					
REFCLKI	PPS	PPS	PPS	I	ST	Reference Input Clock					
REFCLKO	PPS	PPS	PPS	0	_	Reference Output Clock					
Legend:	CMOS = CN ST = Schmi TTL = TTL i	MOS compa tt Trigger in nput buffer	atible input put with CN	Analog = Analog input $P = Power$ $O = Output$ $I = Input$ $PPS = Peripheral Pin Select$ $- = N/A$ "In Diagramme" section for device pin surjich little							

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

	P	Pin Number ⁽¹⁾						
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description		
			re					
IC1	PPS	PPS	PPS	I	ST	Input Capture Input 1-5		
IC2	PPS	PPS	PPS	I	ST			
IC3	PPS	PPS	PPS	I	ST			
IC4	PPS	PPS	PPS	I	ST			
IC5	PPS	PPS	PPS	I	ST			
Legend:	CMOS = C	MOS compa	atible input	Analog = Analog input	P = Power			
	ST = Schmi	tt Trigger in	put with Cl	MOS lev	els	O = Output	I = Input	
	TTL = TTL i	nput buffer				PPS = Peripheral Pin Select	— = N/A	

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Program Memory" (DS60001121), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/44-pin XLP Family devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program the Flash memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming[™] (ICSP[™])

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site (www.microchip.com).

Note: The Flash page size on PIC32MX-1XX/2XX 28/44-pin XLP Family devices is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	_	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
7:0	—	—	—	—	—	_	—	SWRST ^(1,2)

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend:	HC = Hardware Cleared			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-1 Unimplemented: Read as '0'

- bit 0 SWRST: Software Reset Trigger bit^(1,2) 1 = Enable software Reset event
 - 0 = No effect
- Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.
 - 2: Once this bit is set, any read of the RSWRST register will cause a reset to occur.

REGISTER 9-8: DCHXECON: DMA CHANNEL X EVENT CONTROL REGISTER									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24		—	—		—	_	—	—	
22:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
23.10	CHAIRQ<7:0> ⁽¹⁾								
15.0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
10.0	CHSIRQ<7:0> ⁽¹⁾								
7.0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	
7.0	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN		_	_	

REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Legend:	S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-24 Unimplemented: Read as '0'

bit 23-16	CHAIRQ<7:0>: Channel Transfer Abort IRQ bits ⁽¹⁾
	11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
	•
	•
	•
	00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
1.1.45.0	OUCOUDE = Interrupt 0 will abort any transfers in progress and set CHAIF flag
bit 15-8	CHSIRQ<7:0>: Channel Transfer Start IRQ bits ^{1/2}
	11111111 = Interrupt 255 will initiate a DMA transfer
	•
	•
	00000001 = Interrupt 1 will initiate a DMA transfer
	0000000 = Interrupt 0 will initiate a DMA transfer
bit 7	CFORCE: DMA Forced Transfer bit
	1 = A DMA transfer is forced to begin when this bit is written to a '1'
	0 = This bit always reads '0'
bit 6	CABORT: DMA Abort Transfer bit
	1 = A DMA transfer is aborted when this bit is written to a '1'
	0 = This bit always reads '0'
bit 5	PATEN: Channel Pattern Match Abort Enable bit
	1 = Abort transfer and clear CHEN on pattern match
	0 = Pattern match is disabled
bit 4	SIRQEN: Channel Start IRQ Enable bit
	1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
	0 = Interrupt number CHSIRQ is ignored and does not start a transfer
bit 3	AIRQEN: Channel Abort IRQ Enable bit
	1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
	0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer
bit 2-0	Unimplemented: Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
31.24		CHEW1<31:24>									
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
23:16	CHEW1<23:16>										
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
15.0	CHEW1<15:8>										
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
7:0		CHEW1<7:0>									

REGISTER 10-6: CHEW1: CACHE WORD 1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 10-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
31:24				CHEW2<	31:24>								
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
23.10		CHEW2<23:16>											
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
15.6	CHEW2<15:8>												
7.0	R/W-x R/W-x		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
7:0				CHEW2	<7:0>								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	_	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		—	—		—	—	_	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0		—	—		—	—	_	—
	R/WC-0, HS	R-0	R/WC-0, HS					
7:0	STALLIE		RESUMEIE(2)		TRNIF(3)	SOFIE	LIERRIE(4)	URSTIF ⁽⁵⁾
	OTALLII		RECOMEN			0011	OLIVIA	DETACHIF ⁽⁶⁾

REGISTER 11-6: U1IR: USB INTERRUPT REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable	Hardware Settable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

bit 7		STALLIF: STALL Handshake Interrupt bit
	-	1 = In Host mode a STALL handshake was received during the handshake phase of the transaction
	I	In Device mode a STALL handshake was transmitted during the handshake phase of the transaction
	(0 = STALL handshake has not been sent
bit 6		ATTACHIF: Peripheral Attach Interrupt bit ⁽¹⁾
	-	1 = Peripheral attachment was detected by the USB module
	(0 = Peripheral attachment was not detected
bit 5	I	RESUMEIF: Resume Interrupt bit ⁽²⁾
	-	1 = K-State is observed on the D+ or D- pin for 2.5 μs
	(0 = K-State is not observed
bit 4		IDLEIF: Idle Detect Interrupt bit
	-	1 = Idle condition detected (constant Idle state of 3 ms or more)
	(0 = No Idle condition detected
bit 3	1	TRNIF: Token Processing Complete Interrupt bit ⁽³⁾
	-	1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
	(0 = Processing of current token not complete
bit 2		SOFIF: SOF Token Interrupt bit
	-	1 = SOF token received by the peripheral or the SOF threshold reached by the host
	(0 = SOF token was not received nor threshold reached
bit 1	l	UERRIF: USB Error Condition Interrupt bit ⁽⁴⁾
	-	1 = Unmasked error condition has occurred
	(0 = Unmasked error condition has not occurred
bit 0	l	URSTIF: USB Reset Interrupt bit (Device mode) ⁽⁵⁾
	-	1 = Valid USB Reset has occurred
	(0 = No USB Reset has occurred
	I	DETACHIF: USB Detach Interrupt bit (Host mode) ⁽⁹⁾
	-	1 = Peripheral detachment was detected by the USB module
	(0 = Peripheral detachment was not detected
Note	1.	This hit is valid only if the HOSTEN hit is set (see Register 11-11), there is no activity on the USB for
Note	••	2.5 us and the current bus state is not SE0
	2 .	When not in Suspend mode, this interrupt should be disabled
	2.	Clearing this hit will course the STAT FIEO to advance
	J.	Cleaning uns bit will cause the STAT FIFO to advance.
	4:	
	5:	Device mode.
	6:	Host mode.

TABLE 12-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

sse				Bits															
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
EA 5 4	LIACTER	31:16	_	_	-	_		_	I	_		—	I			—	_		0000
1 АЗ4	UTCTSK	15:0	_	—		—	—	—	_	—	—	—	_	—		U1CTS	R<3:0>		0000
		31:16	_	—		—	—	—	_	—	—	—	_	—	_	—	—	_	0000
1 АЗО	UZKAK	15:0	_	—	_	—	_	—	-		_	_	_	—	U2RXR<3:0>				
EAEC	LIDCTOR	31:16	_	—	_	—	—	—	_	—	—	—	_	—	_	—	—	_	0000
FASC	02013K	15:0	—	—	-	—	_	_	-	_	_	—	_	—	U2CTSR<3:0>				0000
EVON		31:16	_	—	_	—	—	—	_	—	—	—	_	—	_	—	—	_	0000
1 A04	SDITR	15:0	_	—	_	—	—	—	_	—	—	—	_	—		SDI1F	R<3:0>		0000
EV 00	SS1D	31:16	_	—	_	—	—	—	_	—	—	—	_	—	_	—	—	_	0000
T A00	551K	15:0	_	—	_	—	—	—	_	—	—	—	_	—		SS1R	<3:0>		0000
EA00	20120	31:16	_	—	_	—	—	—	_	—	—	—	_	—	_	—	—	_	0000
1 A90	SDIZK	15:0	_	—	_	—	_	—	-		_	_	_	—		SDI2F	R<3:0>		0000
EA04	660B	31:16	—	—	-	—	_	_	-	_	_	—	_	—	—	—	—	-	0000
17,94	332R	15:0	_	_	_	—	_	_	_	—	_	—	_	—		SS2R	<3:0>		0000
		31:16	_	_	_	—	_	_	_	—	_	—	_	—	_	_	_	_	0000
FAB8 RI	REFULKIK	15:0	-	_	—	_	—	_	—	_	—	—	—	_		REFCL	(IR<3:0>		0000

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
 - 11 = 1:256 prescale value
 - 10 = 1:64 prescale value
 - 01 = 1:8 prescale value
 - 00 = 1:1 prescale value
- bit 3 Unimplemented: Read as '0'
- bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit
 - <u>When TCS = 1:</u> 1 = External clock input is synchronized
 - 0 = External clock input is not synchronized
 - When TCS = 0:
 - This bit is ignored.
- bit 1 **TCS:** Timer Clock Source Select bit 1 = External clock is defined by the TECS<1:0> bits 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

15.1 Watchdog Timer Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

Bits														6					
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
Table WDTCLRKEY<15:0>										0000									
P600 WDTCON*7 15:0 ON RUNDIV<4:0>							_	_	WDTWINEN	xxxx									

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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REGISTI	ER 19-1: SPIxCON: S	PI CONTROL REGISTER (CONTINUED)										
bit 17	SPIFE: Frame Sync Pulse	e Edge Select bit (Framed SPI mode only)										
	1 = Frame synchronizatio	on pulse coincides with the first bit clock										
hit 16	0 = Frame synchronizatio	on pulse precedes the first bit clock										
DIL TO	1 = Enhanced Buffer mod	e is enabled										
	0 = Enhanced Buffer mod	e is disabled										
bit 15	ON: SPI Peripheral On bit	₍ (1)										
	1 = SPI Peripheral is ena	bled										
	0 = SPI Peripheral is disa	abled										
bit 14	Unimplemented: Read as	s '0'										
bit 13	SIDL: Stop in Idle Mode bit											
	\perp = Discontinue module ope	peration when the device enters Idle mode										
hit 12	DISSDO: Disable SDOx n	sin bit										
511 12	1 = SDOx pin is not used	by the module. Pin is controlled by associated PORT register										
	0 = SDOx pin is controlle	d by the module										
bit 11-10	MODE<32,16>: 32/16-Bit	Communication Select bits										
	When AUDEN = 1:											
	MODE32 MODE16	Communication										
		24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame										
	0 1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame										
	0 0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame										
	When AUDEN = 0:											
	MODE32 MODE16	Communication										
	1 x	32-bit										
		8-bit										
bit 9	SMP: SPI Data Input Sam	nple Phase bit										
	Master mode (MSTEN = 1	<u>.):</u>										
	1 = Input data sampled at	t end of data output time										
	0 = Input data sampled at Slave mode (MSTEN = 0)	t middle of data output time										
	SMP value is ignored whe	<u>.</u> In SPI is used in Slave mode. The module always uses SMP = 0.										
	To write a '1' to this bit. the	e MSTEN value = 1 must first be written.										
bit 8	CKE: SPI Clock Edge Sel	lect bit ⁽³⁾										
	1 = Serial output data cha	anges on transition from active clock state to Idle clock state (see the CKP bit)										
	0 = Serial output data cha	anges on transition from Idle clock state to active clock state (see the CKP bit)										
bit 7	SSEN: Slave Select Enab	ole (Slave mode) bit										
	$1 = \frac{SSx}{SSx}$ pin used for Slav	/e mode Slove mede, pip controlled by part function										
hit 6	CKP: Clock Polarity Selec	Slave mode, pin controlled by port function.										
bit 0	1 = Idle state for clock is a	a high level; active state is a low level										
	0 = Idle state for clock is	a low level; active state is a high level										
••												
Note 1:	When using the 1:1 PBCI	LK divisor, the user's software should not read or write the peripheral's SFRs in										
о.	This hit can only be writte	α when the ON bit = 0										
2:	This bit is not used in the	Framed SPI mode. The user should program this hit to '0' for the Framed SPI										
5.	mode (FRMEN = 1).											
4:	When AUDEN = 1, the SF	PI module functions as if the CKP bit is equal to '1', regardless of the actual value										
	of CKP.											

REGISTE	ER 20-1: I2CxCON: I ² C CONTROL REGISTER (CONTINUED)							
bit 7	GCEN: General Call Enable bit (when operating as I ² C slave) 1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for recention)							
	0 = General call address is disabled							
bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with SCLREL bit. 1 = Enable software or receive clock stretching 0 = Disable software or receive clock stretching							
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive) Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Send a NACK during an Acknowledge sequence 0 = Send an ACK during an Acknowledge sequence							
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I^2C master, applicable during master receive)							
	 1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence. 0 = Acknowledge sequence not in progress 							
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)							
	 1 = Enables Receive mode for I²C. Hardware clear at end of eighth bit of master receive data byte. 0 = Receive sequence not in progress 							
bit 2	PEN: Stop Condition Enable bit (when operating as I ² C master)							
	1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.0 = Stop condition not in progress							
bit 1	RSEN: Repeated Start Condition Enable bit (when operating as I ² C master)							
	 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence. 0 = Repeated Start condition not in progress 							
bit 0	SEN: Start Condition Enable bit (when operating as I ² C master)							
	1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.0 = Start condition not in progress							

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Herefyings out or clear when Start, Represend Start or Stop detected
hit 2	Stort bit
DIL D	1 = Indicates that a Start (or Repeated Start) bit has been detected last
	 0 = Start bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	 1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave Hardware set or clear after reception of I²C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	 1 = Receive complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

0 = Transmit complete, I2CxTRN is empty

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0							
31.24	—	—	—	—	_	—	—	—	
00.40	U-0	U-0							
23:16	—	—	—	—	—	—	—	—	
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	0N ⁽¹⁾	—	SIDL			FORM<2:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC	
		SSRC<2:0>		CLRASAM	_	ASAM	SAMP ⁽²⁾	DONE ⁽³⁾	

REGISTER 24-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode

bit 12-11 Unimplemented: Read as '0'

- bit 10-8 **FORM<2:0>:** Data Output Format bits
 - 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)

 - 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
 - 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
 - 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
 - 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

 - 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 24-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	CH0NB	—	—			CH0SB<4:0>		
00.40	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CH0NA	—	—	CH0SA<4:0>				
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—		—	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_		_	

Legend:

bit 23

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 CH0NB: Negative Input Select bit for Sample B 1 = Channel 0 negative input is AN1 0 = Channel 0 negative input is VREFL bit 30-29 Unimplemented: Read as '0' bit 28-24 CH0SB<4:0>: Positive Input Select bits for Sample B 11111 = Reserved •

- 10010 = Reserved
 10001 = Channel 0 positive input is VDD/2
 10000 = Channel 0 positive input is VBAT
 01111 = Reserved
 01101 = Channel 0 positive input is IVREF⁽¹⁾
 01101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)⁽²⁾
 01100 = Channel 0 positive input is AN12⁽³⁾
 .
 .
 00001 = Channel 0 positive input is AN1
 00000 = Channel 0 positive input is AN1
 00000 = Channel 0 positive input is AN0
 CHONA: Negative Input Select bit for Sample A Multiplexer Setting⁽¹⁾
 1 = Channel 0 negative input is AN1
 0 = Channel 0 negative input is VREFL
- bit 22-21 Unimplemented: Read as '0'

Note 1: See 26.0 "Comparator Voltage Reference (CVREF)" for more information.

- 2: See 28.0 "Charge Time Measurement Unit (CTMU)" for more information.
- 3: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.



FIGURE 29-1: XLP DEVICE BLOCK DIAGRAM

NOTES:

DC CHARA	CTERISTICS	6	Standard Op (unless other Operating terr	erating Conditions: 2.5V to rwise stated) nperature $-40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +105^{\circ}$	3.6V °C for Industrial 5°C for V-temp
Parameter No.	Typical ⁽³⁾	Max.	Units	Co	nditions
Operating (Current (IDD)	(Notes 1, 2, 5)			
DC20	1.7		mA	4 M⊢	łz (Note 4)
DC21	4		mA	1	0 MHz
DC22	12.5	_	mA	30 MI	Hz (Note 4)
DC23	20	_	mA	50 MI	Hz (Note 4)
DC24	29	—	mA	7	2 MHz
DC25	100		μA	+25°C, 3.3V	LPRC (31 kHz) (Note 4)

TABLE 33-7: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

- 2: The test conditions for IDD measurements are as follows:
 - Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to Vss
 - $\overline{\text{MCLR}}$ = VDD
 - CPU executing while(1) statement from Flash
 - RTCC and JTAG are disabled
- **3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

FIGURE 33-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



TABLE 33-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

АС СНА	RACTER	ISTICS	Standar (unless Operatin	d Operating C otherwise stat g temperature	onditions: ed) -40°C ≤ [−] -40°C ≤ [−]	2.5V to Га ≤ +85° Га ≤ +105	3.6V C for Industrial ^{s°} C for V-temp
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
OC10	TCCF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	_	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-9: OCx/PWM MODULE TIMING CHARACTERISTICS



TABLE 33-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHAF	RACTERIST	rics	Standard (unless of Operating	d Operating C otherwise sta g temperature	Conditions ited) -40°C ≤ -40°C ≤	s: 2.5V to 3 ≦ TA ≤ +85° ≦ TA ≤ +105	3.6V C for Industrial °C for V-temp
Param No.	Symbol	Characteristics ⁽¹⁾	Min	Typical ⁽²⁾	Max	Units	Conditions
OC15	Tfd	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	50	—	_	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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