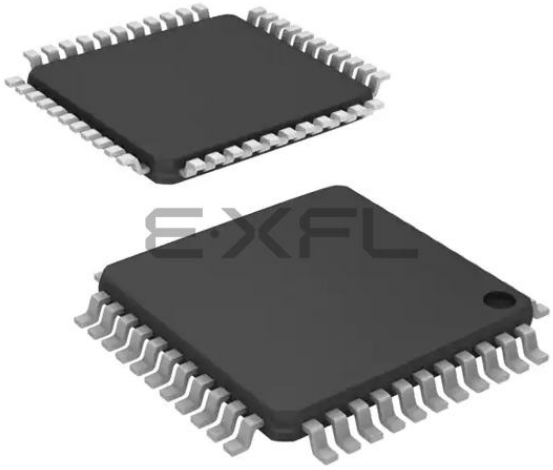

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx174f256d-i-pt

TABLE 1-16: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number[1]			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Power and Ground						
TMS	19[2]	22[2]	9[2]	I	ST	JTAG Test mode select pin
	11[3]	14[3]	41[3]			
TCK	14	17	13	I	ST	JTAG test clock input pin
TDI	13	16	35	O	—	JTAG test data input pin
TDO	15	18	32	O	—	JTAG test data output pin
Programming/Debugging						
PGED1	18[2]	21[2]	8[2]	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
	3[3]	6[3]	23[3]			
PGEC1	19[2]	22[2]	9[2]	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
	4[3]	7[3]	24[3]			
PGED2	1	4	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	2	5	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	11[2]	14[2]	41[2]	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
	27[3]	2[3]	19[3]			
PGEC3	12[2]	15[2]	42[2]	I	ST	Clock input pin for Programming/ Debugging Communication Channel 3
	28[3]	3[3]	20[3]			
PGED4	—	—	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4
PGEC4	—	—	13	I	ST	Clock input pin for Programming/ Debugging Communication Channel 4
$\overline{MCLR}$	26	1	18	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for General Purpose devices only.

3: Pin number for USB devices only.

2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

Crystal manufacturer recommended: $C1 = C2 = 15\ pF$

Therefore:

$$C_{LOAD} = \{([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} + \text{estimated oscillator PCB stray capacitance}$$

$$= \{([5 + 15][5 + 15]) / [5 + 15 + 15 + 5] \} + 2.5\ pF$$

$$= \{([20][20]) / [40] \} + 2.5$$

$$= 10 + 2.5 = 12.5\ pF$$

Rounded to the nearest standard value or 13 pF in this example for Primary Oscillator crystals “C1” and “C2”.

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

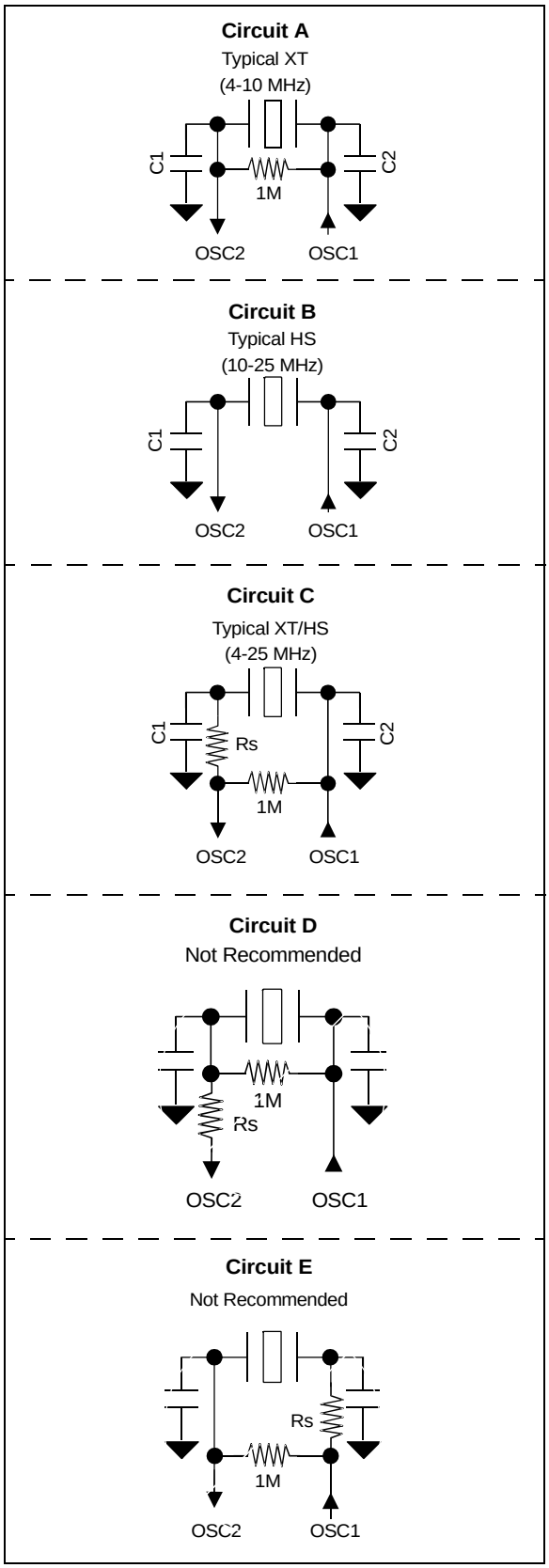
- Select a crystal with a lower “minimum” power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing “ESR” rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit “C” in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 *“PICmicro® Microcontroller Oscillator Design Guide”*
- AN826 *“Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices”*
- AN849 *“Basic PICmicro® Oscillator Design”*

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS00:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC00:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 8-4: UPLLCON: USB PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	UPLLODIV<2:0>		
23:16	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	UPLLMULT<2:0>		
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	UPLLIDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **UPLLODIV<2:0>:** USB PLL Output Clock Divider bits
- 111 = PLL Divide by 16
- 110 = PLL Divide by 12
- 101 = PLL Divide by 8
- 100 = PLL Divide by 6
- 011 = PLL Divide by 4
- 010 = PLL Divide by 3
- 001 = PLL Divide by 2
- 000 = PLL Divide by 1

bit 23-19 **Unimplemented:** Read as '0'

bit 18-16 **UPLLMULT<2:0>:** USB PLL Multiplier bits
- 111 = Multiply by 24
- 110 = Multiply by 21
- 101 = Multiply by 20
- 100 = Multiply by 19
- 011 = Multiply by 18
- 010 = Multiply by 17
- 001 = Multiply by 16
- 000 = Multiply by 15

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Clock Divider bits
- 111 = Divide by 12
- 110 = Divide by 10
- 101 = Divide by 6
- 100 = Divide by 5
- 011 = Divide by 4
- 010 = Divide by 3
- 001 = Divide by 2
- 000 = Divide by 1

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = A change in the ID state was detected
- 0 = No change in the ID state was detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = A change on the session valid input was detected
- 0 = No change on the session valid input was detected

REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<15:9>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** Buffer Descriptor Table Base Address bits

This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

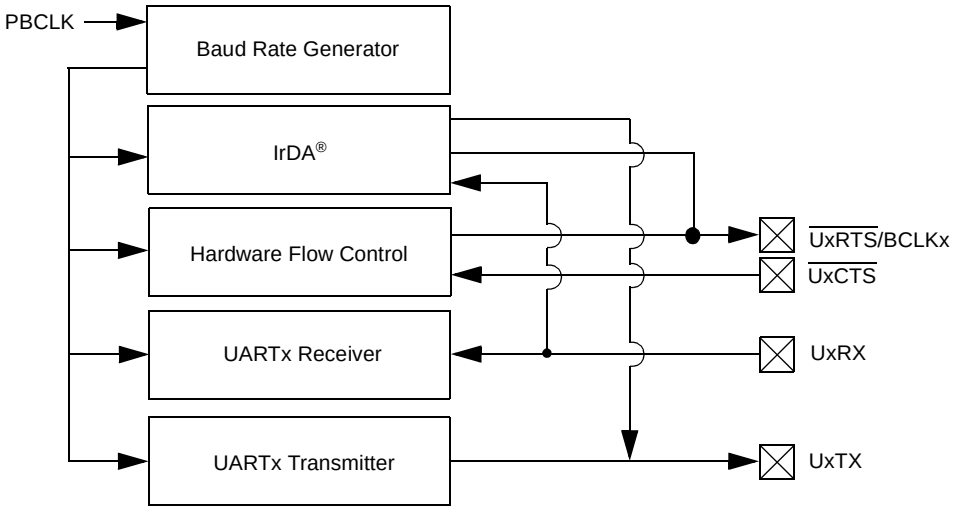
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/44-pin XLP Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The UART module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The following are key features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 33.4 bps to 17.5 Mbps at 72 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support
- Auto-baud support
- Ability to receive data during Sleep mode

Figure 21-1 illustrates a simplified block diagram of the UART module.

FIGURE 21-1: UART SIMPLIFIED BLOCK DIAGRAM



Note: Not all pins are available for all UART modules. Refer to the device-specific pin diagram for more information.

REGISTER 23-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	RTCCLKSEL<1:0>		RTC OUTSEL<1>(2)
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTC OUTSEL<0>(2)	RTC CLKON	—	—	RTC WREN(3)	RTC SYNC	HALFSEC(4)	RTCOE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute
•
•
•
1000000000 = Minimum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON:** RTCC On bit(1)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables RTCC operation when CPU enters Idle mode
0 = Continue normal operation when CPU enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 23-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	HR10<1:0>		HR01<3:0>			
23:16	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	MIN10<2:0>			MIN01<3:0>			
15:8	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	SEC10<2:0>			SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HR10<1:0>:** Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MIN10<2:0>:** Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15 **Unimplemented:** Read as '0'

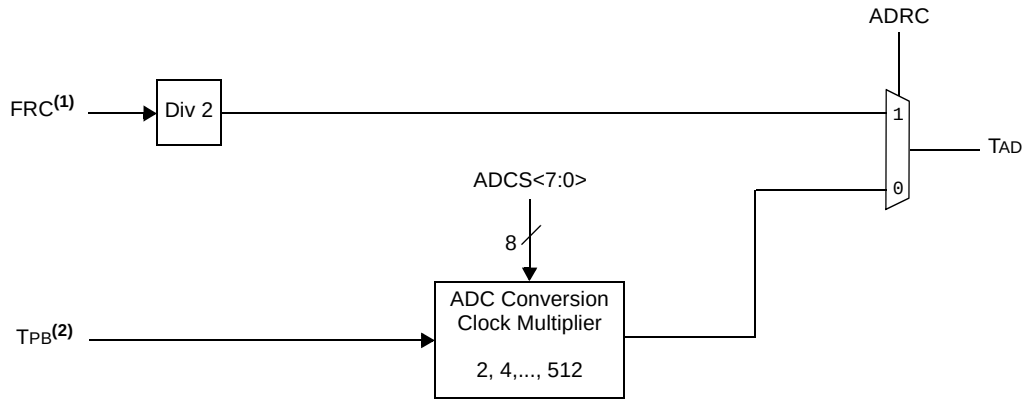
bit 14-12 **SEC10<2:0>:** Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

NOTES:

FIGURE 24-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: See **33.0 "Electrical Characteristics"** for the exact FRC clock value.

2: Refer to Figure 8-1 in **8.0 "Oscillator Configuration"** for more information.

TABLE 33-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
		Program Flash Memory(3)					
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.5	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.5	—	3.6	V	—
D134	TRETD	Characteristic Retention	10	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	—	471	—	FRC Cycles	See **Note 4**
D136	TRW	Row Write Cycle Time	—	8020	—		See **Note 2,4**
D137	TPE	Page Erase Cycle Time	—	240114	—		See **Note 4**
	TCE	Chip Erase Cycle Time	—	640304	—		See **Note 4**

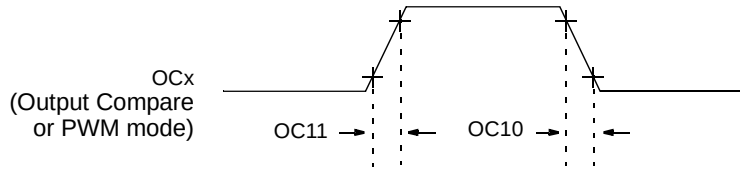
Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the *“PIC32 Flash Programming Specification”* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 33-20) and FRC tuning values (See Register 8-2).

FIGURE 33-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

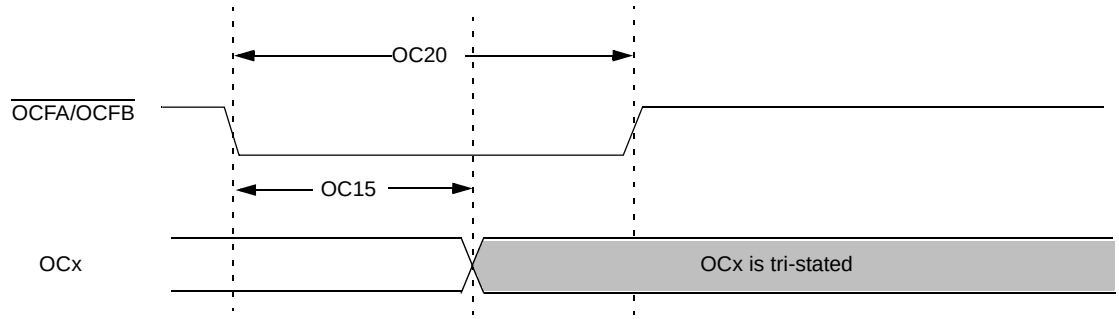
TABLE 33-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

TABLE 33-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 33-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250		ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode **(Note 1)**	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 1)**	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 34-6: TYPICAL FRC FREQUENCY @ VDD = 3.3V

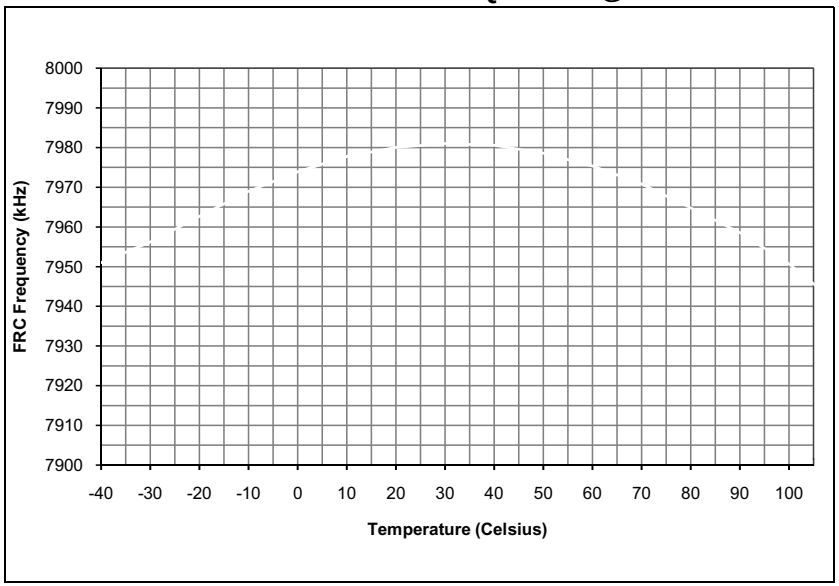


FIGURE 34-7: TYPICAL LPRC FREQUENCY @ VDD = 3.3V

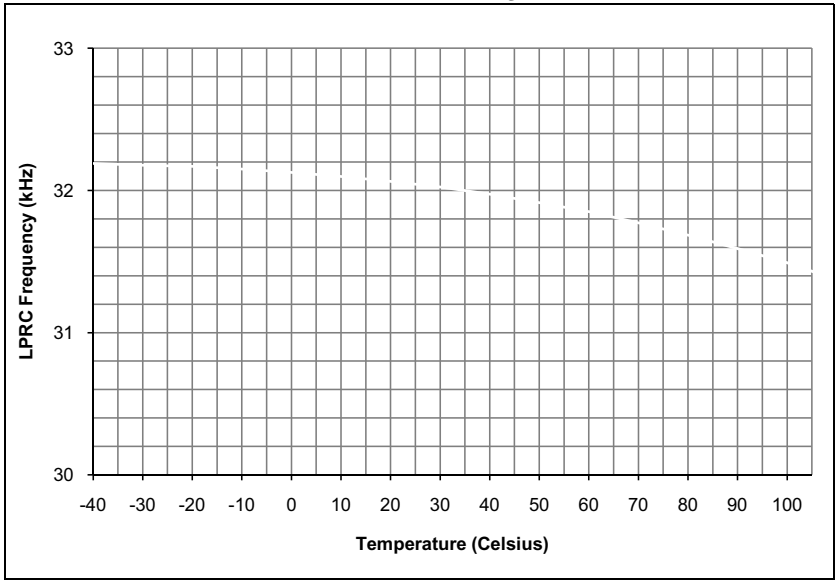
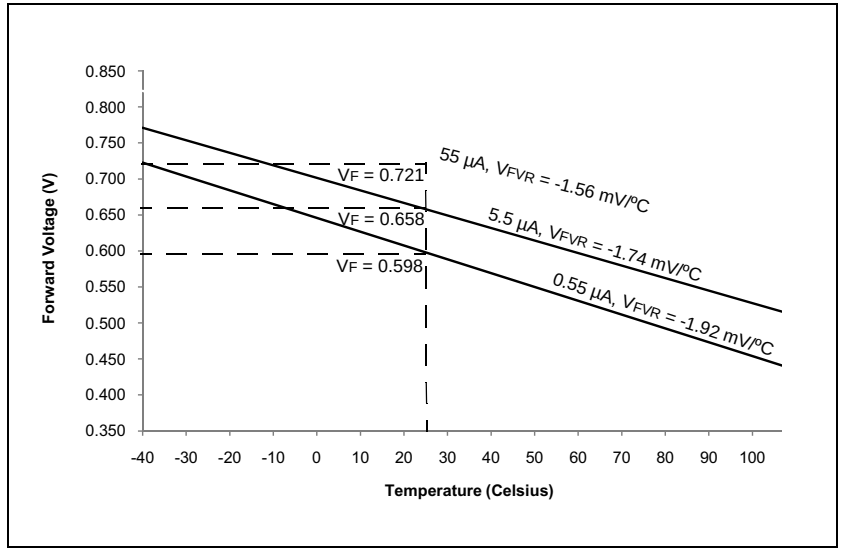


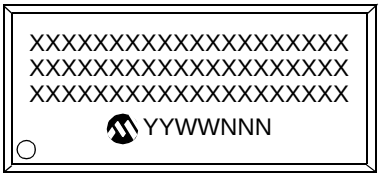
FIGURE 34-8: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE



35.0 PACKAGING INFORMATION

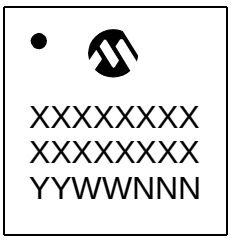
35.1 Package Marking Information

28-Lead SOIC



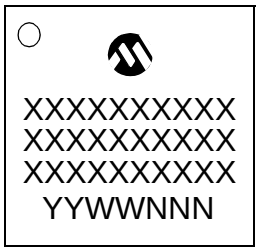
Example

28-Lead QFN

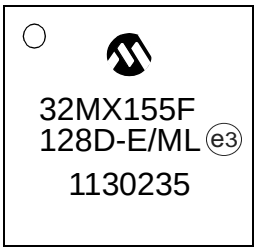


Example

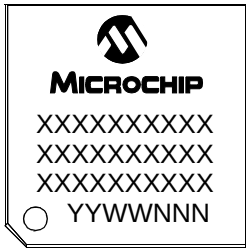
44-Lead QFN



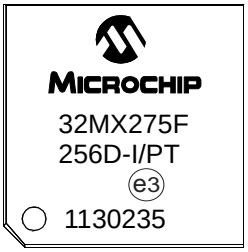
Example



44-Lead TQFP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

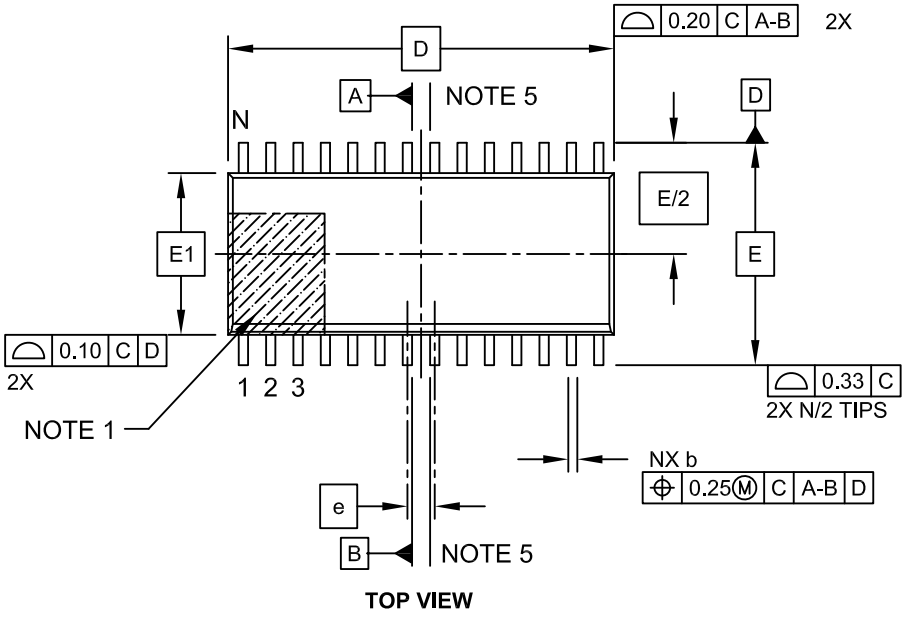
Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

35.2 Package Details

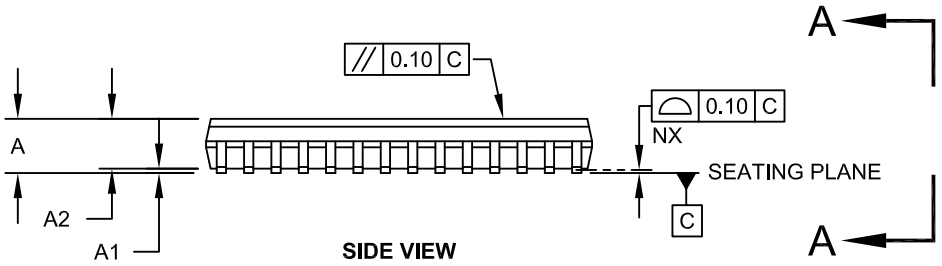
This section provides the technical details of the packages.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

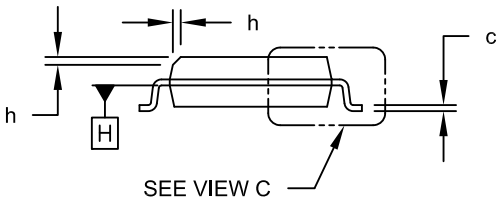
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

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