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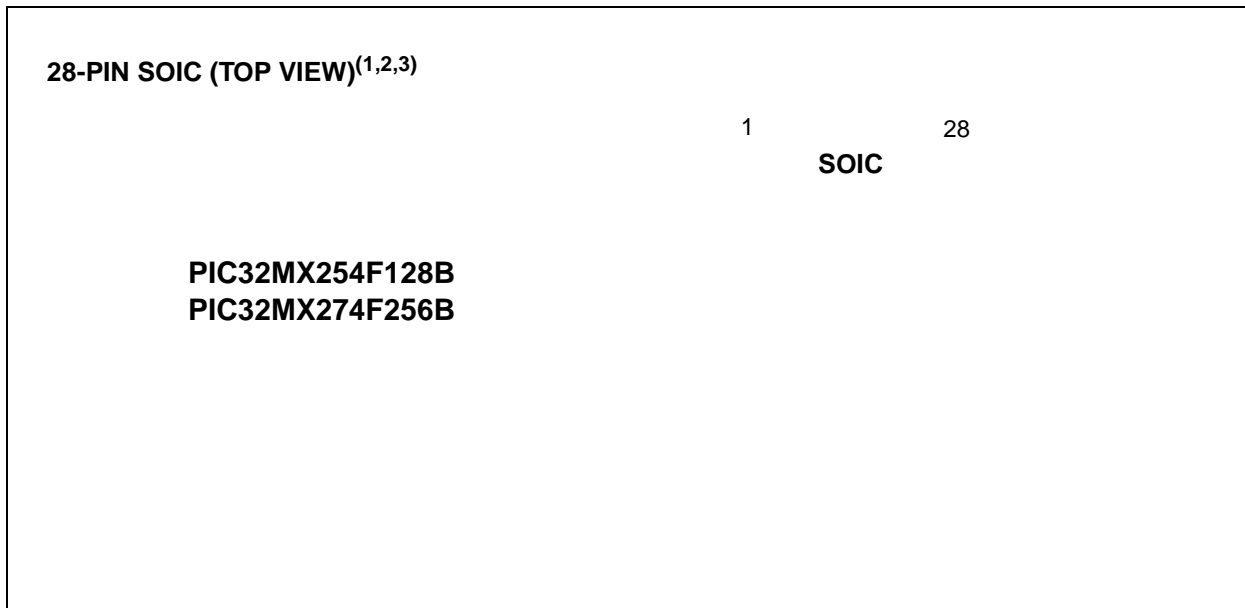
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx254f128bt-v-mm

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES WITHOUT VBAT



Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	VBUS
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1	19	Vss
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	VCAP
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	21	D+
8	Vss	22	D-
9	OSC1/CLKI/RPA2/RA2	23	VUSB3V3
10	OSC2/CLKO/RPA3/PMA0/RA3	24	AN11/RPB13/CTPLS/PMRD/RB13
11	SOSCI/RPB4/CTED11/RB4 ⁽⁴⁾	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	TMS/RPB5/USBID/RB5	28	AVDD

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 “Peripheral Pin Select” for restrictions.
- 2: Every I/O port pin (RAX-RBx) can be used as a change notification pin (CNAX-CNBx). See 12.0 “I/O Ports” for more information.
- 3: Shaded pins are 5V tolerant.
- 4: This is an input-only pin.

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TABLE 1-6: PORTA THROUGH PORTC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/TQFP			
PORTC						
RC0	—	—	25	I/O	ST	PORTC is a bidirectional I/O port
RC1	—	—	26	I/O	ST	
RC2	—	—	27	I/O	ST	
RC3	—	—	36	I/O	ST	
RC4	—	—	37	I/O	ST	
RC5	—	—	38	I/O	ST	
RC6	—	—	2	I/O	ST	
RC7	—	—	3	I/O	ST	
RC8	—	—	4	I/O	ST	
RC9	—	—	5	I/O	ST	

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 TTL = TTL input buffer PPS = Peripheral Pin Select — = N/A

- Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.
2: Pin number for General Purpose devices only.
3: This pin is not available for devices with VBAT.
4: This pin is not available for devices with USB.

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2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/44-pin XLP Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “Decoupling Capacitors”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “Decoupling Capacitors”)
- VCAP pin (see 2.3 “Capacitor on Internal Voltage Regulator (VCAP)”)
- MCLR pin (see 2.4 “Master Clear (MCLR) Pin”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 “ICSP Pins”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “External Oscillator Pins”)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 μF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

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REGISTER 8-8: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	UPLLRDY
7:0	R-0	U-0	R-0	R-0	U-0	R-0	R-0	R-0
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	DIVSPLLRDY	FRCRDY

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **UPLLRDY:** USB PLL (UPLL) Ready Status bit

1 = UPLL is ready
 0 = UPLL is not ready

bit 7 **SPLLRDY:** System PLL (SPLL) Ready Status bit

1 = SPLL is ready
 0 = SPLL is not ready

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** Low-Power RC (LPRC) Oscillator Ready Status bit

1 = LPRC is stable and ready
 0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Status bit

1 = SOSC is stable and ready
 0 = SOSC is disabled or not operating

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (Posc) Ready Status bit

1 = POSC is stable and ready
 0 = POSC is disabled or not operating

bit 1 **DIVSPLLRDY:** Divided System PLL Ready Status bit

1 = Divided System PLL is ready
 0 = Divided System PLL is not ready

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit

1 = FRC is stable and ready
 0 = FRC is disabled for not operating

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REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>**: CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Bits greater than PLEN will return '0' on any read.

REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>**: CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = Enable the XOR input to the Shift register

0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

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REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a
 pattern match event occurs
 0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
 0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
 1 = A channel address error has been detected (either the source or the destination address is invalid)
 0 = No interrupt is pending

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REGISTER 10-8: CHEW3: CACHE WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW3<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW3<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW3<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW3<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CHEW3<31:0>**: Word 3 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>)
 Readable only if the device is not code-protected.

Note: This register is a window into the cache data array and is readable only if the device is not code-protected.

REGISTER 10-9: CHELRU: CACHE LRU REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	CHELRU<24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHELRU<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHELRU<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHELRU<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-25 **Unimplemented**: Write '0'; ignore read
 bit 24-0 **CHELRU<24:0>**: Cache Least Recently Used State Encoding bits
 Indicates the pseudo-LRU state of the cache.

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REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

bit 1 **CRC5EF:** CRC5 Host Error Flag bit⁽⁴⁾
 1 = Token packet rejected due to CRC5 error
 0 = Token packet accepted
 EOFEF: EOF Error Flag bit^(3,5)
 1 = An EOF error condition was detected
 0 = No EOF error condition was detected

bit 0 **PIDEF:** PID Check Failure Flag bit
 1 = PID check failed
 0 = PID check passed

- Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
- 2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
- 3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
- 4:** Device mode.
- 5:** Host mode.

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REGISTER 19-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 SPISGNEXT	U-0 —	U-0 —	R/W-0 FRMERREN	R/W-0 SPIROVEN	R/W-0 SPITUREN	R/W-0 IGNROV	R/W-0 IGNTUR
7:0	R/W-0 AUDEN ⁽¹⁾	U-0 —	U-0 —	U-0 —	R/W-0 AUDMONO ^(1,2)	U-0 —	R/W-0 AUDMOD<1:0> ^(1,2)	R/W-0 —

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit

- 1 = Data from RX FIFO is sign extended
- 0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit

- 1 = Frame Error overflow generates error events
- 0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit

- 1 = Receive overflow generates error events
- 0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit

- 1 = Transmit underrun generates error events
- 0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)

- 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
- 0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)

- 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error that stops SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit⁽¹⁾

- 1 = Audio protocol enabled
- 0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit^(1,2)

- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit^(1,2)

- 11 = PCM/DSP mode
- 10 = Right-Justified mode
- 01 = Left-Justified mode
- 00 = I²S mode

Note 1: This bit can only be written when the ON bit = 0.

Note 2: This bit is only valid for AUDEN = 1.

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REGISTER 22-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	PTEN14	—	—	—	PTEN<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 15-14 **PTEN14:** PMCS1 Address Port Enable bits
1 = PMA14 functions as either PMA14 or PMCS1⁽¹⁾
0 = PMA14 functions as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits
1 = PMA<10:2> function as PMP address lines
0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾
0 = PMA1 and PMA0 pads functions as port I/O

Note 1: The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.
2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

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REGISTER 23-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER (CONTINUED)

- bit 10-9 **RTCCLKSEL<1:0>**: RTCC Clock Select bits
When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.
11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)
- bit 8-7 **RTCOUTSEL<1:0>**: RTCC Output Data Select bits⁽²⁾
11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered
- bit 6 **RTCCLKON**: RTCC Clock Enable Status bit
1 = RTCC Clock is actively running
0 = RTCC Clock is not running
- bit 5-4 **Unimplemented**: Read as '0'
- bit 3 **RTCWREN**: Real-Time Clock Value Registers Write Enable bit⁽³⁾
1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user
- bit 2 **RTCSYNC**: Real-Time Clock Value Registers Read Synchronization bit
1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple
- bit 1 **HALFSEC**: Half-Second Status bit⁽⁴⁾
1 = Second half period of a second
0 = First half period of a second
- bit 0 **RTC OE**: RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is not enabled

- Note 1:** The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

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REGISTER 24-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
	SSRC<2:0>			CLRASAM	—	ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 1 = ADC module is operating
 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation when the device enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss ssss dddd dddd)
 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss ssss dddd dddd)
 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
 111 = Internal counter ends sampling and starts conversion (auto convert)
 110 = Reserved
 101 = Reserved
 100 = Reserved
 011 = CTMU ends sampling and starts conversion
 010 = Timer 3 period match ends sampling and starts conversion
 001 = Active transition on INT0 pin ends sampling and starts conversion
 000 = Clearing SAMP bit ends sampling and starts conversion

- Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
- 3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

26.1 Comparator Voltage Reference Control Register

TABLE 26-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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REGISTER 29-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0, HS DSINT0
7:0	R/W-0, HS DSFLT	U-0 —	U-0 —	R/W-0, HS DSWDT	R/W-0, HS DSRTC	R/W-0, HS DSMCLR	U-0 —	U-0 —

Legend:

R = Readable bit

W = Writable bit

HS = Hardware Set

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit

1 = Interrupt-on-change was asserted during Deep Sleep

0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit

1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted

0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit

1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep

0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit

1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep

0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit

1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep

0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as '0'

Note: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

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29.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 29-2 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 29-2: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
CTMU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Low-Voltage Detect	HLVDM	PMD1<20>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MX1XX 28/44-Pin XLP (General Purpose) Family Features"** and **TABLE 2: "PIC32MX2XX 28/44-Pin XLP (USB) Family Features"** for the lists of available peripherals.

2: The module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

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REGISTER 30-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	—	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	R/P	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	AI2C2	AI2C1	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31 **Reserved:** Write '1'
- bit 30 **FUSBIDIO:** USB USBID Selection bit
 1 = USBID pin is controlled by the USB module
 0 = USBID pin is controlled by the port function
- bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
 1 = Allow only one reconfiguration
 0 = Allow multiple reconfigurations
- bit 28 **PMDI1WAY:** Peripheral Module Disable Configuration bit
 1 = Allow only one reconfiguration
 0 = Allow multiple reconfigurations
- bit 27-24 **Reserved:** Write '1'
- bit 23 **AI2C2:** Alternate I/O Select for I2C2 bit
 1 = I2C2 uses the SDA2/SCL2 pins
 0 = I2C2 uses the ASDA2/ASCL2 pins
- bit 22 **AI2C1:** Alternate I/O Select for I2C1 bit
 1 = I2C1 uses the SDA1/SCL1 pins
 0 = I2C1 uses the ASDA1/ASCL1 pins
- bit 21-16 **Reserved:** Write '1'
- bit 15-0 **USERID<15:0>:** User ID bits
 This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

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TABLE 33-35: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	AVDD	V	(Note 1)
Reference Inputs							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	± 0.001	± 0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 k Ω
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	E _{OFF}	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

- Note 1:** These parameters are not characterized or tested in manufacturing.
2: With no missing codes.
3: These parameters are characterized, but not tested in manufacturing.
4: Characterized with a 1 kHz sine wave.
5: The ADC module is functional at $V_{BORMIN} < V_{DD} < 2.0\text{V}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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TABLE 33-42: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
CTMU CURRENT SOURCE							
CTMUI1	IOUT1	Base Range ⁽¹⁾	—	0.55	—	μA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range ⁽¹⁾	—	5.5	—	μA	CTMUCON<9:8> = 10
CTMUI3	IOUT3	100x Range ⁽¹⁾	—	55	—	μA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range ⁽¹⁾	—	550	—	μA	CTMUCON<9:8> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	—	0.598	—	V	T _A = +25°C, CTMUCON<9:8> = 01
			—	0.658	—	V	T _A = +25°C, CTMUCON<9:8> = 10
			—	0.721	—	V	T _A = +25°C, CTMUCON<9:8> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change ^(1,2)	—	-1.92	—	mV/°C	CTMUCON<9:8> = 01
			—	-1.74	—	mV/°C	CTMUCON<9:8> = 10
			—	-1.56	—	mV/°C	CTMUCON<9:8> = 11

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksp/s
- All PMD bits are cleared (PMDx = 0)
- Executing a `while(1)` statement
- Device operating from the FRC with no PLL

3: The CTMU module is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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NOTES: