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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx274f256b-v-so

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

TABLE 1-7: TIMER1 THROUGH TIMER5 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/TQFP			
Timer1 through Timer5						
T1CK	9	12	34	I	ST	Timer1-5 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	
T3CK	PPS	PPS	PPS	I	ST	
T4CK	PPS	PPS	PPS	I	ST	
T5CK	PPS	PPS	PPS	I	ST	
Real-Time Clock and Calendar						
RTCC	4	7	24	O	ST	Real-Time Clock Alarm Output

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer PPS = Peripheral Pin Select — = N/A

Note 1: Pin numbers are provided for reference only. See the “**Pin Diagrams**” section for device pin availability.

TABLE 1-8: UART1 AND UART2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/TQFP			
Universal Asynchronous Receiver Transmitter 2						
U1CTS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	O	—	UART1 Transmit
Universal Asynchronous Receiver Transmitter 2						
U2CTS	PPS	PPS	PPS	I	ST	UART2 Clear to Send
U2RTS	PPS	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	O	—	UART2 Transmit

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer PPS = Peripheral Pin Select — = N/A

Note 1: Pin numbers are provided for reference only. See the “**Pin Diagrams**” section for device pin availability.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

TABLE 1-11: COMPARATOR 1, COMPARATOR 2, AND COMPARATOR VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Comparator Voltage Reference						
VREF-	28	3	20	I	Analog	Comparator Voltage Reference (Low)
VREF+	27	2	19	I	Analog	Comparator Voltage Reference (High)
CVREFOUT	22	25	14	O	Analog	Comparator Voltage Reference Output
Comparator 1						
C1INA	4	7	24	I	Analog	Comparator 1 Positive Input
C1INB	3	6	23	I	Analog	
C1INC	2	5	22	I	Analog	
C1IND	1	4	21	I	Analog	
C1OUT	PPS	PPS	PPS	O	—	Comparator 1 Output
Comparator 2						
C2INA	2	5	22	I	Analog	Comparator 2 Positive Input
C2INB	1	4	21	I	Analog	
C2INC	4	7	24	I	Analog	
C2IND	3	6	23	I	Analog	
C2OUT	PPS	PPS	PPS	O	—	Comparator 2 Output
Comparator 3						
C3INA	23	26	15	I	Analog	Comparator 3 Positive Input
C3INB	22	25	14	I	Analog	
C3INC	27	2	19	I	Analog	
C3IND	1	4	21	I	Analog	
C3OUT	PPS	PPS	PPS	O	—	Comparator 3 Output

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input
— = N/A

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/44-pin XLP Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “Decoupling Capacitors”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “Decoupling Capacitors”)
- VCAP pin (see 2.3 “Capacitor on Internal Voltage Regulator (VCAP)”)
- MCLR pin (see 2.4 “Master Clear (MCLR) Pin”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 “ICSP Pins”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “External Oscillator Pins”)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 μF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

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Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

TABLE 3-3: MIPS32® M4K® PROCESSOR CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Bp	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see **29.0 “Power-Saving Features”**.

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

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REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCCEN	CRCCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCCAPP bit cannot be set.

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REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

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REGISTER 10-10: CHEHIT: CACHE HIT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEHIT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEHIT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEHIT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEHIT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEHIT<31:0>**: Cache Hit Count bits

Incremented each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

REGISTER 10-11: CHEMIS: CACHE MISS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEMIS<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEMIS<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEMIS<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEMIS<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEMIS<31:0>**: Cache Miss Count bits

Incremented each time the processor issues an instruction fetch from a cacheable region that misses the prefetch cache. Non-cacheable accesses do not modify this value.

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11.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. “USB On-The-Go (OTG)”** (DS60001126), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, Full-Speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB Full-Speed and Low-Speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-Speed support for Host and Device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc., also referred to as USB-IF (www.usb.org). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ^(f)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **12.2 “CLR, SET and INV Registers”** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

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REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
0 = Even/Odd buffer pointers are not Reset
- bit 0 **USBEN:** USB Module Enable bit⁽⁴⁾
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled
- SOFEN:** SOF Enable bit⁽⁵⁾
1 = SOF token is sent every 1 ms
0 = SOF token is disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

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REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 5-4 **TCKPS<1:0>**: Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value
- bit 3 **Unimplemented**: Read as '0'
- bit 2 **TSYNC**: Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.
- bit 1 **TCS**: Timer Clock Source Select bit
1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock
- bit 0 **Unimplemented**: Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

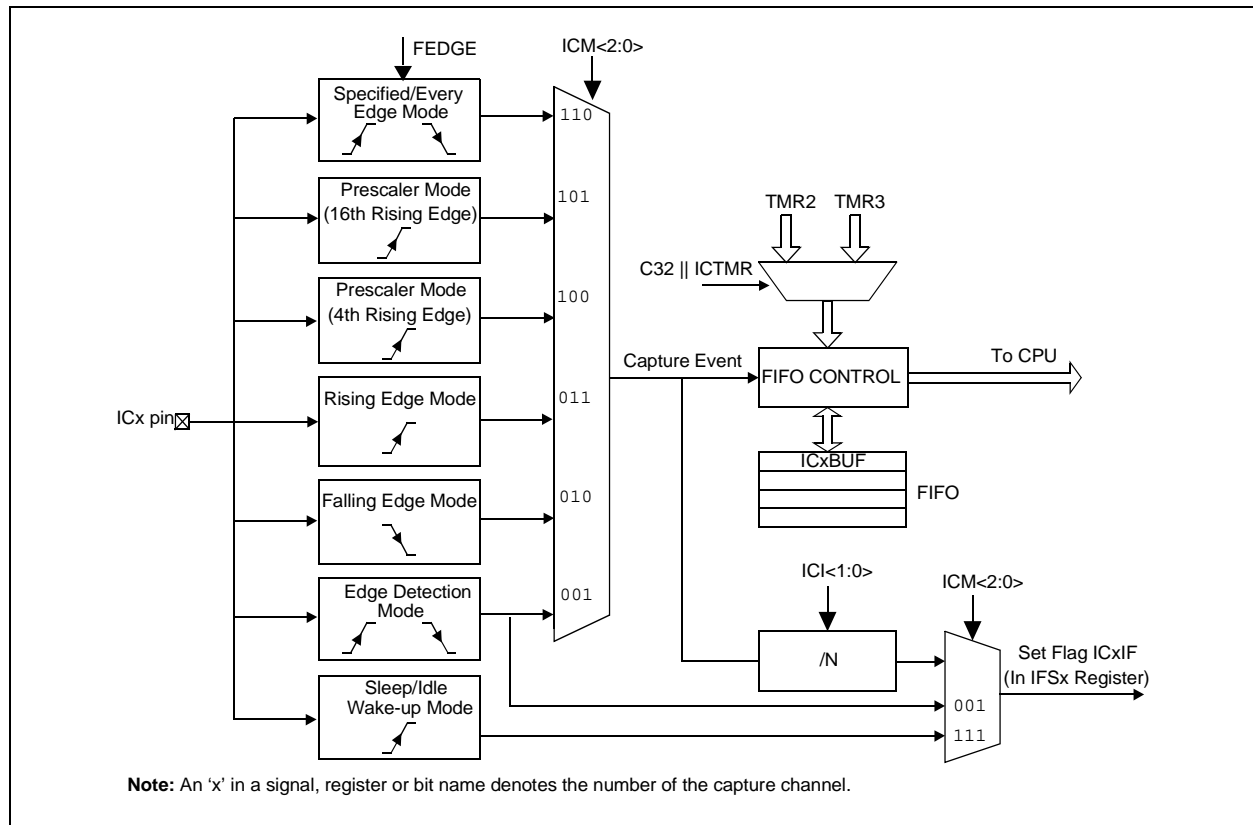
Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 17-1 illustrates a general block diagram of the Input Capture module.

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 **SPIFE**: Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF**: Enhanced Buffer Enable bit⁽²⁾
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled
- bit 15 **ON**: SPI Peripheral On bit⁽¹⁾
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled
- bit 14 **Unimplemented**: Read as '0'
- bit 13 **SIDL**: Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
- bit 12 **DISSDO**: Disable SDOx pin bit
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

- bit 11-10 **MODE<32,16>**: 32/16-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

- bit 9 **SMP**: SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

To write a '1' to this bit, the MSTEN value = 1 must first be written.

- bit 8 **CKE**: SPI Clock Edge Select bit⁽³⁾
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)
- bit 7 **SSEN**: Slave Select Enable (Slave mode) bit
1 = \overline{SSx} pin used for Slave mode
0 = \overline{SSx} pin not used for Slave mode, pin controlled by port function.
- bit 6 **CKP**: Clock Polarity Select bit⁽⁴⁾
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 20-1: I2CxCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	R/W-1, HC SCLREL	R/W-0 STRICT	R/W-0 A10M	R/W-0 DISSLW	R/W-0 SMEN
7:0	R/W-0 GCEN	R/W-0 STREN	R/W-0 ACKDT	R/W-0, HC ACKEN	R/W-0, HC RCEN	R/W-0, HC PEN	R/W-0, HC RSEN	R/W-0, HC SEN

Legend:	HC = Cleared in Hardware
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I²C Enable bit⁽¹⁾

- 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit

- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit

- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

- 1 = Slew rate control disabled
- 0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

NOTES:

21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

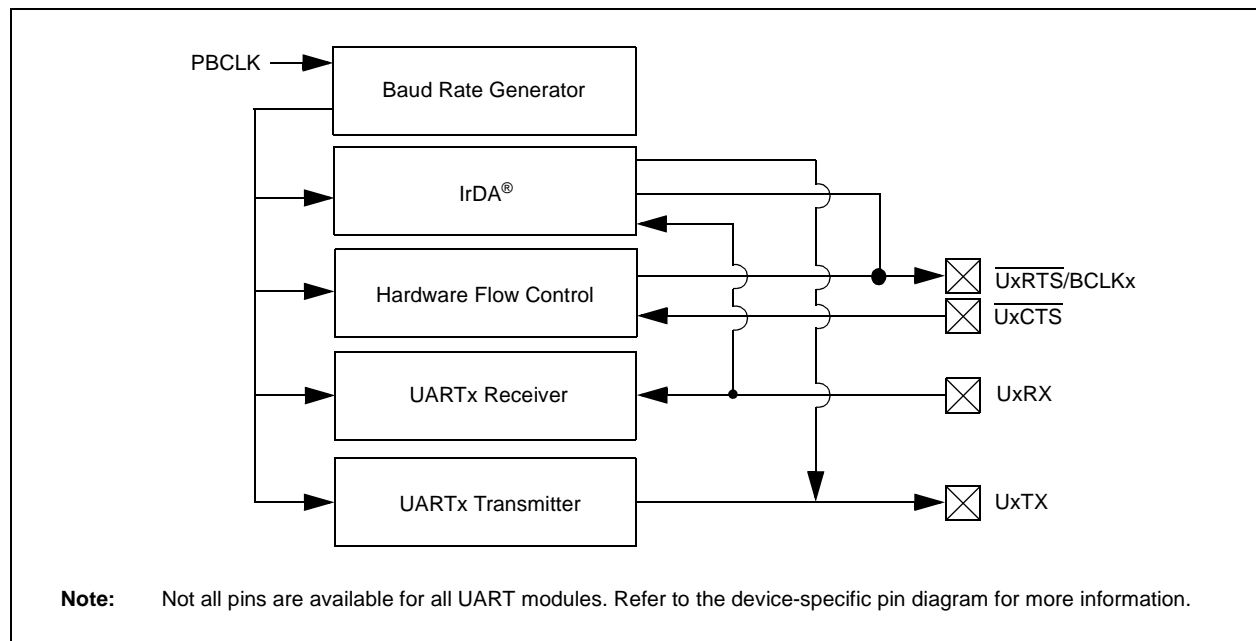
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/44-pin XLP Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The UART module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The following are key features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 33.4 bps to 17.5 Mbps at 72 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support
- Auto-baud support
- Ability to receive data during Sleep mode

Figure 21-1 illustrates a simplified block diagram of the UART module.

FIGURE 21-1: UART SIMPLIFIED BLOCK DIAGRAM



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 23-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 30-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

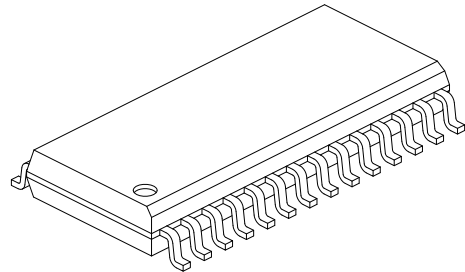
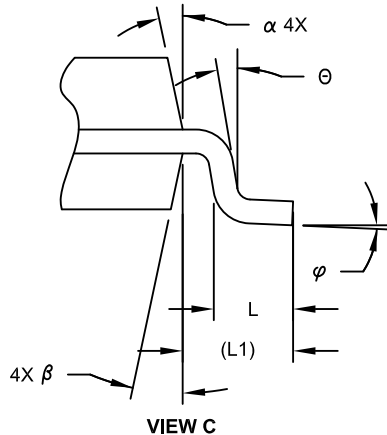
- bit 23 **DSBOREN**: Deep Sleep BOR Enable bit
1 = Enable BOR during Deep Sleep mode
0 = Disable BOR during Deep Sleep mode
- bit 22 **Reserved**: Write '1'
- bit 21 **VBATBOREN**: VBAT BOR Enable bit
1 = Enable BOR during VBAT mode
0 = Disable BOR during VBAT mode
- bit 20 **BOREN**: Brown-Out Reset (BOR) Enable bit
1 = Enable BOR
0 = Disable BOR
- bit 19 **Reserved**: Write '1'
- bit 18-16 **FPLLODIV<2:0>**: Default PLL Output Divisor bits
111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1
- bit 15 **UPLLEN**: USB PLL Enable bit⁽¹⁾
1 = Disable and bypass USB PLL
0 = Enable USB PLL
- bit 14-11 **Reserved**: Write '1'
- bit 10-8 **UPLLDIV<2:0>**: USB PLL Input Divider bits⁽¹⁾
111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider
- bit 7 **FPLLICK**: System PLL Input Clock Select bit
1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL
- bit 6-4 **FPLLMUL<2:0>**: PLL Multiplier bits
111 = 24x multiplier
110 = 21x multiplier
101 = 20x multiplier
100 = 19x multiplier
011 = 18x multiplier
010 = 17x multiplier
001 = 16x multiplier
000 = 15x multiplier
- bit 3 **Reserved**: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

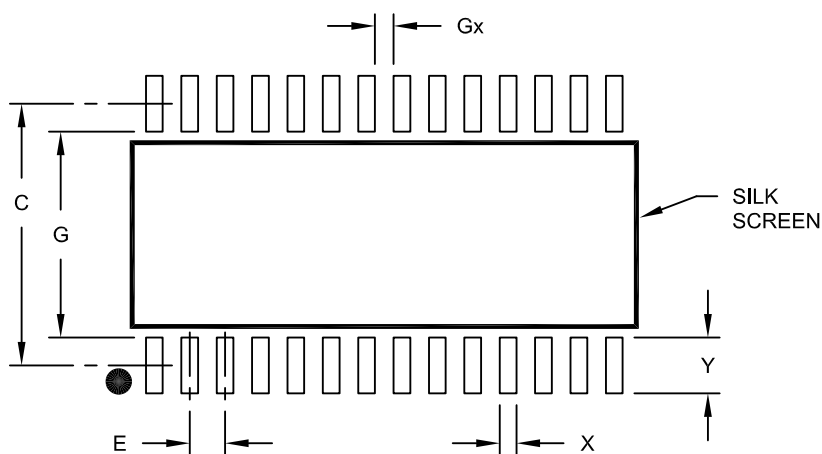
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A