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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx274f256dt-i-ml

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-0
	—	—	—	—	—	BMX CHEDMA	—	—
23:16	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
	—	BMX WSDRM	—	—	—	BMXARB<2:0>		

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **BMXCHEDMA:** BMX PFM Cacheability for DMA Access bit

- 1 = Enable Program Flash memory (data) cacheability for DMA accesses (requires cache to have data caching enabled)
- 0 = Disable program Flash memory (data) cacheability for DMA accesses (hits are still read from the cache, but misses do not update the cache)

bit 25-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit

- 1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
- 0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit

- 1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
- 0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit

- 1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
- 0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)

- 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
- 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)

- 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
- 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit

- 1 = Data RAM accesses from CPU have one wait state for address setup
- 0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits

- 111 = Reserved (using these Configuration modes will produce undefined behavior)
- .
- .
- 011 = Reserved (using these Configuration modes will produce undefined behavior)
- 010 = Arbitration Mode 2
- 001 = Arbitration Mode 1 (default)
- 000 = Arbitration Mode 0

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REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0 CHSPTR<15:8>							
7:0	R-0 CHSPTR<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
 bit 15-0 **CHSPTR<15:0>**: Channel Source Pointer bits
 1111111111111111 = Points to byte 65,535 of the source
 .
 .
 .
 0000000000000001 = Points to byte 1 of the source
 0000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0 CHDPTR<15:8>							
7:0	R-0 CHDPTR<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
 bit 15-0 **CHDPTR<15:0>**: Channel Destination Pointer bits
 1111111111111111 = Points to byte 65,535 of the destination
 .
 .
 .
 0000000000000001 = Points to byte 1 of the destination
 0000000000000000 = Points to byte 0 of the destination

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REGISTER 10-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-0 **CHEPFABT<31:0>**: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

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REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE ⁽¹⁾	URSTIE ⁽²⁾
								DETACHIE ⁽³⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit

1 = STALL interrupt is enabled
0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit

1 = ATTACH interrupt is enabled
0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit

1 = RESUME interrupt is enabled
0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit

1 = Idle interrupt is enabled
0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit

1 = TRNIF interrupt is enabled
0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit

1 = SOFIF interrupt is enabled
0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit⁽¹⁾

1 = USB Error interrupt is enabled
0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit⁽²⁾

1 = URSTIF interrupt is enabled
0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit⁽³⁾

1 = DATTCHIF interrupt is enabled
0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.

2: Device mode.

3: Host mode.

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REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit⁽¹⁾
 1 = Timer is enabled
 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when the device enters Idle mode
 0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
 1 = Writes to Timer1 are ignored until pending write operation completes
 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
 1 = Asynchronous write to the Timer1 register in progress
 0 = Asynchronous write to Timer1 register is complete
In Synchronous Timer mode:
 This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
 11 = Reserved
 10 = External clock comes from the LPRC
 01 = External clock comes from the T1CK pin
 00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
 This bit is ignored.
When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

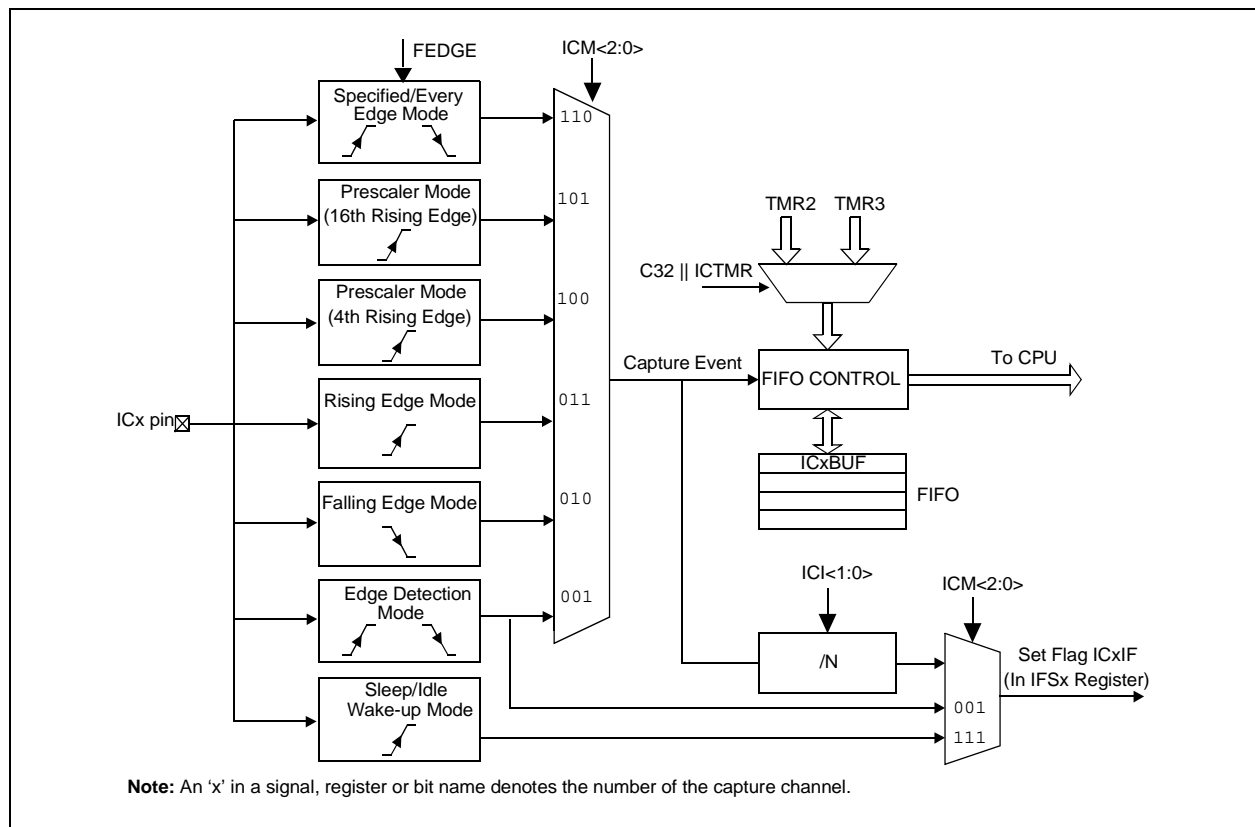
Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 17-1 illustrates a general block diagram of the Input Capture module.

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

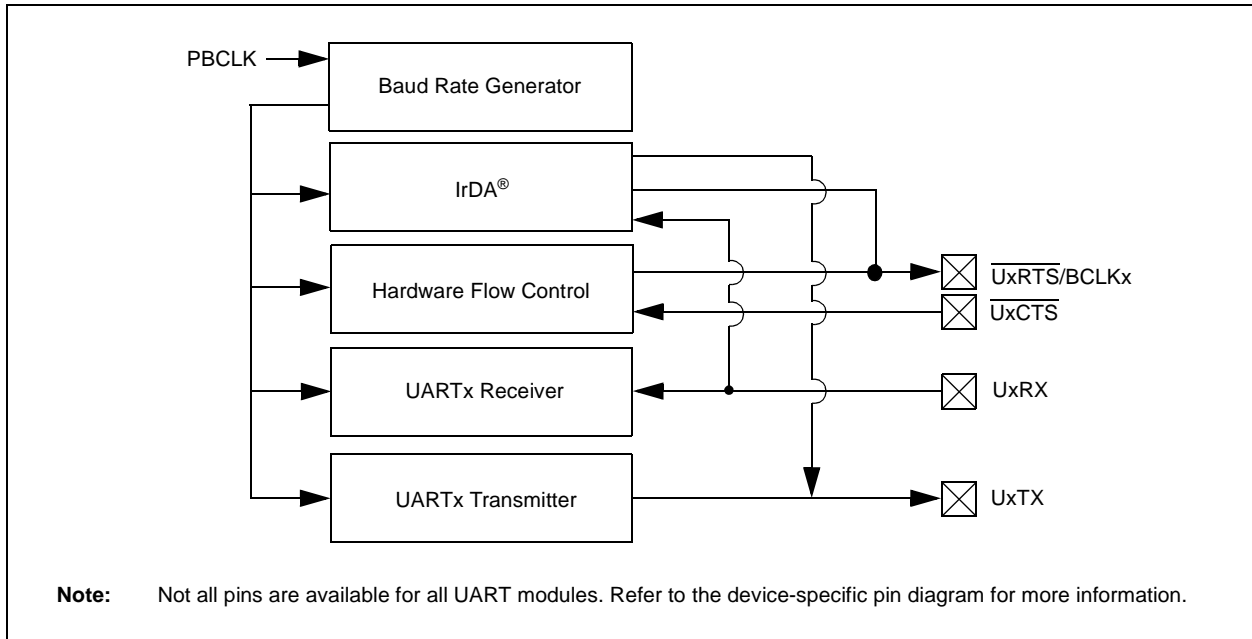
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/44-pin XLP Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The UART module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The following are key features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 33.4 bps to 17.5 Mbps at 72 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support
- Auto-baud support
- Ability to receive data during Sleep mode

Figure 21-1 illustrates a simplified block diagram of the UART module.

FIGURE 21-1: UART SIMPLIFIED BLOCK DIAGRAM



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 10 **UTXEN:** Transmit Enable bit
1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset
- Note:** The event of disabling an enabled transmitter will release the TX pin to the PORT function and reset the transmit buffers to empty. Any pending transmission is aborted and data characters in the transmit buffers are lost. All transmit status flags are cleared and the TRMT bit is set
- bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

Figure 21-2 and Figure 21-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 21-2: UART RECEPTION

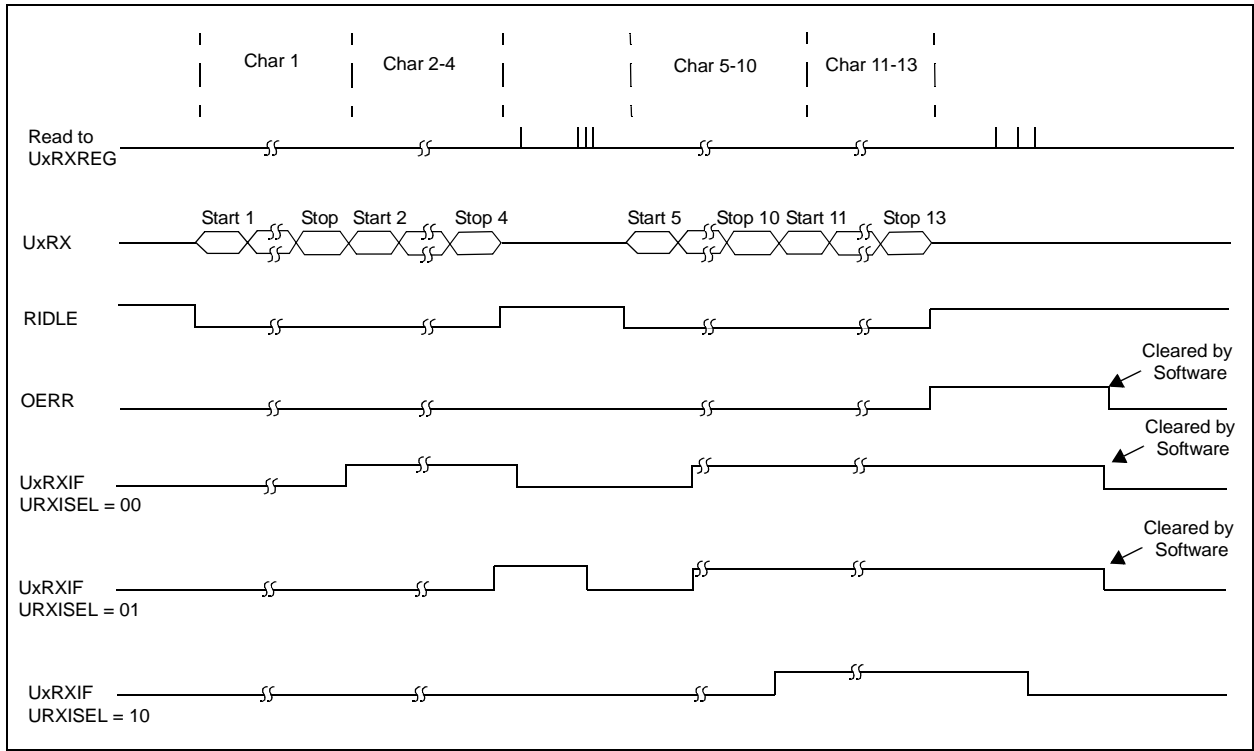
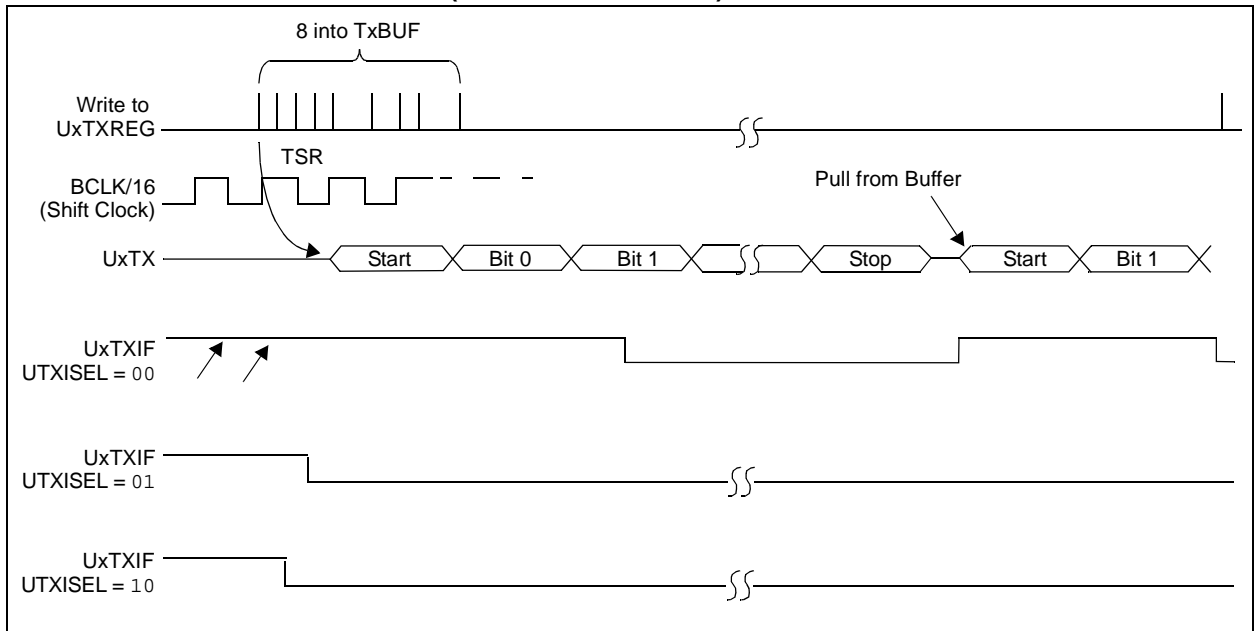


FIGURE 21-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 25-1: CMXCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COOUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-16 **Unimplemented:** Read as '0'
- bit 15 **ON:** Comparator ON bit⁽¹⁾
 - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
 - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
 - 1 = Comparator output is driven on the output CxOUT pin
 - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾
 - 1 = Output is inverted
 - 0 = Output is not inverted
- bit 12-9 **Unimplemented:** Read as '0'
- bit 8 **COOUT:** Comparator Output bit
 - 1 = Output of the Comparator is a '1'
 - 0 = Output of the Comparator is a '0'
- bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
 - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
 - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
 - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
 - 00 = Comparator interrupt generation is disabled
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **CREF:** Comparator Positive Input Configure bit
 - 1 = Comparator non-inverting input is connected to the internal CVREF
 - 0 = Comparator non-inverting input is connected to the CxINA pin
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
 - 11 = Comparator inverting input is connected to the IVREF
 - 10 = Comparator inverting input is connected to the CxIND pin
 - 01 = Comparator inverting input is connected to the CxINC pin
 - 00 = Comparator inverting input is connected to the CxINB pin

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

28.1 CTMU Control Registers

TABLE 28-1: CTMU REGISTER MAP

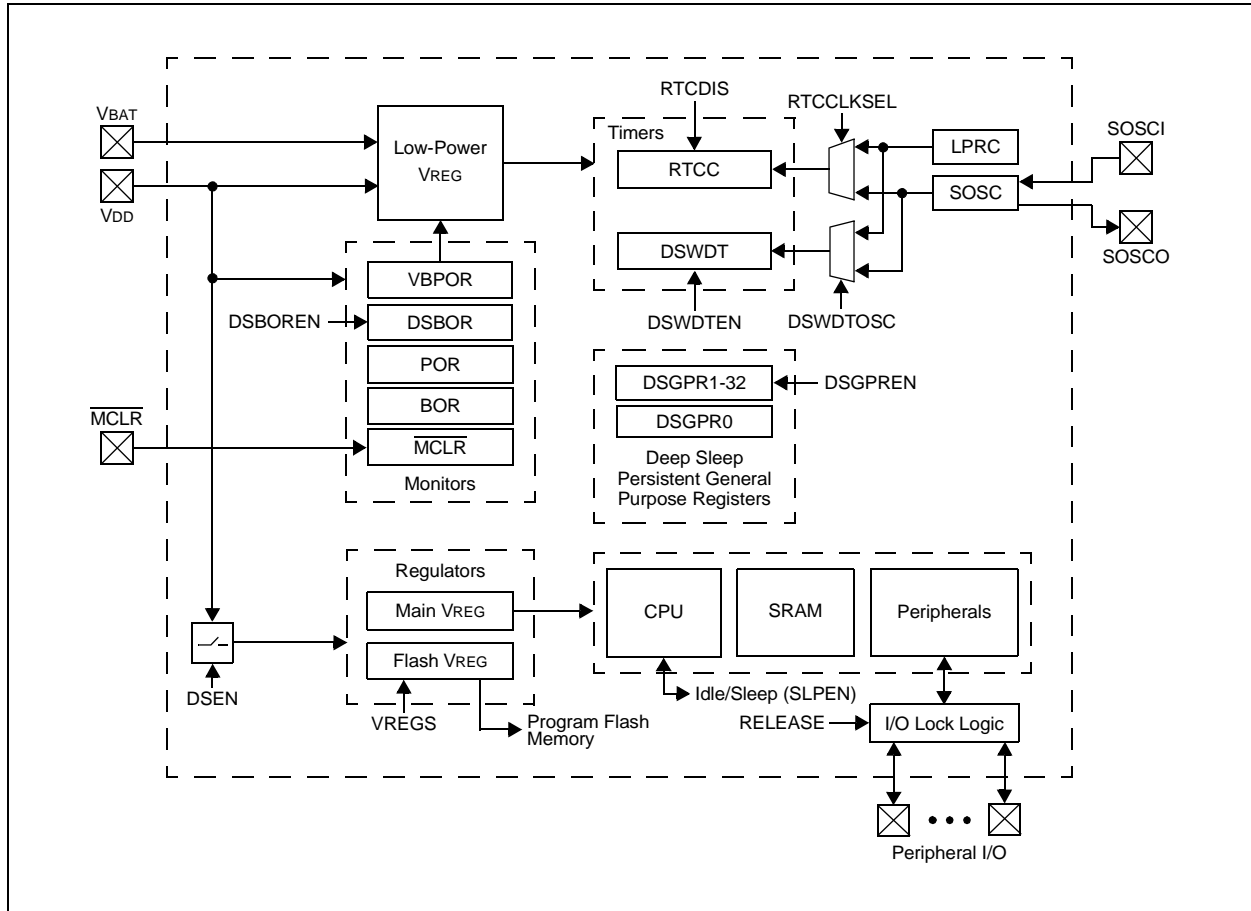
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits														All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	
A200	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>			EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>			—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>			IRNG<1:0>		0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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FIGURE 29-1: XLP DEVICE BLOCK DIAGRAM



PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 30-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOfNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit

- 1 = Watchdog Timer stops during Flash programming
- 0 = Watchdog Timer runs during Flash programming

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

- 10100 = 1:1048576
 - 10011 = 1:524288
 - 10010 = 1:262144
 - 10001 = 1:131072
 - 10000 = 1:65536
 - 01111 = 1:32768
 - 01110 = 1:16384
 - 01101 = 1:8192
 - 01100 = 1:4096
 - 01011 = 1:2048
 - 01010 = 1:1024
 - 01001 = 1:512
 - 01000 = 1:256
 - 00111 = 1:128
 - 00110 = 1:64
 - 00101 = 1:32
 - 00100 = 1:16
 - 00011 = 1:8
 - 00010 = 1:4
 - 00001 = 1:2
 - 00000 = 1:1
- All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

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32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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TABLE 33-9: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp		
Param. No.	Typical ⁽²⁾	Maximum	Units	Conditions	
Power-Down Current (IPD) (Note 1)					
DC40k	—	—	μA	-40°C	Sleep (Note 1)
DC40l	25	42	μA	+25°C	
DC40m	240	390	μA	+85°C	
DC40n	—	—	μA	+105°C	
DC41k	—	—	nA	-40°C	Deep Sleep (Note 5)
DC41l	673	800	nA	+25°C	
DC41m	—	—	nA	+85°C	
DC41n	—	—	nA	+105°C	
DC42k	—	—	nA	-40°C	VBAT (Note 6)
DC42l	—	—	nA	+25°C	
DC42m	—	—	nA	+85°C	
DC42n	—	—	nA	+105°C	
Module Differential Current					
DC44a	5	—	μA	3.6V	Watchdog Timer Current: ΔI _{WDT} (Note 3)
DC44b	23	—	μA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} + ΔI _{TMR} (Note 3)
DC44c	1000	—	mA	3.6V	ADC Current: ΔI _{ADC} (Notes 3, 4)
DC44d	15	—	μA	3.6V	Deadman Timer Current: ΔI _{DMT}
DC44e	0.71	—	μA	3.6V	Deep Sleep Watchdog Timer Current: ΔI _{DSWDT} (Note 3)
DC44f	0.8	—	μA	3.6V	RTCC Current: ΔI _{RTCC} (Note 3)

Note 1: The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
 - CPU is in Sleep mode
 - L1 Cache and Prefetch modules are disabled
 - No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
 - WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
 - Voltage regulator is in Stand-by mode (VREGS = 0; IOANCPEN = 0)
- 2:** Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Voltage regulator is operational (VREGS = 1).
- 5:** The test conditions for Deep Sleep mode current measurements are as follows:
- All I/O pins are configured as inputs and pulled to V_{SS}
 - DSBORN, DSWDTEN, and DGPREN are set to ‘0’ and RTCDIS is set to ‘1’
- 6:** The test conditions for VBAT mode current measurements is as follows:
- VBATBORN is set to ‘0’

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TABLE 33-14: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	-10	—	+10	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	70	—	—	dB	Max VICM = (VDD - 1)V (Note 2)
D303A	TRESP	Large Signal Response Time	—	100	80	ns	AVDD = VDD, AVSS = VSS (Note 1,2)
D303B	TSRESP	Small Signal Response Time	—	50	160	ns	This is defined as an input step of 50 mV with 15 mV of overdrive (Note 2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	110	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.16	1.2	1.24	V	—
D312	TSET	Internal Comparator Voltage DRC Reference Setting time	—	—	1	μs	(Note 3)

- Note 1:** Response time measured with one comparator input at $(VDD - 1.5)/2$, while the other input transitions from VSS to VDD.
- 2:** These parameters are characterized but not tested.
- 3:** Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.
- 4:** The Comparator module is functional at $V_{BORMIN} < VDD < VDDMIN$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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TABLE 33-25: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
TB10	TtXH	TxCK High Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter TB15
TB11	TtXL	TxCK Low Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter TB15
TB15	TtXP	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } [(25 \text{ ns or } 2 \text{ TPB})/N] + 30 \text{ ns})]$	—	ns	$V_{DD} > 2.7\text{V}$
				$[(\text{Greater of } [(25 \text{ ns or } 2 \text{ TPB})/N] + 50 \text{ ns})]$	—	ns	$V_{DD} < 2.7\text{V}$
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 33-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS

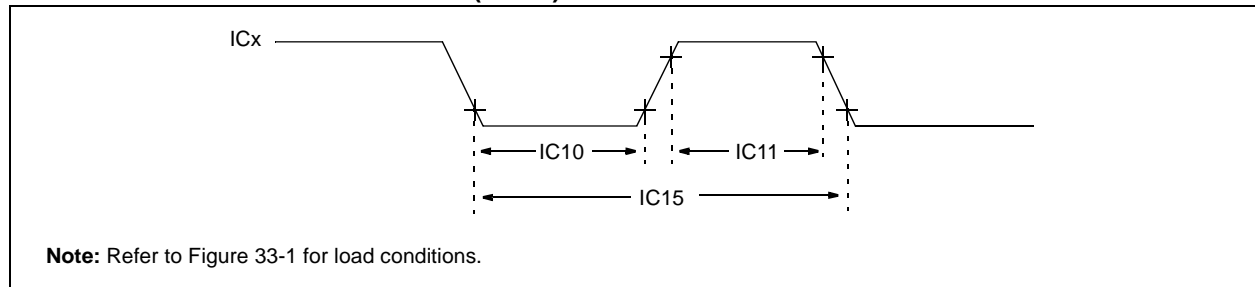


TABLE 33-26: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
IC10	TcCL	ICx Input Low Time		$[(12.5 \text{ ns or } 1 \text{ TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter IC15.
IC11	TcCH	ICx Input High Time		$[(12.5 \text{ ns or } 1 \text{ TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter IC15.
IC15	TcCP	ICx Input Period		$[(25 \text{ ns or } 2 \text{ TPB})/N] + 50 \text{ ns}$	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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TABLE 33-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 \text{ CB}$	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 \text{ CB}$	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	ns	—
			400 kHz mode	$TPB * (BRG + 2)$	—	ns	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	ns	

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

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TABLE 33-35: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	AVDD	V	(Note 1)
Reference Inputs							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	± 0.001	± 0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 k Ω
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	E _{OFF}	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

- Note 1:** These parameters are not characterized or tested in manufacturing.
2: With no missing codes.
3: These parameters are characterized, but not tested in manufacturing.
4: Characterized with a 1 kHz sine wave.
5: The ADC module is functional at $V_{BORMIN} < V_{DD} < 2.0\text{V}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 34-3: TYPICAL IPD CURRENT @ VDD = 3.3V

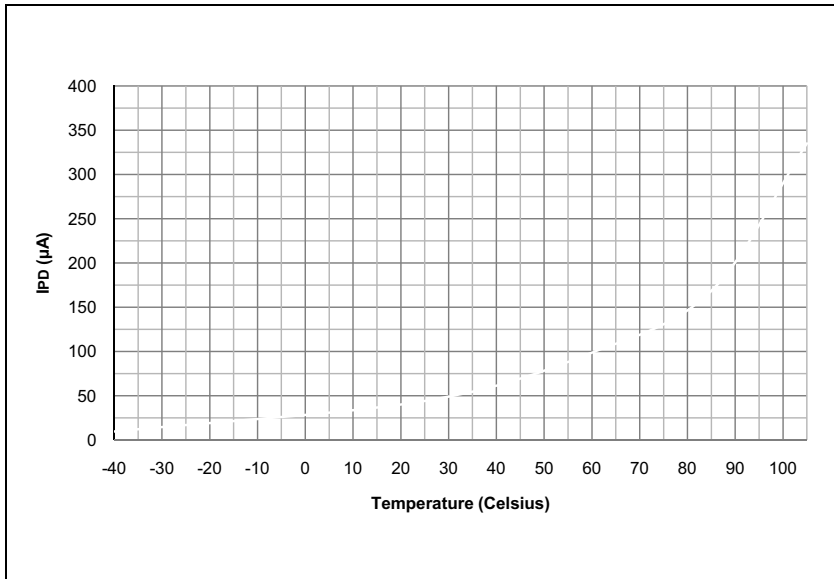


FIGURE 34-5: TYPICAL I_{IDLE} CURRENT @ VDD = 3.3V

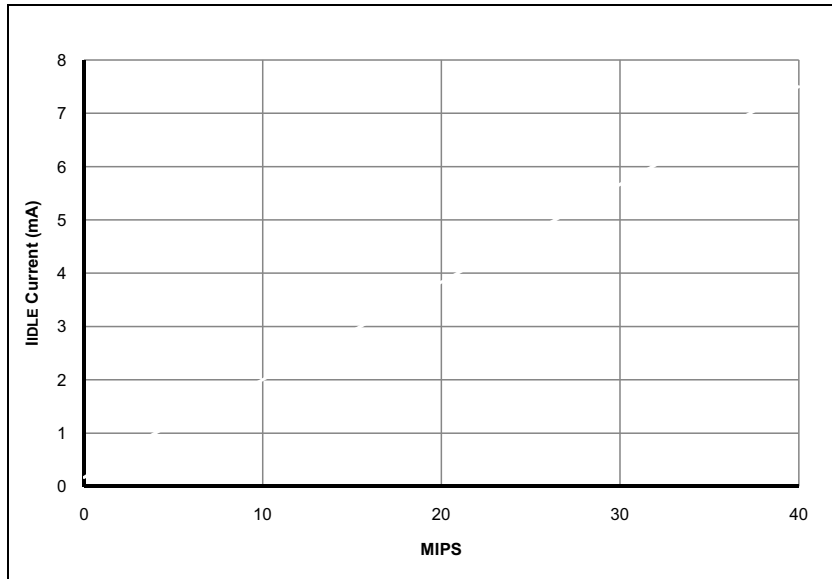


FIGURE 34-4: TYPICAL I_{DD} CURRENT @ VDD = 3.3V

