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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx274f256dt-v-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx274f256dt-v-pt</a>

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

**TABLE 7: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITH VBAT**

<b>28-PIN QFN (TOP VIEW)<sup>(1,2,3,4)</sup></b>  <b>PIC32MX155F128D</b> <b>PIC32MX175F256D</b>		28	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1	16	Vss
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/RB3	18	PGED1/RPB10/CTED11/PMD2/RB10
5	Vss	19	PGEC1/TMS/RPB11/PMD1/RB11
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12
7	OSC2/CLKO/RPA3/PMA0/RA3	21	VBAT
8	SOSCI/RPB4/RB4 <sup>(5)</sup>	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
9	SOSCO/RPA4/T1CK/CTED9/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	PGED3/RPB5/ASDA2/PMD7/RB5	25	AVDD
12	PGEC3/RPB6/ASCL2/PMD6/RB6	26	$\overline{\text{MCLR}}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/AN0/C3INC/RPA0ASDA1//CTED1/PMA1/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/AN1/RPA1/ASCL1/CTED2/PMRD/RA1

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 “Peripheral Pin Select” for restrictions.
  - 2: Every I/O port pin (RAX-RBx) can be used as a change notification pin (CNAX-CNBx). See 12.0 “I/O Ports” for more information.
  - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
  - 4: Shaded pins are 5V tolerant.
  - 5: This is an input-only pin.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

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## Referenced Sources

This device data sheet is based on the following individual chapters of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: <http://www.microchip.com/pic32>

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 4. “Prefetch Cache”** (DS60001119)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (C<sub>VREF</sub>)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167)
- **Section 38. “High/Low Voltage Detect (HLVD)”** (*DS number pending*)

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

## 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

### 2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/44-pin XLP Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “Decoupling Capacitors”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “Decoupling Capacitors”)
- VCAP pin (see 2.3 “Capacitor on Internal Voltage Regulator (VCAP)”)
- MCLR pin (see 2.4 “Master Clear (MCLR) Pin”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 “ICSP Pins”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “External Oscillator Pins”)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

### 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1  $\mu\text{F}$  (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu\text{F}$  to 0.001  $\mu\text{F}$ . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1  $\mu\text{F}$  in parallel with 0.001  $\mu\text{F}$ .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 3. “Memory Organization”** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

PIC32MX1XX/2XX 28/44-pin XLP Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/44-pin XLP Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate Boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

## 4.1 PIC32MX1XX/2XX 28/44-pin XLP Family Memory Layout

PIC32MX1XX/2XX 28/44-pin XLP Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/44-pin XLP Family devices are illustrated in Figure 4-1 and Figure 4-2.

Table 4-1 provides SFR memory map details.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

**TABLE 4-1: SFR MEMORY MAP**

Peripheral	Virtual Address	
	Base	Offset Start
Deep Sleep Controller	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1 and I2C2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator, Reset		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Watchdog Timer		0xF600
PPS		0xFA00
HLVD		0xFC00
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch		0x4000
USB		0x5000
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x2FF0

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

## REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
BMXDRMSZ<31:24>								
23:16	R	R	R	R	R	R	R	R
BMXDRMSZ<23:16>								
15:8	R	R	R	R	R	R	R	R
BMXDRMSZ<15:8>								
7:0	R	R	R	R	R	R	R	R
BMXDRMSZ<7:0>								

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>**: Data RAM Memory (DRM) Size bits  
 Static value that indicates the size of the Data RAM in bytes:  
 0x00008000 = Device has 32 KB RAM  
 0x00010000 = Device has 64 KB RAM

## REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—								
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—								
BMXPUPBA<19:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
BMXPUPBA<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
BMXPUPBA<7:0>								

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-20 **Unimplemented**: Read as '0'  
 bit 19-11 **BMXPUPBA<19:11>**: Program Flash (PFM) User Program Base Address bits  
 bit 10-0 **BMXPUPBA<10:0>**: Read-Only bits  
 This value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.  
**2:** The value in this register must be less than or equal to BMXPFMSZ.

**TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>															0000	
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<7:0>															0000	
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	—
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00FF
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	—	FF00
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16	CHSSA<31:0>															0000	
		15:0																0000	
32E0	DCH3DSA	31:16	CHDSA<31:0>															0000	
		15:0																0000	
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>															0000	
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>															0000	
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>															0000	
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>															0000	
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>															0000	
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>															0000	
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<7:0>															0000	

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.



# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

## REGISTER 10-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<7:0>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-0 **CHEPFABT<31:0>**: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

**REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON <sup>(1)</sup>	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit<sup>(1)</sup>  
 1 = Timer is enabled  
 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit  
 1 = Discontinue module operation when the device enters Idle mode  
 0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit  
 1 = Writes to Timer1 are ignored until pending write operation completes  
 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit  
In Asynchronous Timer mode:  
 1 = Asynchronous write to the Timer1 register in progress  
 0 = Asynchronous write to Timer1 register is complete  
In Synchronous Timer mode:  
 This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits  
 11 = Reserved  
 10 = External clock comes from the LPRC  
 01 = External clock comes from the T1CK pin  
 00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit  
When TCS = 1:  
 This bit is ignored.  
When TCS = 0:  
 1 = Gated time accumulation is enabled  
 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

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## REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 5-4 **TCKPS<1:0>**: Timer Input Clock Prescale Select bits  
11 = 1:256 prescale value  
10 = 1:64 prescale value  
01 = 1:8 prescale value  
00 = 1:1 prescale value
- bit 3 **Unimplemented**: Read as '0'
- bit 2 **TSYNC**: Timer External Clock Input Synchronization Selection bit  
When TCS = 1:  
1 = External clock input is synchronized  
0 = External clock input is not synchronized  
When TCS = 0:  
This bit is ignored.
- bit 1 **TCS**: Timer Clock Source Select bit  
1 = External clock is defined by the TECS<1:0> bits  
0 = Internal peripheral clock
- bit 0 **Unimplemented**: Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.



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## REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 10 **UTXEN:** Transmit Enable bit  
1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)  
0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset
- Note:** The event of disabling an enabled transmitter will release the TX pin to the PORT function and reset the transmit buffers to empty. Any pending transmission is aborted and data characters in the transmit buffers are lost. All transmit status flags are cleared and the TRMT bit is set
- bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)  
1 = Transmit buffer is full  
0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)  
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)  
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit  
11 = Reserved  
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full  
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full  
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)  
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect  
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)  
1 = Receiver is Idle  
0 = Data is being received
- bit 3 **PERR:** Parity Error Status bit (read-only)  
1 = Parity error has been detected for the current character  
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)  
1 = Framing error has been detected for the current character  
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit.  
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.  
1 = Receive buffer has overflowed  
0 = Receive buffer has not overflowed
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)  
1 = Receive buffer has data, at least one more character can be read  
0 = Receive buffer is empty

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## REGISTER 22-2: PPMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits<sup>(1)</sup>

- 11 = Wait of 4 TPB
- 10 = Wait of 3 TPB
- 01 = Wait of 2 TPB
- 00 = Wait of 1 TPB (default)

For Read operations:

- 11 = Wait of 3 TPB
- 10 = Wait of 2 TPB
- 01 = Wait of 1 TPB
- 00 = Wait of 0 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

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**REGISTER 22-6: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	R/W-0 WCS1	U-0 —	U-0 —	U-0 —	R/W-0 —	R/W-0 —	R/W-0 —
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WADDR<7:0>								

**Legend:**

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **WCS1:** Chip Select 1 bit  
1 = Chip Select 1 is active  
0 = Chip Select 1 is inactive

bit 14-11 **Unimplemented:** Read as '0'

bit 10-0 **WADDR<10:0>:** Address bits

**Note:** This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.



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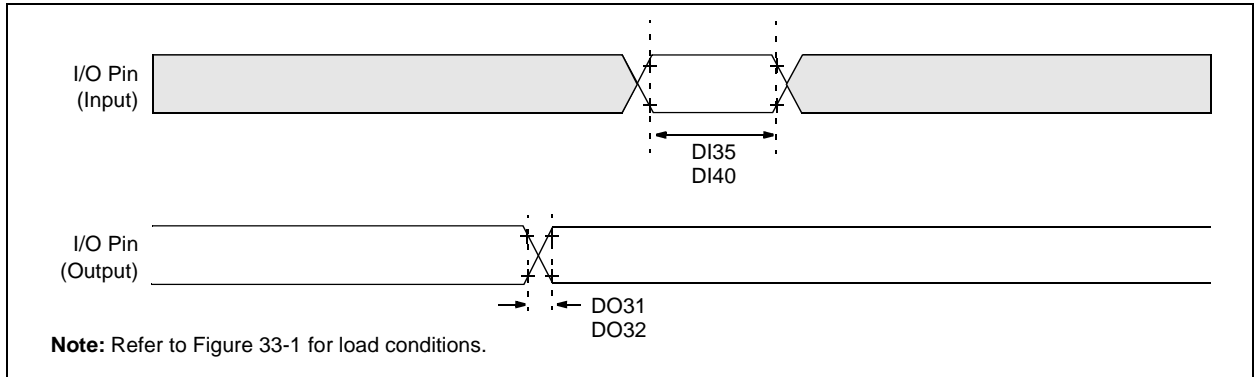
**TABLE 33-6: LOW-VOLTAGE DETECT CHARACTERISTICS**

DC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp						
Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
HLV10	VHLVD	HLVD Voltage on VDD Transition	LVDL<3:0> = 0100 <sup>(1)</sup>	—	3.59	—	V	—
			LVDL<3:0> = 0101	—	3.44	—	V	—
			LVDL<3:0> = 0110	—	3.13	—	V	—
			LVDL<3:0> = 0111	—	2.92	—	V	—
			LVDL<3:0> = 1000	—	2.81	—	V	—
			LVDL<3:0> = 1001	—	2.60	—	V	—
			LVDL<3:0> = 1010	—	2.50	—	V	—
HLV11	VHTHL	HLVD Voltage on HLVDIN Pin Transition	LVDL<3:0> = 1111	—	1.20	—	V	—

**Note 1:** Trip points for values of HLVD<3:0>, from '0000' to '0011' and '1001' to '1110' are not implemented.

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**FIGURE 33-3: I/O TIMING CHARACTERISTICS**



**TABLE 33-22: I/O TIMING REQUIREMENTS**

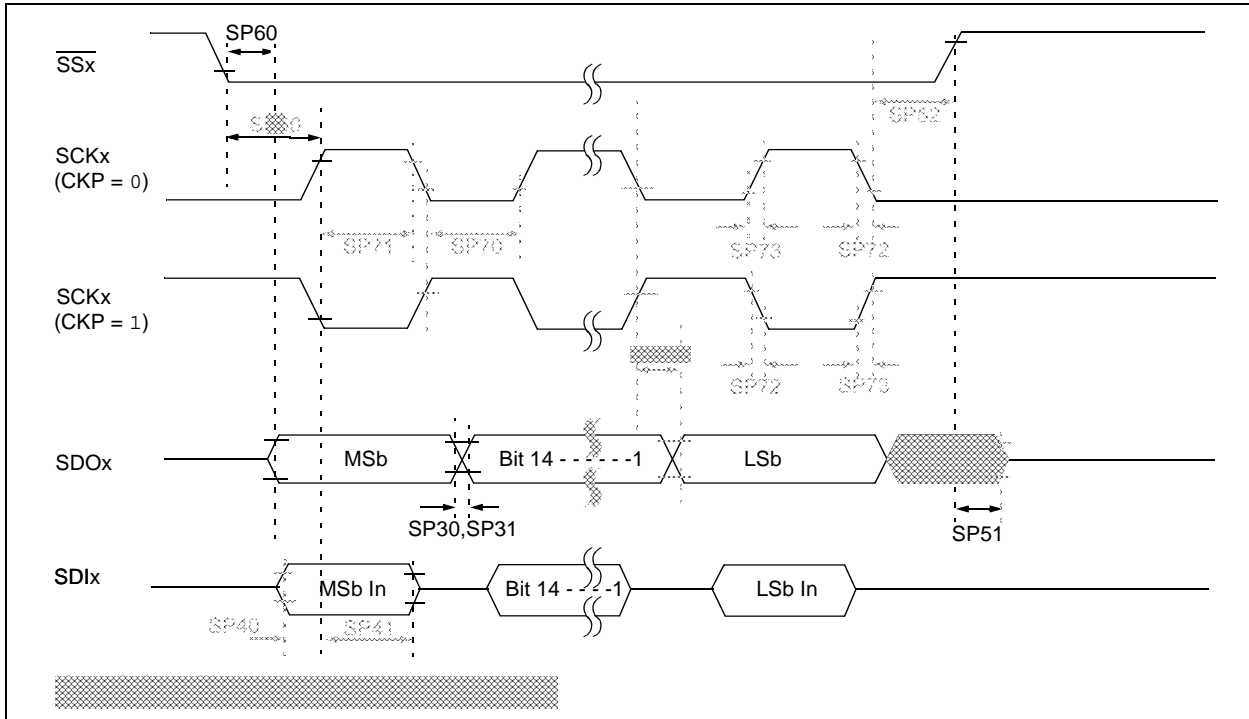
AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics <sup>(2)</sup>	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	15	ns	V <sub>DD</sub> < 2.0V
			—	5	10	ns	V <sub>DD</sub> > 2.0V
DO32	TioF	Port Output Fall Time	—	5	15	ns	V <sub>DD</sub> < 2.0V
			—	5	10	ns	V <sub>DD</sub> > 2.0V
DI35	TINP	INTx Pin High or Low Time	20	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	10	—	T <sub>SYSCLOCK</sub>	—

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**Note 2:** This parameter is characterized, but not tested in manufacturing.

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**FIGURE 33-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**



**TABLE 33-32: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time ( <b>Note 3</b> )	Tsck/2	—	—	ns	—
SP71	Tsch	SCKx Input High Time ( <b>Note 3</b> )	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	Tssl2sch, Tssl2scL	SSx ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**Note 3:** The minimum clock period for SCKx is 50 ns.

**Note 4:** Assumes 50 pF load on all SPIx pins.

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**TABLE 33-35: ADC MODULE SPECIFICATIONS**

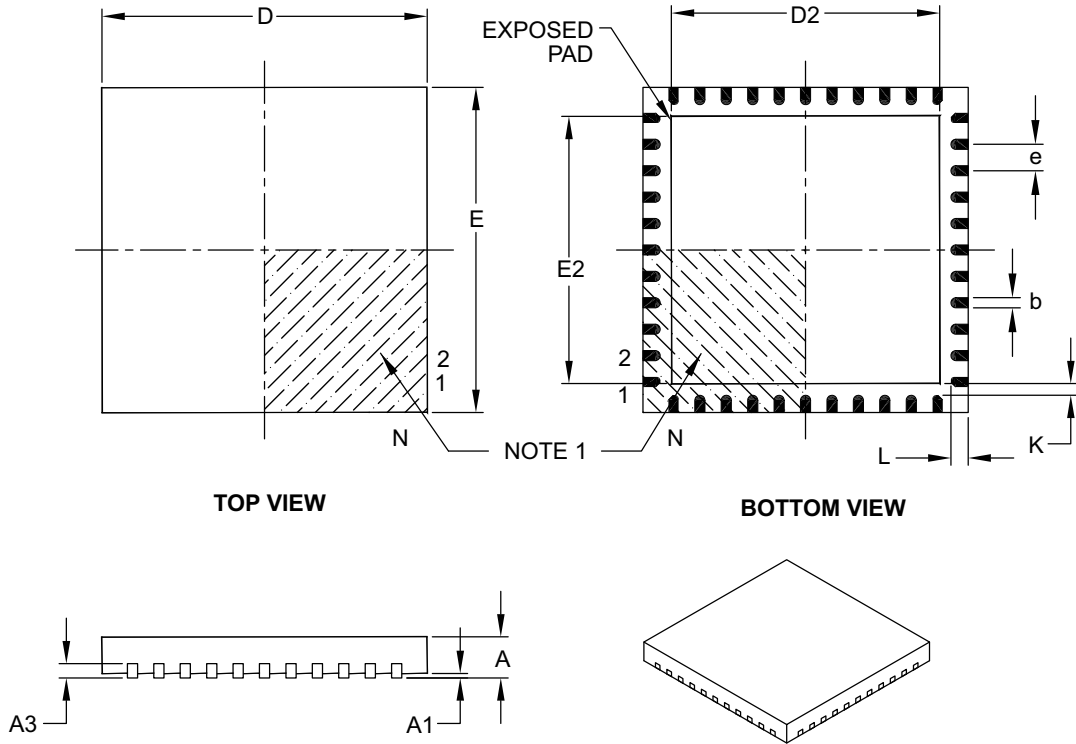
AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
<b>Device Supply</b>							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	VSS	—	AVDD	V	(Note 1)
<b>Reference Inputs</b>							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	$\mu\text{A}$ $\mu\text{A}$	ADC operating ADC off
<b>Analog Input</b>							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	$\pm 0.001$	$\pm 0.610$	$\mu\text{A}$	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 k $\Omega$
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	$\Omega$	(Note 1)
<b>ADC Accuracy – Measurements with External VREF+/VREF-</b>							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	E <sub>OFF</sub>	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

- Note 1:** These parameters are not characterized or tested in manufacturing.  
**2:** With no missing codes.  
**3:** These parameters are characterized, but not tested in manufacturing.  
**4:** Characterized with a 1 kHz sine wave.  
**5:** The ADC module is functional at  $V_{BORMIN} < V_{DD} < 2.0\text{V}$ , but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

# PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

## 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B