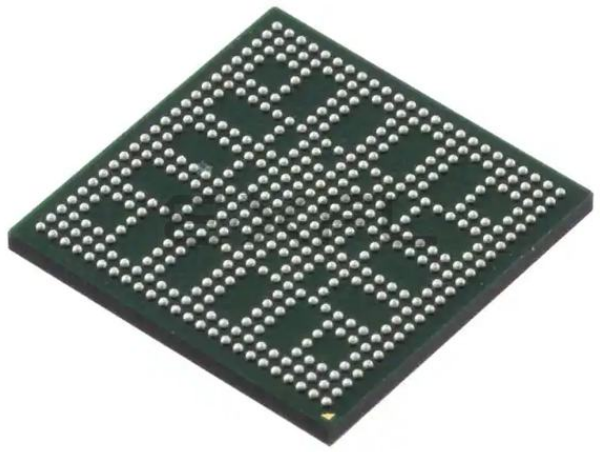

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LPDDR3
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	-
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.2V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6v7dvn10ab

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. GPIO module (1 - 5) supports 32 bits of I/O and GPIO6 supports 5 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 32-bit LPDDR2/LPDDR3 • Supports up to 2 GByte DDR memory space

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SLL processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing.

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SLL specific SoC characteristics: All three MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v5.0 including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SLL processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments"." Signal descriptions are provided in the *i.MX 6SLL Reference Manual*.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/ CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6SLL Reference Manual* for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard. The corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLK1 input/output could be disabled (if not used). If unused, the CLK1_N/P pair may remain unconnected.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SLL are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices).
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MODE must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MODE set to high configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MODE set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
ONOFF	In normal mode may be connected to ONOFF button (de-bouncing provided at this input). Internally this pad is pulled up. A short duration (<5s) connection to GND in OFF mode causes the internal power management state machine to change the state to ON. In ON mode, a short duration connection to GND generates interrupt (intended to initiate a software controllable power down). A long duration (above ~5s) connection to GND causes “forced” OFF.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SLL.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SLL Chip-Level Conditions

For these characteristics …	Topic appears …
Absolute Maximum Ratings	on page 15
Thermal Resistance	on page 17
Operating Ranges	on page 19
External Clock Sources	on page 20
Maximum Supply Currents	on page 21
Low Power Mode Supply Currents	on page 22
USB PHY Current Consumption	on page 23

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 shows the absolute maximum operating ratings.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max[1]	Unit
Core supply voltages	VDD_ARM_IN VDD_SOC_IN	-0.3	1.4	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975 (see note 2)	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.6	V
USB_OTG1_VBUS, USB_OTG2_VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Input voltage on USB_OTG1_DP, USB_OTG1_DN, and USB_OTG2_DP, USB_OTG2_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V

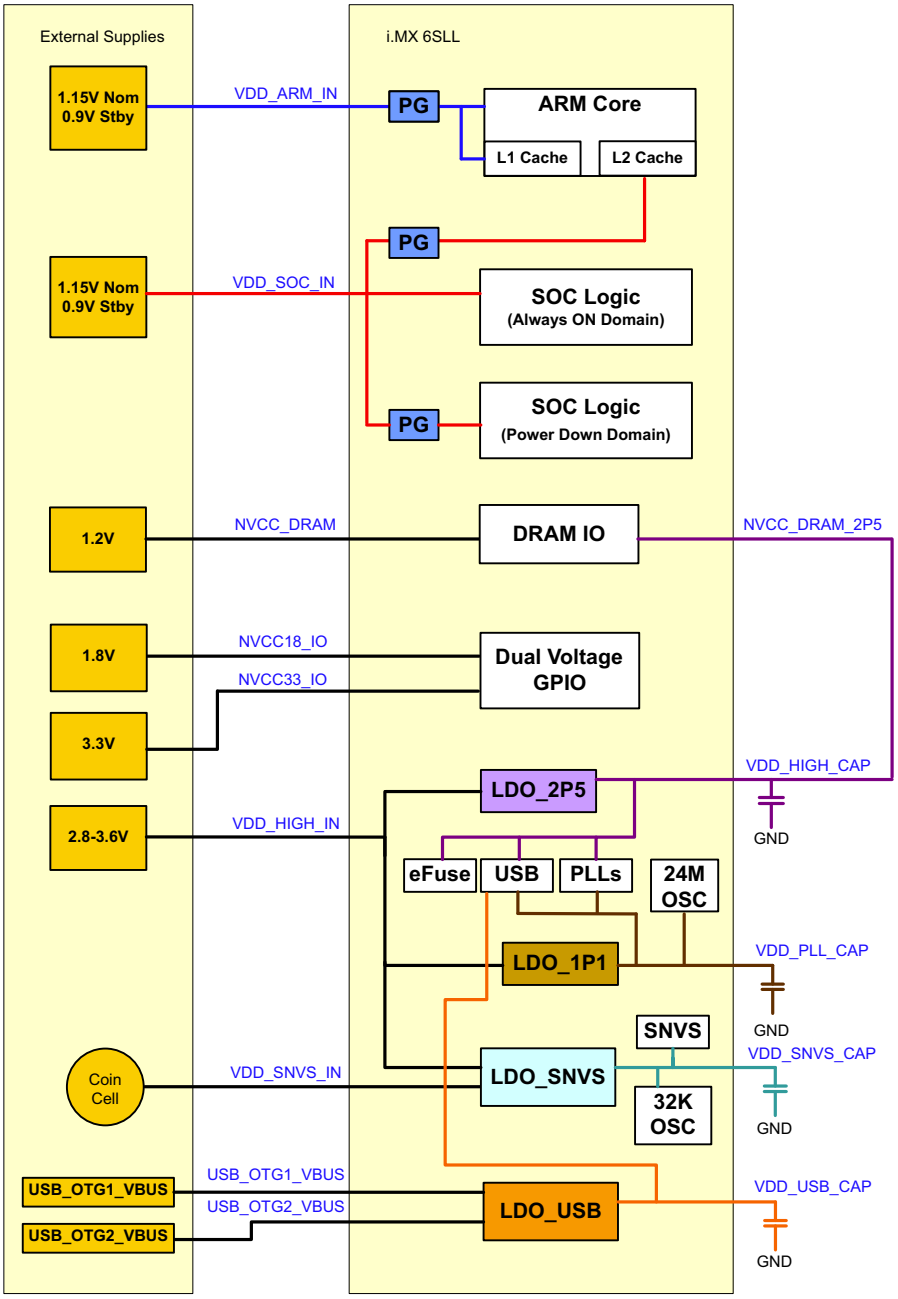

Figure 3. i.MX 6SLL SoC Power Block Diagram

4.2.2 Power-Down Sequence

For power-down sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned off after all other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after all other supply are switched off.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC33_IO and NVCC18_IO) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 64, "14 x 14 mm Functional Contact Assignments," on page 71.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6SLL Reference Manual* for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Regulators for Analog Modules

4.3.1.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. LDO_1P1 supplies the USB Phy and the PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG). For additional information, see the *i.MX 6SLL Reference Manual*.

4.3.1.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for min and max input requirements). Typical programming operating range is 2.25 V to 2.75 V

with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB Phy, LVDS Phy and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG).

For additional information, see the *i.MX 6SLL Reference Manual* (IMX6SLLRM).

4.3.1.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG1_VBUS and USB_OTG2_VBUS voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG).

For additional information, see the *i.MX 6SLL Reference Manual* (IMX6SLLRM).

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 23 and Table 24, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 23. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 24. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs.

The i.MX 6SLL MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6SLL Applications Processor* (IMX6SLLHDG).

Table 25 shows the AC parameters for DDR I/O operating in LPDDR2 and LPDDR3 mode.

Table 25. DDR I/O AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 and LPDDR3 specification (JESD209_2B and JESD209-3B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SLL processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Single Voltage General Purpose I/O cell set (GPIO)

Table 39. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC input setup time	t_{ISU}	2.5	—	ns
SD8	eSDHC input hold time[5]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 uSDHC3 dat4 ~ dat7 have two pad groups. The first group use SD2 pad and run at 52 MHz for output. The second group use KEY pad and only run at 50 MHz for output.

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 19 depicts the timing of eMMC4.4/4.41. Table 40 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SDx_CMD).

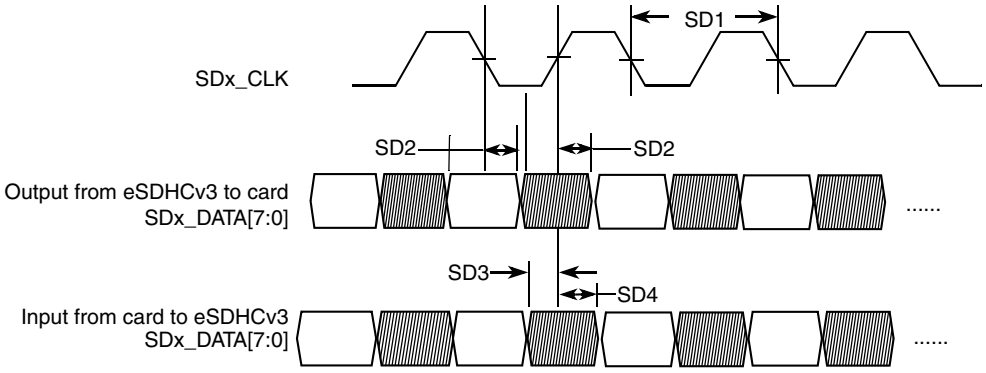

Figure 19. eMMC4.4/4.41 Timing

Table 40. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to CLK)					
SD2	uSDHC output delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to CLK)					
SD3	uSDHC input setup time	t_{ISU}	1.7	—	ns
SD4	uSDHC input hold time	t_{IH}	1.5	—	ns

4.10.6 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMn_OUT) external pin (see external signals table in the *i.MX 6SLL Reference Manual* for PWM pin assignments).

Figure 23 depicts the timing of the PWM, and Table 44 lists the PWM timing parameters.

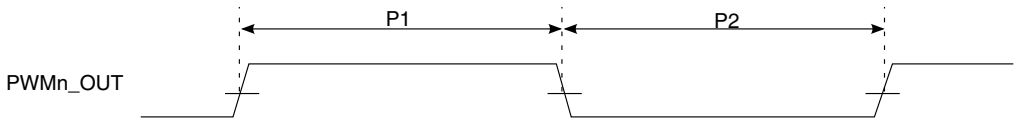

Figure 23. PWM Timing

Table 44. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	9.1591	—	ns

4.10.7 LCD Controller (LCDIF) Parameters

Figure 24 shows the LCDIF timing and Table 45 lists the timing parameters.

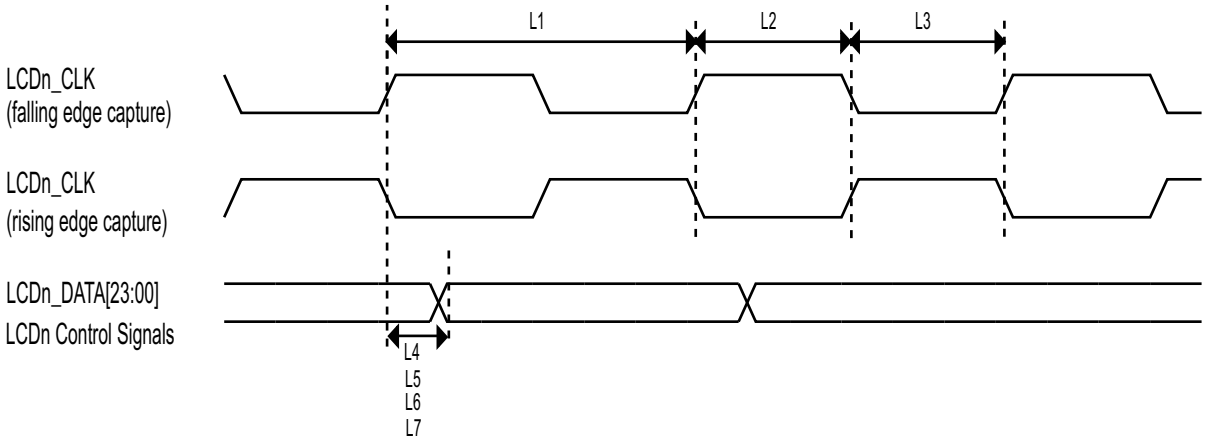

Figure 24. LCD Timing

Table 46. LCD Signal Parameters (continued)

LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.10.8 SCAN JTAG Controller (SJC) Timing Parameters

Figure 25 depicts the SJC test clock input timing. Figure 26 depicts the SJC boundary scan timing. Figure 27 depicts the SJC test access port. Signal parameters are listed in Table 47.

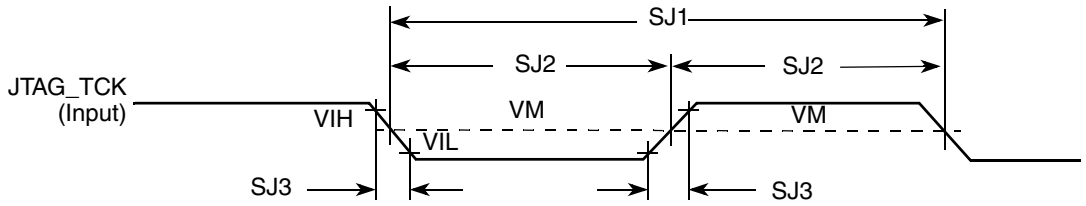

Figure 25. Test Clock Input Timing Diagram

Table 53. SSI Receiver Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC=0) and a non-inverted frame sync (TXFS/RXFS=0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11 UART I/O Configuration and Timing Parameters

4.10.11.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SLL UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 54 shows the UART I/O configuration based on the enabled mode.

Table 54. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UART_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UART_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UART_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UART_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UART_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UART_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.11.2.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 37 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 57 lists the transmit timing characteristics.

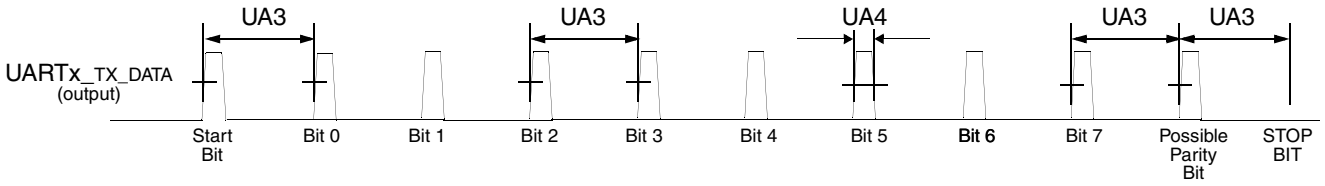

Figure 37. UART IrDA Mode Transmit Timing Diagram

Table 57. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] $- T_{ref\_clk}$ [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 38 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 58 lists the receive timing characteristics.

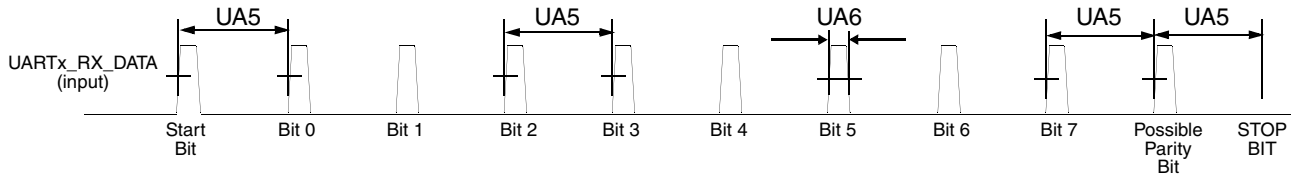

Figure 38. UART IrDA Mode Receive Timing Diagram

Table 58. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] $- 1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

Table 59. Fuses and Associated Pins Used for Boot (continued)

Ball Name	Direction at Reset	eFuse Name
LCD_DAT19	Input	BOOT_CFG4[3]
LCD_DAT20	Input	BOOT_CFG4[4]
LCD_DAT21	Input	BOOT_CFG4[5]
LCD_DAT22	Input	BOOT_CFG4[6]
LCD_DAT23	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 60 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 60. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Ball Names During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	—
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	—
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	—
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	—
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD1_DAT4, SD1_DAT5, SD1_DAT6, SD1_DAT7, GPIO3_IO30, GPIO4_IO7, ECSPI2_MOSI	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, SD2_DAT4, SD2_DAT5, SD2_DAT6, SD2_DAT7, SD2_RST, ECSPI1_MOSI	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, GPIO3_IO26, GPIO3_IO27, GPIO3_IO28, GPIO3_IO29, GPIO4_IO4, GPIO4_IO5	1, 4, or 8 bit Fastboot
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B	—

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
DRAM_D21	W1	DRAM	DDR	ALT0	DRAM_D[21]	Input	PU (100K)	PU (100K)
DRAM_D22	U1	DRAM	DDR	ALT0	DRAM_D[22]	Input	PU (100K)	PU (100K)
DRAM_D23	V1	DRAM	DDR	ALT0	DRAM_D[23]	Input	PU (100K)	PU (100K)
DRAM_D24	E2	DRAM	DDR	ALT0	DRAM_D[24]	Input	PU (100K)	PU (100K)
DRAM_D25	E1	DRAM	DDR	ALT0	DRAM_D[25]	Input	PU (100K)	PU (100K)
DRAM_D26	D1	DRAM	DDR	ALT0	DRAM_D[26]	Input	PU (100K)	PU (100K)
DRAM_D27	C2	DRAM	DDR	ALT0	DRAM_D[27]	Input	PU (100K)	PU (100K)
DRAM_D28	B1	DRAM	DDR	ALT0	DRAM_D[28]	Input	PU (100K)	PU (100K)
DRAM_D29	C1	DRAM	DDR	ALT0	DRAM_D[29]	Input	PU (100K)	PU (100K)
DRAM_D3	R1	DRAM	DDR	ALT0	DRAM_D[3]	Input	PU (100K)	PU (100K)
DRAM_D30	B2	DRAM	DDR	ALT0	DRAM_D[30]	Input	PU (100K)	PU (100K)
DRAM_D31	A2	DRAM	DDR	ALT0	DRAM_D[31]	Input	PU (100K)	PU (100K)
DRAM_D4	P2	DRAM	DDR	ALT0	DRAM_D[4]	Input	PU (100K)	PU (100K)
DRAM_D5	N2	DRAM	DDR	ALT0	DRAM_D[5]	Input	PU (100K)	PU (100K)
DRAM_D6	M2	DRAM	DDR	ALT0	DRAM_D[6]	Input	PU (100K)	PU (100K)
DRAM_D7	N1	DRAM	DDR	ALT0	DRAM_D[7]	Input	PU (100K)	PU (100K)
DRAM_D8	J2	DRAM	DDR	ALT0	DRAM_D[8]	Input	PU (100K)	PU (100K)
DRAM_D9	H1	DRAM	DDR	ALT0	DRAM_D[9]	Input	PU (100K)	PU (100K)

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
DRAM_DQM0	P3	DRAM	DDR	ALT0	DRAM_DQM[0]	Output	0	PU (100K)
DRAM_DQM1	F3	DRAM	DDR	ALT0	DRAM_DQM[1]	Output	0	PU (100K)
DRAM_DQM2	T3	DRAM	DDR	ALT0	DRAM_DQM[2]	Output	0	PU (100K)
DRAM_DQM3	C3	DRAM	DDR	ALT0	DRAM_DQM[3]	Output	0	PU (100K)
DRAM_SDCKE0	M1	DRAM	DDR	ALT0	DRAM_SDCKE[0]	Output	0	PD (100K)
DRAM_SDCKE1	K3	DRAM	DDR	ALT0	DRAM_SDCKE[1]	Output	0	PD (100K)
DRAM_SDCLK_0	J4	DRAM	DDRCLK	ALT0	DRAM_SDCLK[0]	Input	Hi-Z	PU (100K)
DRAM_SDCLK_0_B	J3	DRAM	—	—	—	—	—	—
DRAM_SDQS0	R3	DRAM	DDRCLK	ALT0	DRAM_SDQS[0]	Input	Hi-Z	Not connected
DRAM_SDQS0_B	R4	DRAM	—	—	—	—	—	—
DRAM_SDQS1	E4	DRAM	DDRCLK	ALT0	DRAM_SDQS[1]	Input	Hi-Z	Not connected
DRAM_SDQS1_B	E3	DRAM	—	—	—	—	—	—
DRAM_SDQS2	U2	DRAM	DDRCLK	ALT0	DRAM_SDQS[2]	Input	Hi-Z	Not connected
DRAM_SDQS2_B	U3	DRAM	—	—	—	—	—	—
DRAM_SDQS3	D2	DRAM	DDRCLK	ALT0	DRAM_SDQS[3]	Input	Hi-Z	Not connected
DRAM_SDQS3_B	D3	DRAM	—	—	—	—	—	—
ECSPI1_MISO	L18	GPIO	GPIO	ALT5	GPIO4_GPIO[10]	Not connected	Hi-Z	Hi-Z
ECSPI1_MOSI	M18	GPIO	GPIO	ALT5	GPIO4_GPIO[9]	Not connected	Hi-Z	Hi-Z
ECSPI1_SCLK	M17	GPIO	GPIO	ALT5	GPIO4_GPIO[8]	Not connected	Hi-Z	Hi-Z
ECSPI1_SS0	L17	GPIO	GPIO	ALT5	GPIO4_GPIO[11]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
SD1_DAT5	A17	GPIO	GPIO	ALT5	GPIO5_GPIO[9]	Not connected	Hi-Z	Hi-Z
SD1_DAT6	A16	GPIO	GPIO	ALT5	GPIO5_GPIO[7]	Not connected	Hi-Z	Hi-Z
SD1_DAT7	D14	GPIO	GPIO	ALT5	GPIO5_GPIO[10]	Not connected	Hi-Z	Hi-Z
SD2_CLK	Y19	GPIO	GPIO	ALT5	GPIO5_GPIO[5]	Not connected	Hi-Z	Hi-Z
SD2_CMD	W20	GPIO	GPIO	ALT5	GPIO5_GPIO[4]	Not connected	Hi-Z	Hi-Z
SD2_DAT0	Y18	GPIO	GPIO	ALT5	GPIO5_GPIO[1]	Not connected	Hi-Z	Hi-Z
SD2_DAT1	W18	GPIO	GPIO	ALT5	GPIO4_GPIO[30]	Not connected	Hi-Z	Hi-Z
SD2_DAT2	V18	GPIO	GPIO	ALT5	GPIO5_GPIO[3]	Not connected	Hi-Z	Hi-Z
SD2_DAT3	W19	GPIO	GPIO	ALT5	GPIO4_GPIO[28]	Not connected	Hi-Z	Hi-Z
SD2_DAT4	V20	GPIO	GPIO	ALT5	GPIO5_GPIO[2]	Not connected	Hi-Z	Hi-Z
SD2_DAT5	U17	GPIO	GPIO	ALT5	GPIO4_GPIO[31]	Not connected	Hi-Z	Hi-Z
SD2_DAT6	U18	GPIO	GPIO	ALT5	GPIO4_GPIO[29]	Not connected	Hi-Z	Hi-Z
SD2_DAT7	V19	GPIO	GPIO	ALT5	GPIO5_GPIO[0]	Not connected	Hi-Z	Hi-Z
SD2_RST	U19	GPIO	GPIO	ALT5	GPIO4_GPIO[27]	Not connected	Hi-Z	Hi-Z
SD3_CLK	U7	GPIO	GPIO	ALT5	GPIO5_GPIO[18]	Not connected	Hi-Z	Hi-Z
SD3_CMD	W7	GPIO	GPIO	ALT5	GPIO5_GPIO[21]	Not connected	Hi-Z	Hi-Z
SD3_DAT0	Y8	GPIO	GPIO	ALT5	GPIO5_GPIO[19]	Not connected	Hi-Z	Hi-Z
SD3_DAT1	W8	GPIO	GPIO	ALT5	GPIO5_GPIO[20]	Not connected	Hi-Z	Hi-Z

Table 65. 14 x 14 mm, 0.65 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
R	DRAM_D3	DRAM_D2	DRAM_SDQS0	DRAM_SDQS0_B	GND	NVCC_DRAM_2P5	NVCC_1V8	NVCC_1V8	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	GND	LCD_DAT6	LCD_CLK	LCD_DAT7	LCD_DAT4
T	DRAM_D1	DRAM_D0	DRAM_DQM2	GND	PWM1	GND	GND	REF_CLK_24M	JTAG_MOD	REF_CLK_32K	BOOT_MODE1	TAMPER	VDD_USB_CAP	NGND_KEL0	GND	GPANAIO	LCD_DAT5	LCD_DAT3	LCD_DAT2	LCD_DAT1
U	DRAM_D22	DRAM_SDQS2	DRAM_SDQS2_B	GPIO4_IO21	GPIO4_IO20	GPIO4_IO16	SD3_CLK	JTAG_TDI	JTAG_TMS	JTAG_TRSTB	TEST_MODE	ONOFF	XTALO	VDD_SNVS_CAP	CLK1_N	VDD_HIGH_CAP	SD2_DAT5	SD2_DAT6	SD2_RST	LCD_DAT0
V	DRAM_D23	DRAM_D20	GND	GPIO4_IO19	GPIO4_IO25	GPIO4_IO226	SD3_DAT2	SD3_DAT3	JTAG_TCK	JTAG_TDO	POR_B	GND	XTALI	VDD_SNVS_IN	CLK1_P	VDD_HIGH_CAP	NVCC_PLL	SD2_DAT2	SD2_DAT7	SD2_DAT4
W	DRAM_D21	DRAM_D18	DRAM_D16	GPIO4_IO17	GPIO4_IO23	GPIO4_IO22	SD3_CMD	SD3_DAT1	I2C1_SDA	PMC_STBY_REQ	BOOT_MODE0	USB_OTG2_DP	USB_OTG1_VBUS	USB_OTG1_DP	USB_OTG1_CHD_B	RTC_XTALO	VDD_HIGH_IN	SD2_DAT1	SD2_DAT3	SD2_CMD
Y	GND	DRAM_D19	DRAM_D17	GND	GPIO4_IO18	GPIO4_IO24	GND	SD3_DAT0	I2C1_SCL	PMIC_ON_REQ	GND	USB_OTG2_DN	USB_OTG2_VBUS	USB_OTG1_DN	GND	RTC_XTALI	VDD_HIGH_IN	SD2_DAT0	SD2_CLK	GND