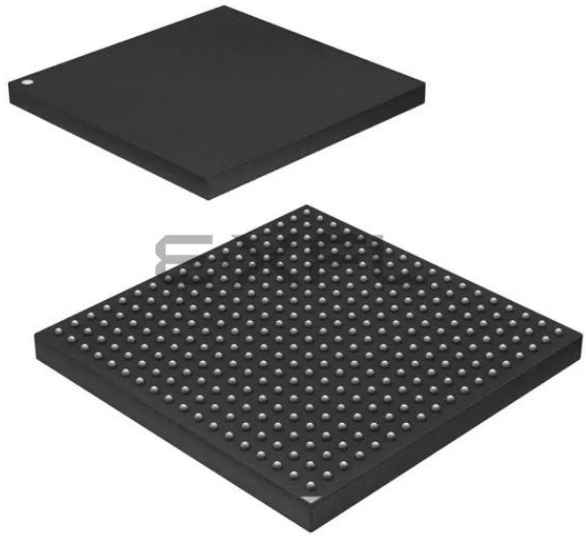

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	536MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	324-LFBGA
Supplier Device Package	324-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d31a-cu

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
P13	VDDIOM	EBI	PE0	I/O	—	—	A0/NBS0	O	—	—	—	—	A,I, PD, ST
R14	VDDIOM	EBI	PE1	I/O	—	—	A1	O	—	—	—	—	A,I, PD, ST
R13	VDDIOM	EBI	PE2	I/O	—	—	A2	O	—	—	—	—	A,I, PD, ST
V18	VDDIOM	EBI	PE3	I/O	—	—	A3	O	—	—	—	—	A,I, PD, ST
P14	VDDIOM	EBI	PE4	I/O	—	—	A4	O	—	—	—	—	A,I, PD, ST
U18	VDDIOM	EBI	PE5	I/O	—	—	A5	O	—	—	—	—	A,I, PD, ST
T18	VDDIOM	EBI	PE6	I/O	—	—	A6	O	—	—	—	—	A,I, PD, ST
R15	VDDIOM	EBI	PE7	I/O	—	—	A7	O	—	—	—	—	A,I, PD, ST
P17	VDDIOM	EBI	PE8	I/O	—	—	A8	O	—	—	—	—	A,I, PD, ST
P15	VDDIOM	EBI	PE9	I/O	—	—	A9	O	—	—	—	—	A,I, PD, ST
P18	VDDIOM	EBI	PE10	I/O	—	—	A10	O	—	—	—	—	A,I, PD, ST
R16	VDDIOM	EBI	PE11	I/O	—	—	A11	O	—	—	—	—	A,I, PD, ST
N16	VDDIOM	EBI	PE12	I/O	—	—	A12	O	—	—	—	—	A,I, PD, ST
R17	VDDIOM	EBI	PE13	I/O	—	—	A13	O	—	—	—	—	A,I, PD, ST
N17	VDDIOM	EBI	PE14	I/O	—	—	A14	O	—	—	—	—	A,I, PD, ST
R18	VDDIOM	EBI	PE15	I/O	—	—	A15	O	SCK3	I/O	—	—	A,I, PD, ST
N18	VDDIOM	EBI	PE16	I/O	—	—	A16	O	CTS3	I	—	—	A,I, PD, ST
P16	VDDIOM	EBI	PE17	I/O	—	—	A17	O	RTS3	O	—	—	A,I, PD, ST
M18	VDDIOM	EBI	PE18	I/O	—	—	A18	O	RXD3	I	—	—	A,I, PD, ST
N15	VDDIOM	EBI	PE19	I/O	—	—	A19	O	TXD3	O	—	—	A,I, PD, ST
M15	VDDIOM	EBI	PE20	I/O	—	—	A20	O	SCK2	I/O	—	—	A,I, PD, ST
N14	VDDIOM	EBI	PE21	I/O	—	—	A21/NANDALE	O	—	—	—	—	A,I, PD, ST
M17	VDDIOM	EBI	PE22	I/O	—	—	A22/NANDCLE	O	—	—	—	—	A,I, PD, ST
M13	VDDIOM	EBI	PE23	I/O	—	—	A23	O	CTS2	I	—	—	A,I, PD, ST
M16	VDDIOM	EBI	PE24	I/O	—	—	A24	O	RTS2	O	—	—	A,I, PD, ST
N12	VDDIOM	EBI	PE25	I/O	—	—	A25	O	RXD2	I	—	—	A,I, PD, ST
M14	VDDIOM	EBI	PE26	I/O	—	—	NCS0	O	TXD2	O	—	—	A,I, PD, ST
M12	VDDIOM	EBI	PE27	I/O	—	—	NCS1	O	TIOA2	I/O	LCDDAT22	O	PIO,I, PD, ST
L13	VDDIOM	EBI	PE28	I/O	—	—	NCS2	O	TIOB2	I/O	LCDDAT23	O	PIO, I, PD, ST
L15	VDDIOM	EBI	PE29	I/O	—	—	NWR1/NBS1	O	TCLK2	I	—	—	PIO, I, PD, ST
L14	VDDIOM	EBI	PE30	I/O	—	—	NWAIT	I	—	—	—	—	PIO, I, PD, ST
L16	VDDIOM	EBI	PE31	I/O	—	—	IRQ	I	PWML1	O	—	—	PIO,I, PD, ST
U15	VDDBU	SYSC	TST	I	—	—	—	—	—	—	—	—	I, PD,
U9	VDDIOP0	SYSC	BMS	I	—	—	—	—	—	—	—	—	I
U8	VDDIOP0	CLOCK	XIN	I	—	—	—	—	—	—	—	—	I
V8	VDDIOP0	CLOCK	XOUT	O	—	—	—	—	—	—	—	—	O
U16	VDDBU	CLOCK	XIN32	I	—	—	—	—	—	—	—	—	I
V16	VDDBU	CLOCK	XOUT32	O	—	—	—	—	—	—	—	—	O
T12	VDDBU	SYSC	SHDN	O	—	—	—	—	—	—	—	—	O
T10	VDDBU	SYSC	WKUP	I	—	—	—	—	—	—	—	—	I, ST
V9	VDDIOP0	RSTJTAG	NRST	I/O	—	—	—	—	—	—	—	—	I, PU, ST
P11	VDDIOP0	RSTJTAG	NTRST	I	—	—	—	—	—	—	—	—	I, PU, ST
R8	VDDIOP0	RSTJTAG	TDI	I	—	—	—	—	—	—	—	—	I, ST

5. Power Considerations

5.1 Power Supplies

Table 5-1 defines the power supply rails and the estimated power consumption at typical voltage.

Table 5-1. SAMA5D3 Power supplies

Name	Voltage Range, Nominal	Associated Ground	Powers
VDDCORE	1.1–1.32V, 1.2V	GNDCORE	The core, including the processor, the embedded memories and the peripherals
VDDIODDR	1.7–1.9V, 1.8V 1.14–1.30, 1.2V	GNDIODDR	LPDDR/DDR2 Interface I/O lines LPDDR2 Interface I/O lines
VDDIOM	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	GNDIOM	NAND and HSMC Interface I/O lines
VDDIOP0	1.65–3.6V	GNDIOP	Peripheral I/O lines
VDDIOP1	1.65–3.6V	GNDIOP	Peripheral I/O lines
VDDBU	1.65–3.6V	GNDBU	The Slow Clock Oscillator, the internal 32 kHz RC Oscillator and a part of the System Controller
VDDUTMIC	1.1–1.32V, 1.2V	GNDUTMI	The USB device and host UTMI+ core The UTMI PLL
VDDUTMII	3.0–3.6V, 3.3V	GNDUTMI	The USB device and host UTMI+ interface
VDDPLLA	1.1–1.32V, 1.2V	GNDPLL	The PLLA cell
VDDOSC	1.65–3.6V	GNDOSC	Main Oscillator Cell and PLL UTMI. If PLL UTMI is used the range is to be 3.0V to 3.6V.
VDDANA	3.0–3.6V, 3.3V	GNDANA	The Analog-to-Digital Converter
VDDFUSE	2.25–2.75V, 2.5V	GNDFUSE	Fuse box for programming. It can be tied to ground with a 100 Ω resistor for fuse reading only.

5.2 Power-up Consideration

The user must first activate VDDIOP and VDDIOM, then VDDPLL and VDDCORE with the constraint that VDDPLL is established no later than 1 ms after VDDCORE.

The VDDCORE and VDDBU power supplies rising time must be defined according to the Core and Backup Power-On-Reset characteristics to ensure VDDCORE or VDDBU has reached V_{IH} after the POR reset time.

Please refer to the “Core Power Supply POR Characteristics” and “Backup Power Supply POR Characteristics” sections of the product datasheet for power-up constraints.

5.3 Power-down Consideration

The user must remove VDDPLL first, then VDDCORE, and at last VDDIOP and VDDIOM, to ensure a reliable operation of the device.

Figure 40-24.Multi-master Flowchart

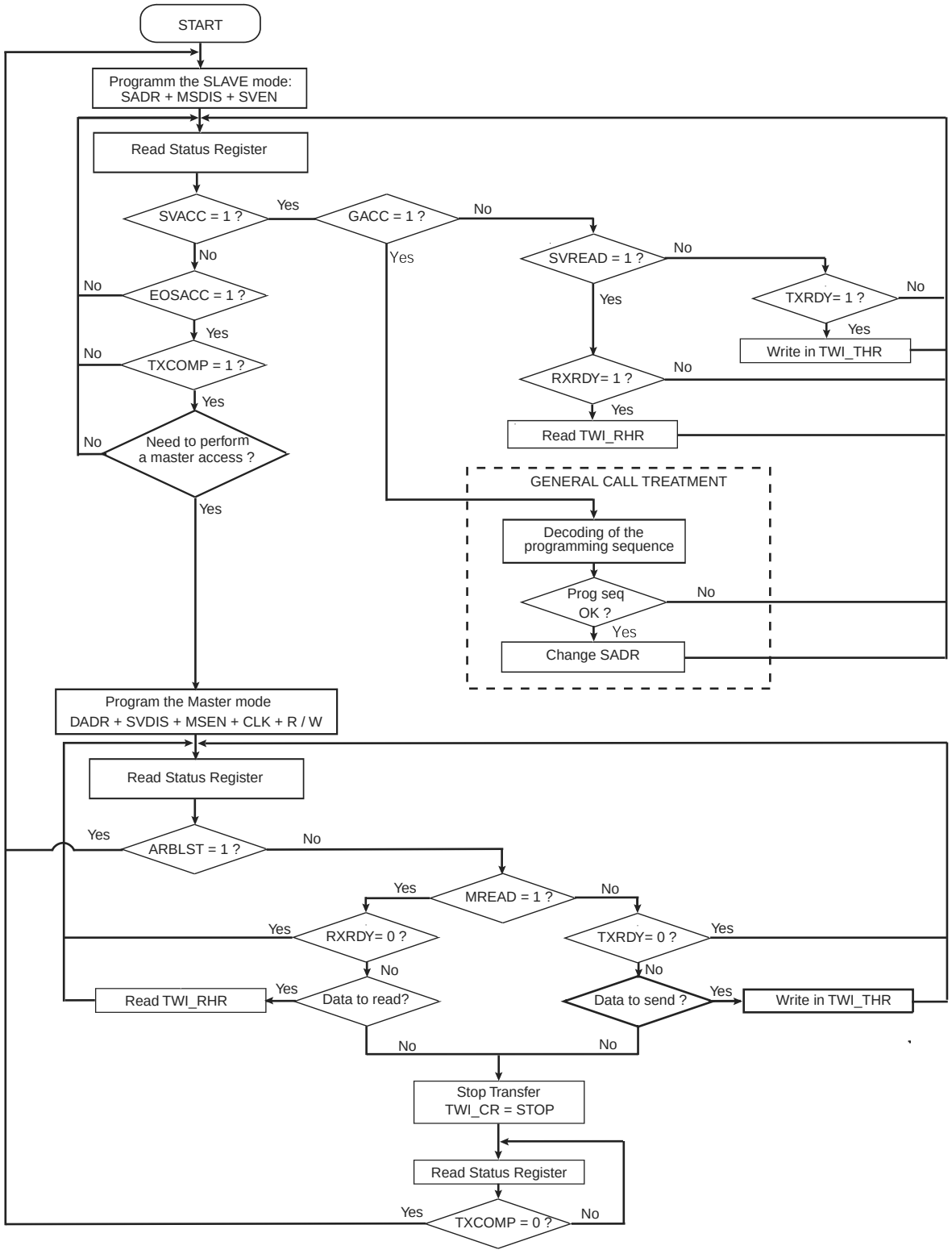
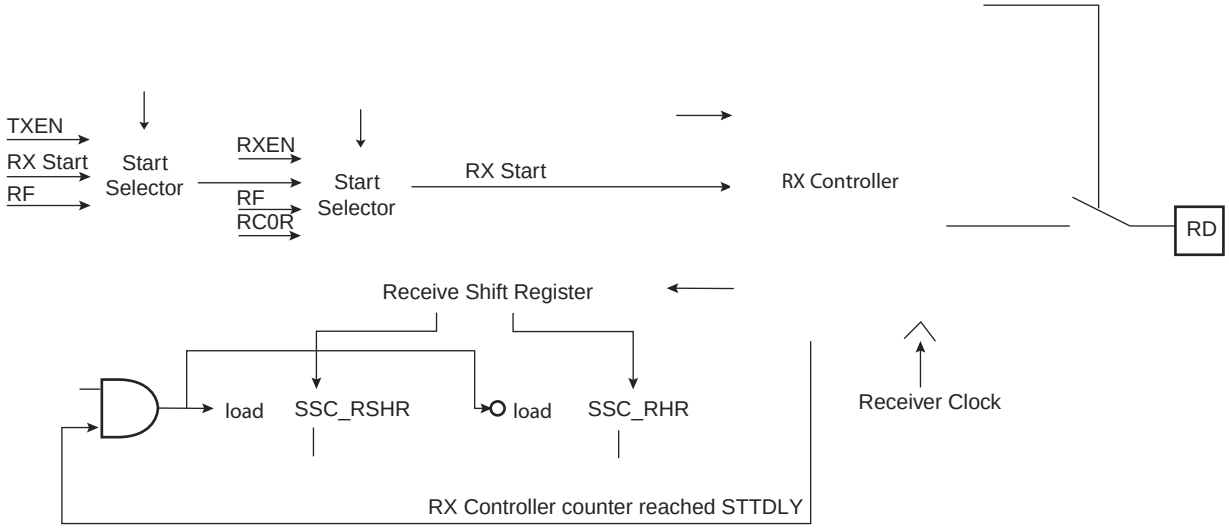


Figure 41-9. Receiver Block Diagram



41.7.4 Start

The transmitter and receiver can both be programmed to start their operations when an event occurs, respectively in the Transmit Start Selection (START) field of SSC_TCMR and in the Receive Start Selection (START) field of SSC_RCMR.

Under the following conditions the start event is independently programmable:

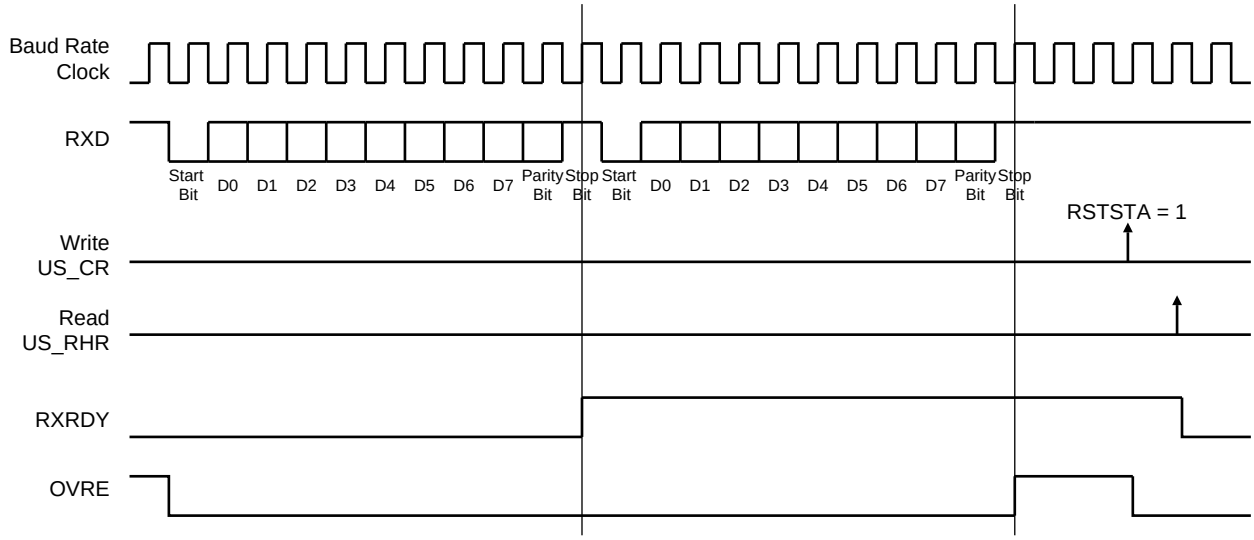
- Continuous. In this case, the transmission starts as soon as a word is written in SSC_THR and the reception starts as soon as the Receiver is enabled.
- Synchronously with the transmitter/receiver
- On detection of a falling/rising edge on TF/RF
- On detection of a low level/high level on TF/RF
- On detection of a level change or an edge on TF/RF

A start can be programmed in the same manner on either side of the Transmit/Receive Clock Register (RCMR/TCMR). Thus, the start could be on TF (Transmit) or RF (Receive).

Moreover, the Receiver can start when data is detected in the bit stream with the Compare Functions.

Detection on TF/RF input/output is done by the field FSOS of the Transmit/Receive Frame Mode Register (TFMR/RFMR).

Figure 44-21.Receiver Status



44.7.3.8 Parity

The USART supports five parity modes selected by writing to the PAR field in the US_MR. The PAR field also enables the Multidrop mode, see “Multidrop Mode” on page 1385. Even and odd parity bit generation and error detection are supported.

If even parity is selected, the parity generator of the transmitter drives the parity bit to 0 if a number of 1s in the character data bit is even, and to 1 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If odd parity is selected, the parity generator of the transmitter drives the parity bit to 1 if a number of 1s in the character data bit is even, and to 0 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If the mark parity is used, the parity generator of the transmitter drives the parity bit to 1 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 0. If the space parity is used, the parity generator of the transmitter drives the parity bit to 0 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 1. If parity is disabled, the transmitter does not generate any parity bit and the receiver does not report any parity error.

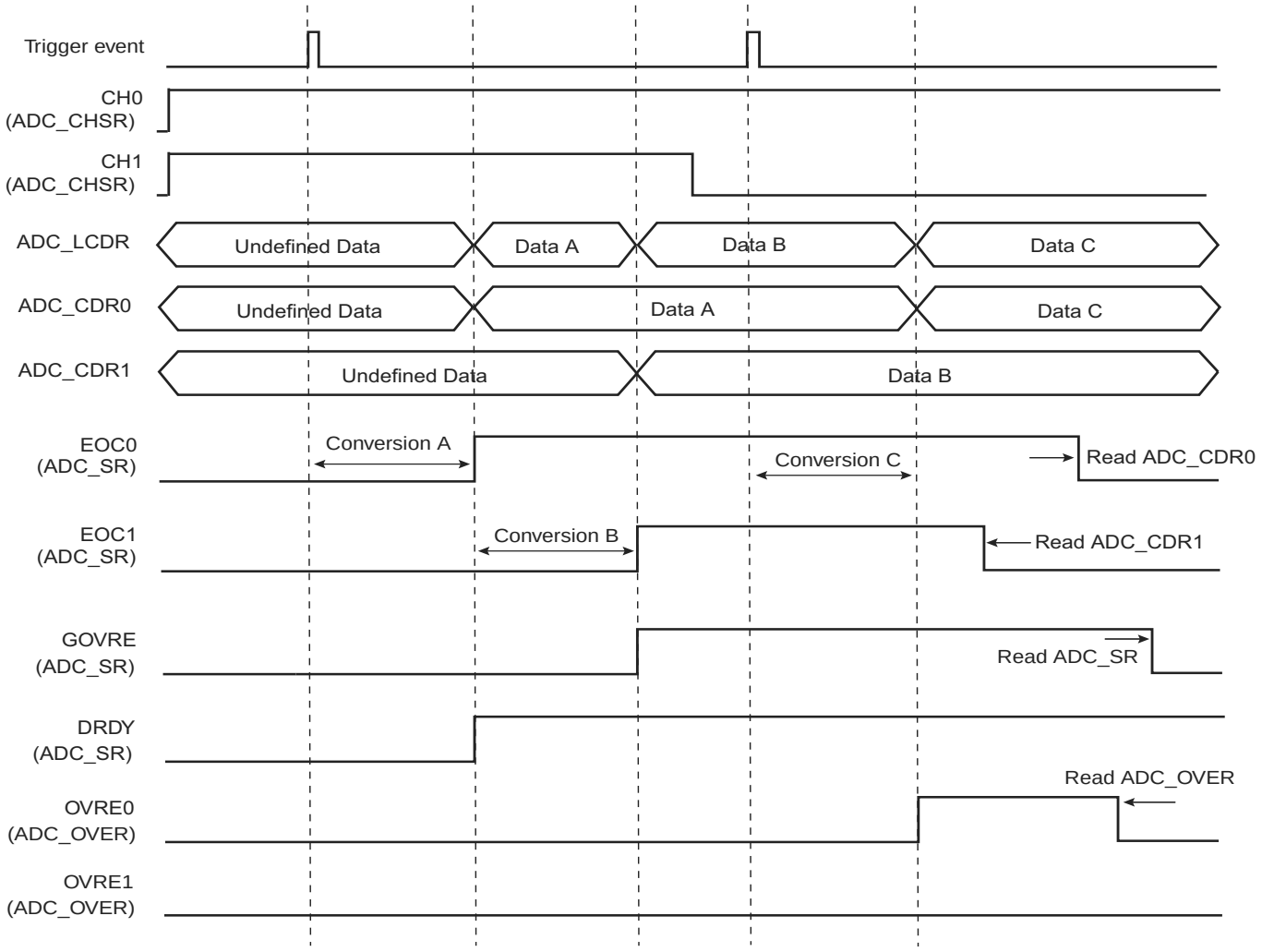
Table 44-9 shows an example of the parity bit for the character 0x41 (character ASCII “A”) depending on the configuration of the USART. Because there are two bits to 1, 1 bit is added when a parity is odd, or 0 is added when a parity is even.

Table 44-9. Parity Bit Examples

Character	Hexadecimal	Binary	Parity Bit	Parity Mode
A	0x41	0100 0001	1	Odd
A	0x41	0100 0001	0	Even
A	0x41	0100 0001	1	Mark
A	0x41	0100 0001	0	Space
A	0x41	0100 0001	None	None

When the receiver detects a parity error, it sets the PARE (Parity Error) bit in the US_CSR. The PARE bit can be cleared by writing the US_CR with the RSTSTA bit to 1. Figure 44-22 illustrates the parity bit status setting and clearing.

Figure 49-5. GOVRE and OVREx Flag Behavior



Warning: If the corresponding channel is disabled during a conversion or if it is disabled and then reenabled during a conversion, its associated data and its corresponding EOC and OVRE flags in ADC_SR are unpredictable.

49.8.19 ADC Analog Control Register

Name: ADC_ACR

Address: 0xF8018094

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	PENDETSENS	

This register can only be written if the WPEN bit is cleared in “ADC Write Protect Mode Register” .

- **PENDETSENS: Pen Detection Sensitivity**

Allows to modify the pen detection input pull-up resistor value. (See the product electrical characteristics for further details).

54.4.2 Master Clock Characteristics

The master clock is the maximum clock at which the system is able to run. It is given by the smallest value of the internal bus clock and EBI clock.

Table 54-10. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPMCK})$	Master Clock Frequency	VDDCORE[1.08V, 1.32V], T_A = 85°C	125(1)	134	MHz
		VDDCORE[1.2V, 1.32V], VDDIODDR[1.75V, 1.9V], DDR2 mode only, T_A = 85°C	125(1)	166	

Note: 1. Limitation for DDR2 usage only. There are no limitations to LP-DDR and LP-DDR2.