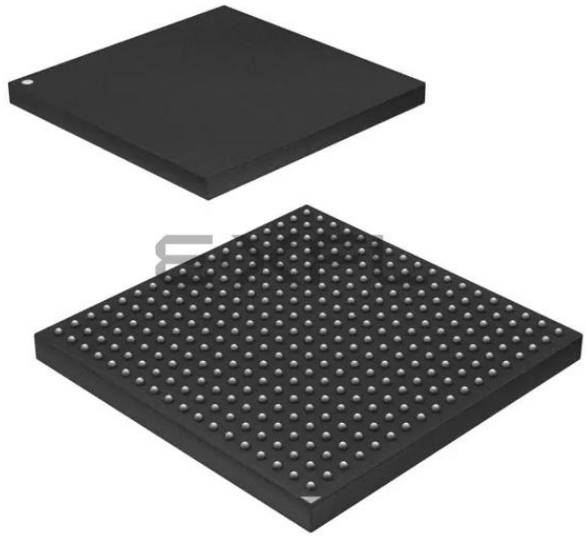

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	536MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	324-LFBGA
Supplier Device Package	324-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d34a-cu

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
H13	VDDIODDR	DDR_IO	DDR_D2	I/O	—	—	—	—	—	—	—	—	HiZ
G17	VDDIODDR	DDR_IO	DDR_D3	I/O	—	—	—	—	—	—	—	—	HiZ
G16	VDDIODDR	DDR_IO	DDR_D4	I/O	—	—	—	—	—	—	—	—	HiZ
H15	VDDIODDR	DDR_IO	DDR_D5	I/O	—	—	—	—	—	—	—	—	HiZ
F17	VDDIODDR	DDR_IO	DDR_D6	I/O	—	—	—	—	—	—	—	—	HiZ
G15	VDDIODDR	DDR_IO	DDR_D7	I/O	—	—	—	—	—	—	—	—	HiZ
F16	VDDIODDR	DDR_IO	DDR_D8	I/O	—	—	—	—	—	—	—	—	HiZ
E17	VDDIODDR	DDR_IO	DDR_D9	I/O	—	—	—	—	—	—	—	—	HiZ
G14	VDDIODDR	DDR_IO	DDR_D10	I/O	—	—	—	—	—	—	—	—	HiZ
E16	VDDIODDR	DDR_IO	DDR_D11	I/O	—	—	—	—	—	—	—	—	HiZ
D17	VDDIODDR	DDR_IO	DDR_D12	I/O	—	—	—	—	—	—	—	—	HiZ
C18	VDDIODDR	DDR_IO	DDR_D13	I/O	—	—	—	—	—	—	—	—	HiZ
D16	VDDIODDR	DDR_IO	DDR_D14	I/O	—	—	—	—	—	—	—	—	HiZ
C17	VDDIODDR	DDR_IO	DDR_D15	I/O	—	—	—	—	—	—	—	—	HiZ
B16	VDDIODDR	DDR_IO	DDR_D16	I/O	—	—	—	—	—	—	—	—	HiZ
B18	VDDIODDR	DDR_IO	DDR_D17	I/O	—	—	—	—	—	—	—	—	HiZ
C15	VDDIODDR	DDR_IO	DDR_D18	I/O	—	—	—	—	—	—	—	—	HiZ
A18	VDDIODDR	DDR_IO	DDR_D19	I/O	—	—	—	—	—	—	—	—	HiZ
C16	VDDIODDR	DDR_IO	DDR_D20	I/O	—	—	—	—	—	—	—	—	HiZ
C14	VDDIODDR	DDR_IO	DDR_D21	I/O	—	—	—	—	—	—	—	—	HiZ
D15	VDDIODDR	DDR_IO	DDR_D22	I/O	—	—	—	—	—	—	—	—	HiZ
B14	VDDIODDR	DDR_IO	DDR_D23	I/O	—	—	—	—	—	—	—	—	HiZ
A15	VDDIODDR	DDR_IO	DDR_D24	I/O	—	—	—	—	—	—	—	—	HiZ
A14	VDDIODDR	DDR_IO	DDR_D25	I/O	—	—	—	—	—	—	—	—	HiZ
E12	VDDIODDR	DDR_IO	DDR_D26	I/O	—	—	—	—	—	—	—	—	HiZ
A11	VDDIODDR	DDR_IO	DDR_D27	I/O	—	—	—	—	—	—	—	—	HiZ
B11	VDDIODDR	DDR_IO	DDR_D28	I/O	—	—	—	—	—	—	—	—	HiZ
F12	VDDIODDR	DDR_IO	DDR_D29	I/O	—	—	—	—	—	—	—	—	HiZ
A10	VDDIODDR	DDR_IO	DDR_D30	I/O	—	—	—	—	—	—	—	—	HiZ
E11	VDDIODDR	DDR_IO	DDR_D31	I/O	—	—	—	—	—	—	—	—	HiZ
G12	VDDIODDR	DDR_IO	DDR_DQM0	O	—	—	—	—	—	—	—	—	O
E15	VDDIODDR	DDR_IO	DDR_DQM1	O	—	—	—	—	—	—	—	—	O
B15	VDDIODDR	DDR_IO	DDR_DQM2	O	—	—	—	—	—	—	—	—	O
D12	VDDIODDR	DDR_IO	DDR_DQM3	O	—	—	—	—	—	—	—	—	O
E18	VDDIODDR	DDR_IO	DDR_DQS0	I/O	—	—	—	—	—	—	—	—	I, PD
G18	VDDIODDR	DDR_IO	DDR_DQS1	I/O	—	—	—	—	—	—	—	—	I, PD
B17	VDDIODDR	DDR_IO	DDR_DQS2	I/O	—	—	—	—	—	—	—	—	I, PD
B13	VDDIODDR	DDR_IO	DDR_DQS3	I/O	—	—	—	—	—	—	—	—	I, PD
D18	VDDIODDR	DDR_IO	DDR_DQSN0	I/O	—	—	—	—	—	—	—	—	I, PU
F18	VDDIODDR	DDR_IO	DDR_DQSN1	I/O	—	—	—	—	—	—	—	—	I, PU
A17	VDDIODDR	DDR_IO	DDR_DQSN2	I/O	—	—	—	—	—	—	—	—	I, PU
A13	VDDIODDR	DDR_IO	DDR_DQSN3	I/O	—	—	—	—	—	—	—	—	I, PU
C8	VDDIODDR	DDR_IO	DDR_CS	O	—	—	—	—	—	—	—	—	O

26.2.15.11 PMC Master Clock Register

Name: PMC_MCKR

Address: 0xFFFFFC30

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	PLLADIV2	–	–	MDIV	

7	6	5	4	3	2	1	0
–	PRES			–	–	CSS	

- **CSS: Master/Processor Clock Source Selection**

Value	Name	Description
0	SLOW_CLK	Slow Clock is selected
1	MAIN_CLK	Main Clock is selected
2	PLLA_CLK	PLLACK is selected
3	UPLL_CLK	UPLL Clock is selected

- **PRES: Master/Processor Clock Prescaler**

Value	Name	Description
0	CLOCK	Selected clock
1	CLOCK_DIV2	Selected clock divided by 2
2	CLOCK_DIV4	Selected clock divided by 4
3	CLOCK_DIV8	Selected clock divided by 8
4	CLOCK_DIV16	Selected clock divided by 16
5	CLOCK_DIV32	Selected clock divided by 32
6	CLOCK_DIV64	Selected clock divided by 64
7	Reserved	Reserved

Figure 30-15.Early Read Wait State: NCS Controlled Write with No Hold Followed by a Read with No NCS Setup

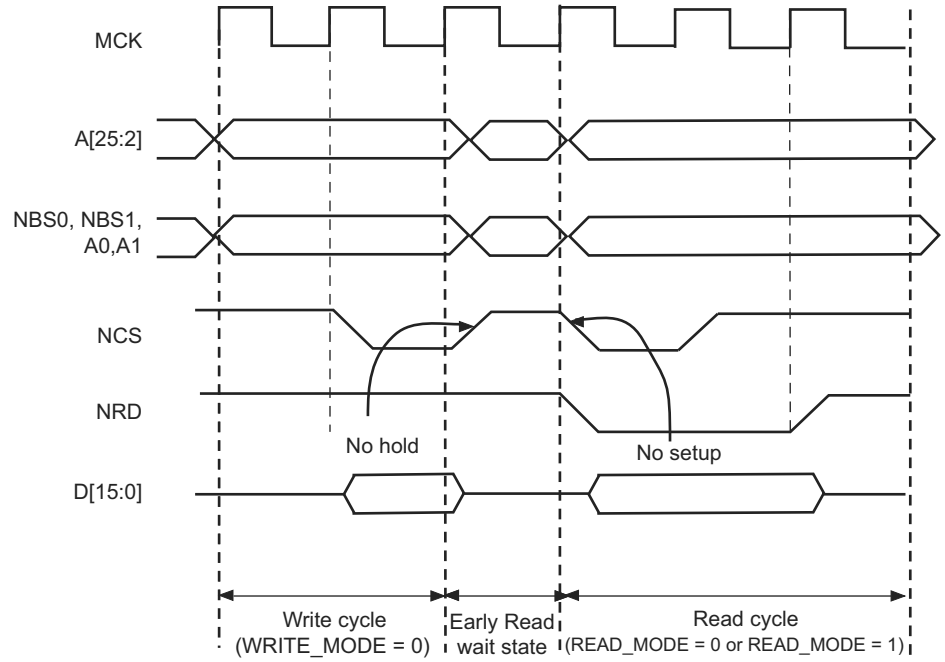
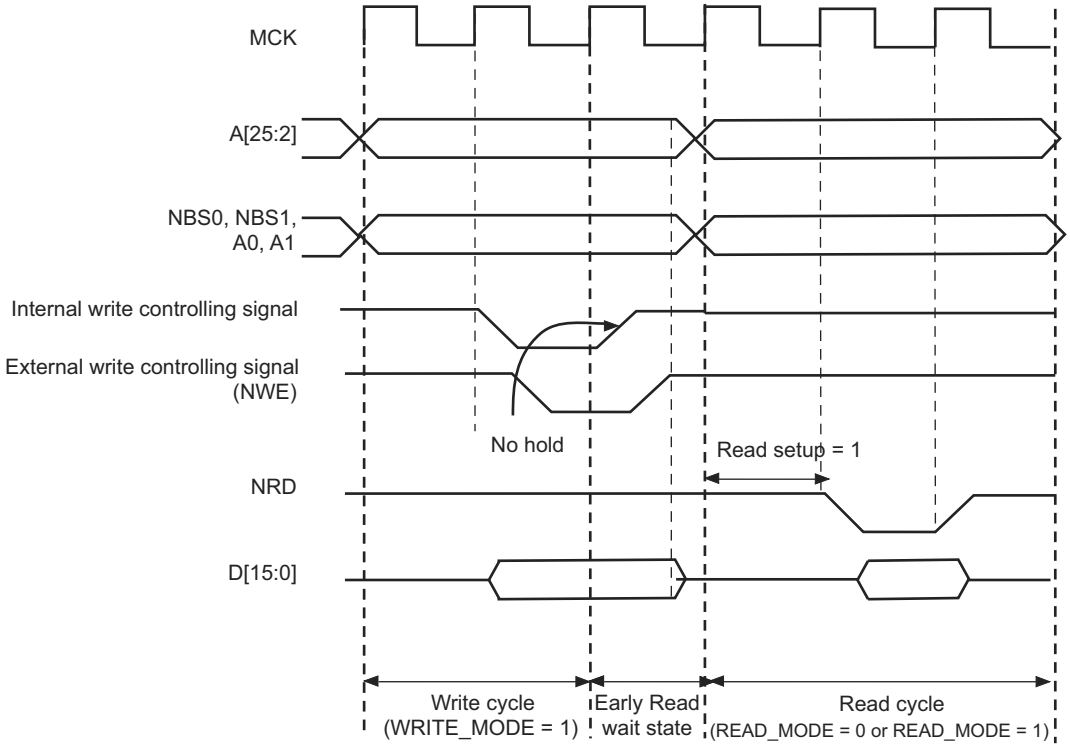


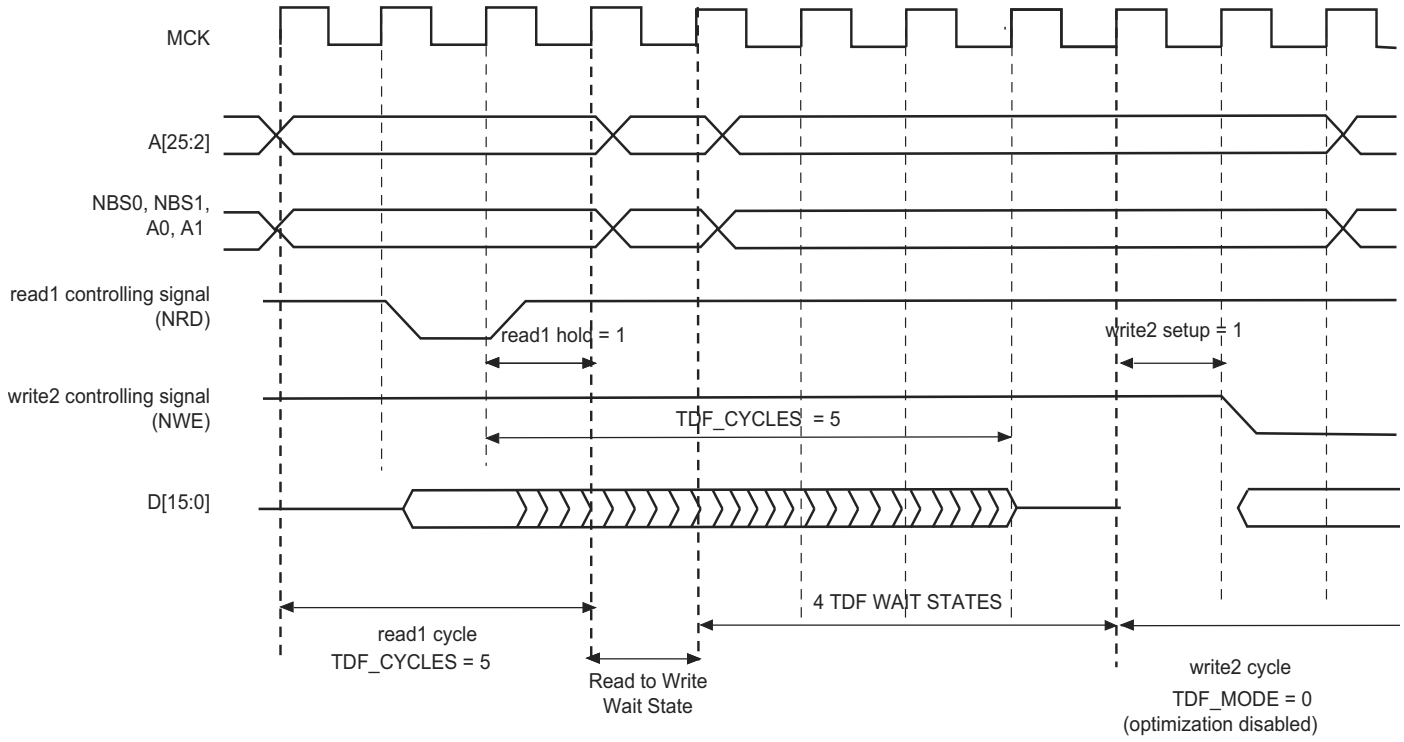
Figure 30-16.Early Read Wait State: NWE-controlled Write with No Hold Followed by a Read with one Set-up Cycle



30.12.3 Reload User Configuration Wait State

The user may change any of the configuration parameters by writing the SMC user interface.

Figure 30-22.TDF Mode = 0: TDF wait states between read and write accesses on the same chip select



30.14 External Wait

Any access can be extended by an external device using the NWAIT input signal of the SMC. The EXNW_MODE field of the HSMC_MODE register on the corresponding chip select must be set to either ‘10’ (frozen mode) or ‘11’ (ready mode). When the EXNW_MODE is set to ‘00’ (disabled), the NWAIT signal is simply ignored on the corresponding chip select. The NWAIT signal delays the read or write operation in regards to the read or write controlling signal, depending on the read and write modes of the corresponding chip select.

30.14.1 Restriction

When one of the EXNW_MODE is enabled, it is mandatory to program at least one hold cycle for the read/write controlling signal. For that reason, the NWAIT signal cannot be used in Slow Clock Mode (Section 30.15 “Slow Clock Mode” on page 432).

The NWAIT signal is assumed to be a response of the external device to the read/write request of the SMC. NWAIT is then examined by the SMC in the pulse state of the read or write controlling signal. The assertion of the NWAIT signal outside the expected period has no impact on the SMC behavior.

30.14.2 Frozen Mode

When the external device asserts the NWAIT signal (active low), and after an internal synchronization of this signal, the SMC state is frozen, i.e., SMC internal counters are frozen, and all control signals remain unchanged. When the resynchronized NWAIT signal is deasserted, the SMC completes the access, resuming the access from the point where it was stopped. See Figure 30-23. This mode must be selected when the external device uses the NWAIT signal to delay the access and to freeze the SMC.

The assertion of the NWAIT signal outside the expected period is ignored as illustrated in Figure 30-24.

Table 30-16. MLC Controller Configuration when the Host Controller is Used

	NFC		PMECC		
Transfer Type	**RSPARE**	**WSPARE**	**SPAREEN**	**AUTO**	**User Mode**
Program Page main area is protected, spare is not protected, spare is written manually	0	0	0	0	Not used
Program Page main area is protected, spare is protected, spare is written by NFC	0	1	1	0	Not used
Read Page main area is protected, spare is not protected, spare is not retrieved by NFC	0	0	0	0	Used
Read Page main area is protected, spare is not protected, spare is retrieved by NFC	1	0	0	1	Not used
Read Page main area is protected, spare is protected, spare is retrieved by NFC	1	0	1	0	Used

30.19 Software Implementation

30.19.1 Remainder Substitution Procedure

The substitute function evaluates the remainder polynomial, with different values of the field primitive element. The addition arithmetic operation is performed with the exclusive OR. The multiplication arithmetic operation is performed through the gf_log and gf_antilog look-up tables.

The REM2NP1 and REMN2NP3 fields of the PMECCREMN registers contain only odd remainders. Each bit indicates whether the coefficient of the remainder polynomial is set to zero or not.

NB_ERROR_MAX defines the maximum value of the error correcting capability.

NB_ERROR defines the error correcting capability selected at encoding/decoding time.

NB_FIELD_ELEMENTS defines the number of elements in the field.

si[] is a table that holds the current syndrome value. An element of that table belongs to the field. This is also a shared variable for the next step of the decoding operation.

oo[] is a table that contains the degree of the remainders.

```
int substitute()
{
int i;
int j;
for (i = 1; i < 2 * NB_ERROR_MAX; i++)
{
      si[i] = 0;
}
for (i = 1; i < 2*NB_ERROR; i++)
{
      for (j = 0; j < oo[i]; j++)
      {
```

Table 32-54. Register Mapping (Continued)

Offset	Register	Name	Access	Reset
...	...	...	...	...
0x19FC	Hardware Cursor CLUT Register 255	LCDC_HCRCLUT255	Read-write	0x00000000
0x1A00-0x1FE4	Reserved	–	–	–

Note: 1. The CLUT registers are located in the RAM.

32.7.82 High End Overlay Layer Interrupt Status Register

Name: LCDC_HEOISR

Address: 0xF0030358

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	VOVR	VDONE	VADD	VDSCR	VDMA	–	–
15	14	13	12	11	10	9	8
–	UOVR	UDONE	UADD	UDSCR	UDMA	–	–
7	6	5	4	3	2	1	0
–	OVR	DONE	ADD	DSCR	DMA	–	–

- **DMA: End of DMA Transfer**

When set to one this flag indicates that an End of Transfer has been detected. This flag is reset after a read operation.

- **DSCR: DMA Descriptor Loaded**

When set to one this flag indicates that a descriptor has been loaded successfully. This flag is reset after a read operation.

- **ADD: Head Descriptor Loaded**

When set to one this flag indicates that the descriptor pointed to by the head register has been loaded successfully. This flag is reset after a read operation.

- **DONE: End of List Detected**

When set to one this flag indicates that an End of List condition has occurred. This flag is reset after a read operation.

- **OVR: Overflow Detected**

When set to one this flag indicates that an overflow occurred. This flag is reset after a read operation.

- **UDMA: End of DMA Transfer for U component**

When set to one this flag indicates that an End of Transfer has been detected. This flag is reset after a read operation.

- **UDSCR: DMA Descriptor Loaded for U component**

When set to one this flag indicates that a descriptor has been loaded successfully. This flag is reset after a read operation.

- **UADD: Head Descriptor Loaded for U component**

When set to one this flag indicates that the descriptor pointed to by the head register has been loaded successfully. This flag is reset after a read operation.

- **UDONE: End of List Detected for U component**

When set to one this flag indicates that an End of List condition has occurred. This flag is reset after a read operation.

- **UOVR: Overflow Detected for U component**

When set to one this flag indicates that an overflow occurred. This flag is reset after a read operation.

- **VDMA: End of DMA Transfer for V component**

When set to one this flag indicates that an End of Transfer has been detected. This flag is reset after a read operation.

32.7.93 High End Overlay Layer V Control Register

Name: LCDC_HEOVCTRL

Address: 0xF0030384

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	VDONEIEN	VADDIEN	VDSCRIEN	VDMAIEN	–	VDFETCH

- **VDFETCH: Transfer Descriptor Fetch Enable**

0: Transfer Descriptor fetch is disabled.

1: Transfer Descriptor fetch is enabled.

- **VDMAIEN: End of DMA Transfer Interrupt Enable**

0: DMA transfer completed interrupt is enabled.

1: DMA transfer completed interrupt is disabled.

- **VDSCRIEN: Descriptor Loaded Interrupt Enable**

0: Transfer descriptor loaded interrupt is enabled.

1: Transfer descriptor loaded interrupt is disabled.

- **VADDIEN: Add Head Descriptor to Queue Interrupt Enable**

0: Transfer descriptor added to queue interrupt is enabled.

1: Transfer descriptor added to queue interrupt is enabled.

- **VDONEIEN: End of List Interrupt Enable**

0: End of list interrupt is disabled.

1: End of list interrupt is enabled.

32.7.136High End Overlay Layer Configuration 41 Register

Name: LCDC_HEOCFG41

Address: 0xF0030430

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	YPHIDEF		
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	XPHIDEF		

- **XPHIDEF: Horizontal Filter Phase Offset**

XPHIDEF defines the index of the first coefficient set used when the horizontal resampling operation is started.

- **YPHIDEF: Vertical Filter Phase Offset**

XPHIDEF defines the index of the first coefficient set used when the vertical resampling operation is started.

- **INTDIS_DMA: Interrupt Disables DMA**

If set, when an enabled endpoint-originated interrupt is triggered, the DMA request is disabled regardless of the UDPHS_IEN register EPT_x bit for this endpoint. Then, the firmware will have to clear or disable the interrupt source or clear this bit if transfer completion is needed.

If the exception raised is associated with the new system bank packet, then the previous DMA packet transfer is normally completed, but the new DMA packet transfer is not started (not requested).

If the exception raised is not associated to a new system bank packet (ex: ERR_FL_ISO), then the request cancellation may happen at any time and may immediately stop the current DMA transfer.

This may be used, for example, to identify or prevent an erroneous packet to be transferred into a buffer or to complete a DMA buffer by software after reception of a short packet, or to perform buffer truncation on ERR_FL_ISO interrupt for adaptive rate.

- **DATAX_RX: DATAx Interrupt Enabled (Only for High Bandwidth Isochronous OUT endpoints)**

0: No effect.

1: Send an interrupt when a DATA2, DATA1 or DATA0 packet has been received meaning the whole microframe data payload has been received.

- **MDATA_RX: MDATA Interrupt Enabled (Only for High Bandwidth Isochronous OUT endpoints)**

0: No effect.

1: Send an interrupt when an MDATA packet has been received and so at least one packet of the microframe data payload has been received.

- **ERR_OVFLW: Overflow Error Interrupt Enabled**

0: Overflow Error Interrupt is masked.

1: Overflow Error Interrupt is enabled.

- **RXRDY_TXKL: Received OUT Data Interrupt Enabled**

0: Received OUT Data Interrupt is masked.

1: Received OUT Data Interrupt is enabled.

- **TX_COMPLT: Transmitted IN Data Complete Interrupt Enabled**

0: Transmitted IN Data Complete Interrupt is masked.

1: Transmitted IN Data Complete Interrupt is enabled.

- **TXRDY_TRER: TX Packet Ready/Transaction Error Interrupt Enabled**

0: TX Packet Ready/Transaction Error Interrupt is masked.

1: TX Packet Ready/Transaction Error Interrupt is enabled.

Caution: Interrupt source is active as long as the corresponding UDPHS_EPTSTAx register TXRDY_TRER flag remains low. If there are no more banks available for transmitting after the software has set UDPHS_EPTSTAx/TXRDY_TRER for the last transmit packet, then the interrupt source remains inactive until the first bank becomes free again to transmit at UDPHS_EPTSTAx/TXRDY_TRER hardware clear.

- **ERR_FL_ISO: Error Flow Interrupt Enabled**

0: Error Flow Interrupt is masked.

1: Error Flow Interrupt is enabled.

- **ERR_CRC_NTR: ISO CRC Error/Number of Transaction Error Interrupt Enabled**

0: ISO CRC error/number of Transaction Error Interrupt is masked.

1: ISO CRC error/number of Transaction Error Interrupt is enabled.

- **ERR_FLUSH: Bank Flush Error Interrupt Enabled**

0: Bank Flush Error Interrupt is masked.

1: Bank Flush Error Interrupt is enabled.

- **BUSY_BANK: Busy Bank Interrupt Enabled**

0: BUSY_BANK Interrupt is masked.

1: BUSY_BANK Interrupt is enabled.

For OUT endpoints: An interrupt is sent when all banks are busy.

For IN endpoints: An interrupt is sent when all banks are free.

- **SHRT_PCKT: Short Packet Interrupt Enabled**

For OUT endpoints: send an Interrupt when a Short Packet has been received.

0: Short Packet Interrupt is masked.

1: Short Packet Interrupt is enabled.

For IN endpoints: a Short Packet transmission is guaranteed upon end of the DMA Transfer, thus signaling an end of isochronous (micro-)frame data, but only if the UDPHS_DMACONTROLx register END_B_EN and UDPHS_EPTCTLx register AUTO_VALID bits are also set.

36.7.39 Octets Transmitted [31:0] Register

Name: GMAC_OTLO

Address: 0xF0028100

Access: Read-only

31	30	29	28	27	26	25	24
TXO							

23	22	21	20	19	18	17	16
TXO							

15	14	13	12	11	10	9	8
TXO							

7	6	5	4	3	2	1	0
TXO							

When reading the Octets Transmitted and Octets Received Registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

- **TXO: Transmitted Octets**

Transmitted octets in frame without errors [31:0]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

37.6.25 User Input/Output Register

Name: EMAC_USRIO

Address: 0xF802C0C0

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	CLKEN	RMII

- **RMII: Reduce MII**

When set, this bit enables the RMII operation mode.

- **CLKEN: Clock Enable**

When set, this bit enables the transceiver input clock.

Setting this bit to 0 reduces power consumption when the treasurer is not used.

37.6.27.9 Late Collisions Register

Name: EMAC_LCOL

Address: 0xF802C05C

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
LCOL							

- **LCOL: Late Collisions**

An 8-bit register counting the number of frames that experience a collision after the slot time (512 bits) has expired. A late collision is counted twice; i.e., both as a collision and a late collision.

–SCSIZE must be set according to the value of HSMCI_DMA, CHKSIZE field.

–BTSIZE is programmed with *block_length[1:0].* (last 1, 2, or 3 bytes of the buffer).

14. Configure the fields of LLI_B.DMAC_CTRLBx as follows:

–DST_INCR is set to INCR

–SRC_INCR is set to INCR

–FC field is programmed with peripheral to memory flow control mode.

–Both SRC_DSCR and DST_DSCR are set to 1 (descriptor fetch is disabled) or Next descriptor location points to 0.

–DIF and SIF are set with their respective layer ID. If SIF is different from DIF, DMA Controller is able to prefetch data and write HSMCI simultaneously.

15. Configure the LLI_B.DMAC_CFGx memory location for Channel x as follows:

–FIFOCFG defines the watermark of the DMA channel FIFO.

–SRC_H2SEL is set to true to enable hardware handshaking on the destination.

–SRC_PER is programmed with the hardware handshaking ID of the targeted HSMCI Host Controller.

16. Program LLI_B.DMAC_DSCR with 0.
17. Program the DMAC_CTRLBx register for Channel x with 0. Its content is updated with the LLI fetch operation.
18. Program DMAC_DSCRx with the address of LLI_W if *block_length* greater than 4 else with address of LLI_B.
19. Enable Channel x writing one to DMAC_CHER[x]. The DMAC is ready and waiting for request.

3. Wait for XFRDONE in the HSMCI_SR.

38.8.6.3 Block Length is Not Multiple of 4, with Padding Value (ROPT field in HSMCI_DMA register set to 1)

When the ROPT field is set to one, The DMA Controller performs only WORD access on the bus to transfer a non-multiple of 4 block length. Unlike previous flow, in which the transfer size is rounded to the nearest multiple of 4.

1. Program the HSMCI Interface, see previous flow.
   - ROPT field is set to 1.
2. Program the DMA Controller
   1. Read the channel register to choose an available (disabled) channel.
   2. Clear any pending interrupts on the channel from the previous DMA transfer by reading the DMAC_EBCISR.
   3. Program the channel registers.
   4. The DMAC_SADDRx register for Channel x must be set with the starting address of the HSMCI_FIFO address.
   5. The DMAC_DADDRx register for Channel x must be word aligned.
   6. Configure the fields of DMAC_CTRLAx for Channel x as follows:

   –DST_WIDTH is set to WORD

   –SRC_WIDTH is set to WORD

   –SCSIZE must be set according to the value of HSMCI_DMA.CHKSIZE Field.

   –BTSIZE is programmed with *CEILING(block_length/4).*

   7. Configure the fields of DMAC_CTRLBx for Channel x as follows:

   –DST_INCR is set to INCR

   –SRC_INCR is set to INCR

   –FC field is programmed with peripheral to memory flow control mode.

- **DTOE: Data Time-out Error**

0: No error.

1: The data time-out set by DTOCYC and DTOMUL in HSMCI_DTOR has been exceeded. Cleared by reading in the HSMCI_SR.

- **CSTOE: Completion Signal Time-out Error**

0: No error.

1: The completion signal time-out set by CSTOCYC and CSTOMUL in HSMCI_CSTOR has been exceeded. Cleared by reading in the HSMCI_SR. Cleared by reading in the HSMCI_SR.

- **BLKOVRE: DMA Block Overrun Error**

0: No error.

1: A new block of data is received and the DMA controller has not started to move the current pending block, a block overrun is raised. Cleared by reading in the HSMCI_SR.

- **DMADONE: DMA Transfer done**

0: DMA buffer transfer has not completed since the last read of the HSMCI_SR.

1: DMA buffer transfer has completed.

- **FIFOEMPTY: FIFO empty flag**

0: FIFO contains at least one byte.

1: FIFO is empty.

- **XFRDONE: Transfer Done flag**

0: A transfer is in progress.

1: Command Register is ready to operate and the data bus is in the idle state.

- **ACKRCV: Boot Operation Acknowledge Received**

0: No Boot acknowledge received since the last read of the status register.

1: A Boot acknowledge signal has been received. Cleared by reading the HSMCI_SR.

- **ACKRCVE: Boot Operation Acknowledge Error**

0: No error

1: Corrupted Boot Acknowledge signal received.

- **OVRE: Overrun**

0: No error.

1: At least one 8-bit received data has been lost (not read). Cleared when sending a new data transfer command.

When FERRCTRL in HSMCI_CFG is set to 1, OVRE becomes reset after read.

- **UNRE: Underrun**

0: No error.

1: At least one 8-bit data has been sent without valid information (not written). Cleared when sending a new data transfer command or when setting FERRCTRL in HSMCI_CFG to 1.

When FERRCTRL in HSMCI_CFG is set to 1, UNRE becomes reset after read.

- **BLKOVRE: DMA Block Overrun Error Interrupt Disable**
- **DMADONE: DMA Transfer completed Interrupt Disable**
- **FIFOEMPTY: FIFO empty Interrupt Disable**
- **XFRDONE: Transfer Done Interrupt Disable**
- **ACKRCV: Boot Acknowledge Interrupt Disable**
- **ACKRCVE: Boot Acknowledge Error Interrupt Disable**
- **OVRE: Overrun Interrupt Disable**
- **UNRE: Underrun Interrupt Disable**

44.8.6 USART Interrupt Enable Register (SPI_MODE)

Name: US_IER (SPI_MODE)

Address: 0xF001C008 (0), 0xF0020008 (1), 0xF8020008 (2), 0xF8024008 (3)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	UNRE	TXEMPTY	–
7	6	5	4	3	2	1	0
–	–	OVRE	–	–	–	TXRDY	RXRDY

This configuration is relevant only if USART_MODE = 0xE or 0xF in “USART Mode Register” on page 1407.

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Enables the corresponding interrupt.

- **RXRDY: RXRDY Interrupt Enable**
- **TXRDY: TXRDY Interrupt Enable**
- **OVRE: Overrun Error Interrupt Enable**
- **TXEMPTY: TXEMPTY Interrupt Enable**
- **UNRE: SPI Underrun Error Interrupt Enable**

  - “PWM Channel Period Register” on page 1612
  - “PWM Channel Period Update Register” on page 1613
- Register group 4:
  - “PWM Channel Dead Time Register” on page 1615
  - “PWM Channel Dead Time Update Register” on page 1616
- Register group 5:
  - “PWM Fault Mode Register” on page 1594
  - “PWM Fault Protection Value Register” on page 1597

52.5.2 TDES Mode Register

Name: TDES_MR

Address: 0xF803C004

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	CFBS	
15	14	13	12	11	10	9	8
LOD	–	OPMOD		–	–	SMOD	
7	6	5	4	3	2	1	0
–	–	–	KEYMOD	–	–	TDESMOD	CIPHER

- **CIPHER: Processing Mode**

0 (DECRYPT): Decrypts data.

1 (ENCRYPT): Encrypts data.

- **TDESMOD: ALGORITHM mode**

0 (SINGLE_DES): Single DES processing using TDES_KEY1WRx registers.

1 (TRIPLE_DES): Triple DES processing using registers TDES_KEY1WRx, TDES_KEY2WRx and TDES_KEY3WRx if KEYMOD is set.

- **KEYMOD: Key Mode**

0: Three-key algorithm is selected.

1: Two-key algorithm is selected. There is no need to write TDES_KEY3WRx registers.

- **SMOD: Start Mode**

Value	Name	Description
0x0	MANUAL_START	Manual Mode
0x1	AUTO_START	Auto Mode
0x2	IDATAR0_START	TDES_IDATAR0 access only Auto Mode

Values which are not listed in the table must be considered as “reserved”.

If a DMA transfer is used, 0x2 must be configured. Refer to Section 52.4.3.2 ”DMA Mode” for more details.

- **OPMOD: Operation Mode**

Value	Name	Description
0x0	ECB	ECB: Electronic Code Book mode
0x1	CBC	CBC: Cipher Block Chaining mode
0x2	OFB	OFB: Output Feedback mode
0x3	CFB	CFB: Cipher Feedback mode

For CBC-MAC operating mode, please set OPMOD to CBC and LOD to 1.

The OFB and CFB modes of operation are only available if 2-key mode is selected (KEYMOD=1).