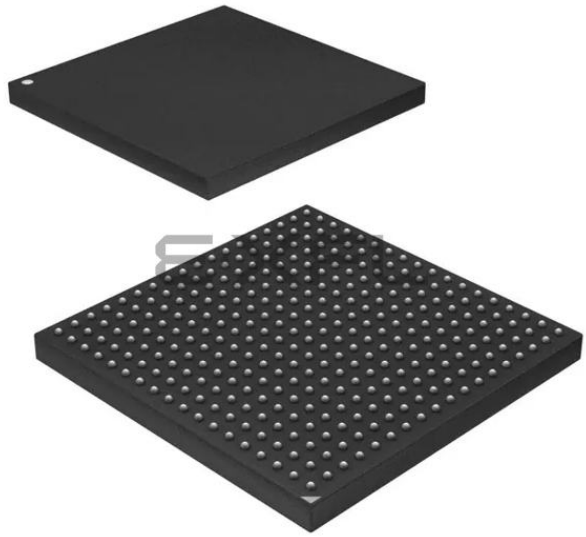

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

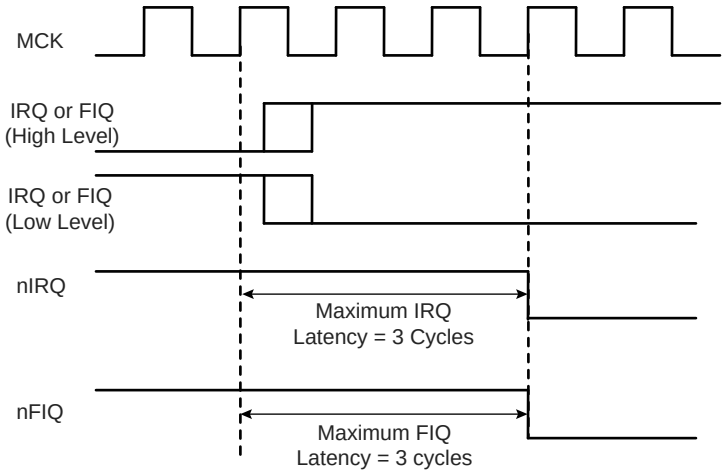
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	536MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	324-LFBGA
Supplier Device Package	324-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d36a-cur

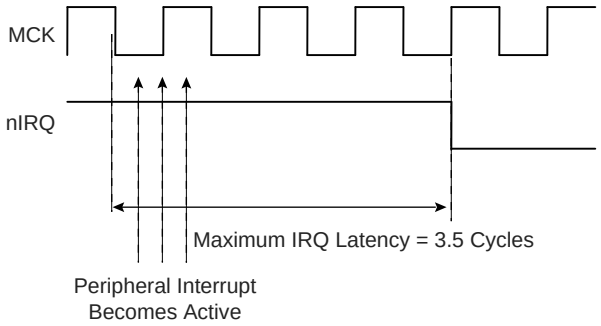
17.8.2.3 Internal Interrupt Edge Triggered Source

Figure 17-8. Internal Interrupt Edge Triggered Source



17.8.2.4 Internal Interrupt Level Sensitive Source

Figure 17-9. Internal Interrupt Level Sensitive Source



17.8.3 Normal Interrupt

17.8.3.1 Priority Controller

An 8-level priority controller drives the nIRQ line of the processor, depending on the interrupt conditions occurring on the interrupt sources 1 to 127 (except for those programmed in Fast Forcing).

Each interrupt source has a programmable priority level of 7 to 0, which is user-definable by writing the PRIOR field of the AIC_SMR (Source Mode Register). Level 7 is the highest priority and level 0 the lowest.

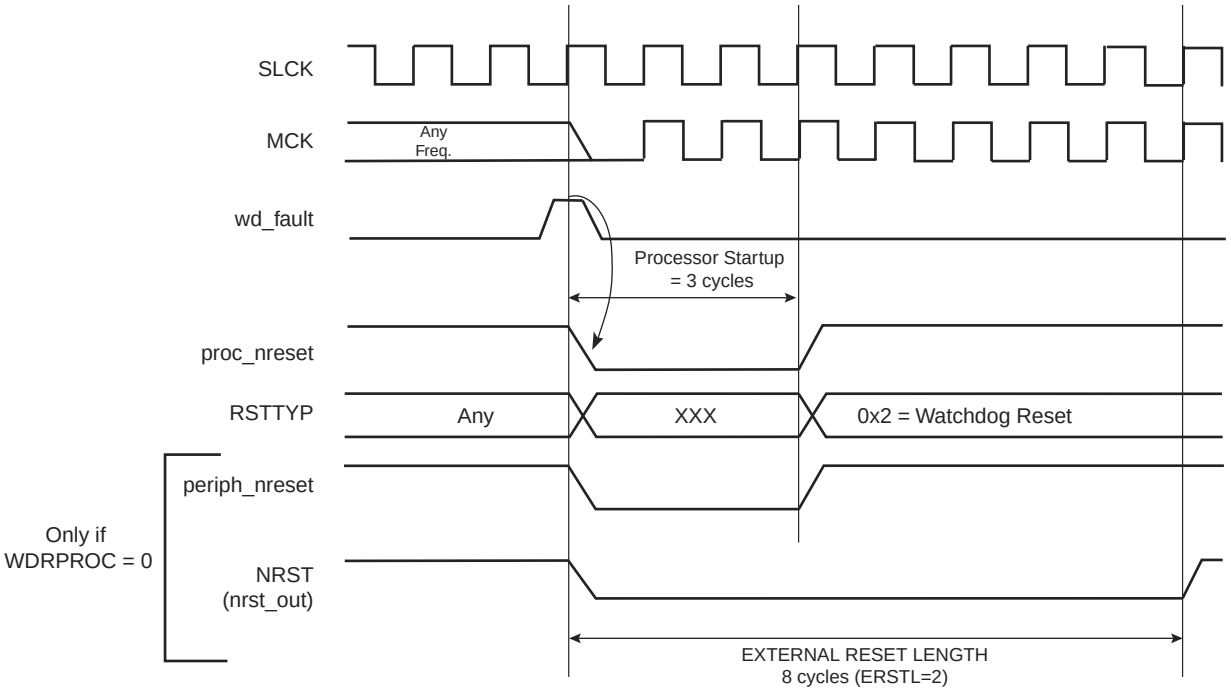
As soon as an interrupt condition occurs, as defined by the SRCTYPE field of the AIC_SMR (Source Mode Register), the nIRQ line is asserted. As a new interrupt condition might have happened on other interrupt sources since the nIRQ has been asserted, the priority controller determines the current interrupt at the time the AIC_IVR (Interrupt Vector Register) is read. The read of AIC_IVR is the entry point of the interrupt handling which allows the AIC to consider that the interrupt has been taken into account by the software.

The current priority level is defined as the priority level of the current interrupt.

If several interrupt sources of equal priority are pending and enabled when the AIC_IVR is read, the interrupt with the lowest interrupt source number is serviced first.

The nIRQ line can be asserted only if an interrupt condition occurs on an interrupt source with a higher priority. If an interrupt condition happens (or is pending) during the interrupt treatment in progress, it is delayed until the software

Figure 19-8. Watchdog Reset



19.4.5 Reset State Priorities

The Reset State Manager manages the following priorities between the different reset sources, given in descending order:

- Backup Reset
- Wake-up Reset
- User Reset
- Watchdog Reset
- Software Reset

Particular cases are listed below:

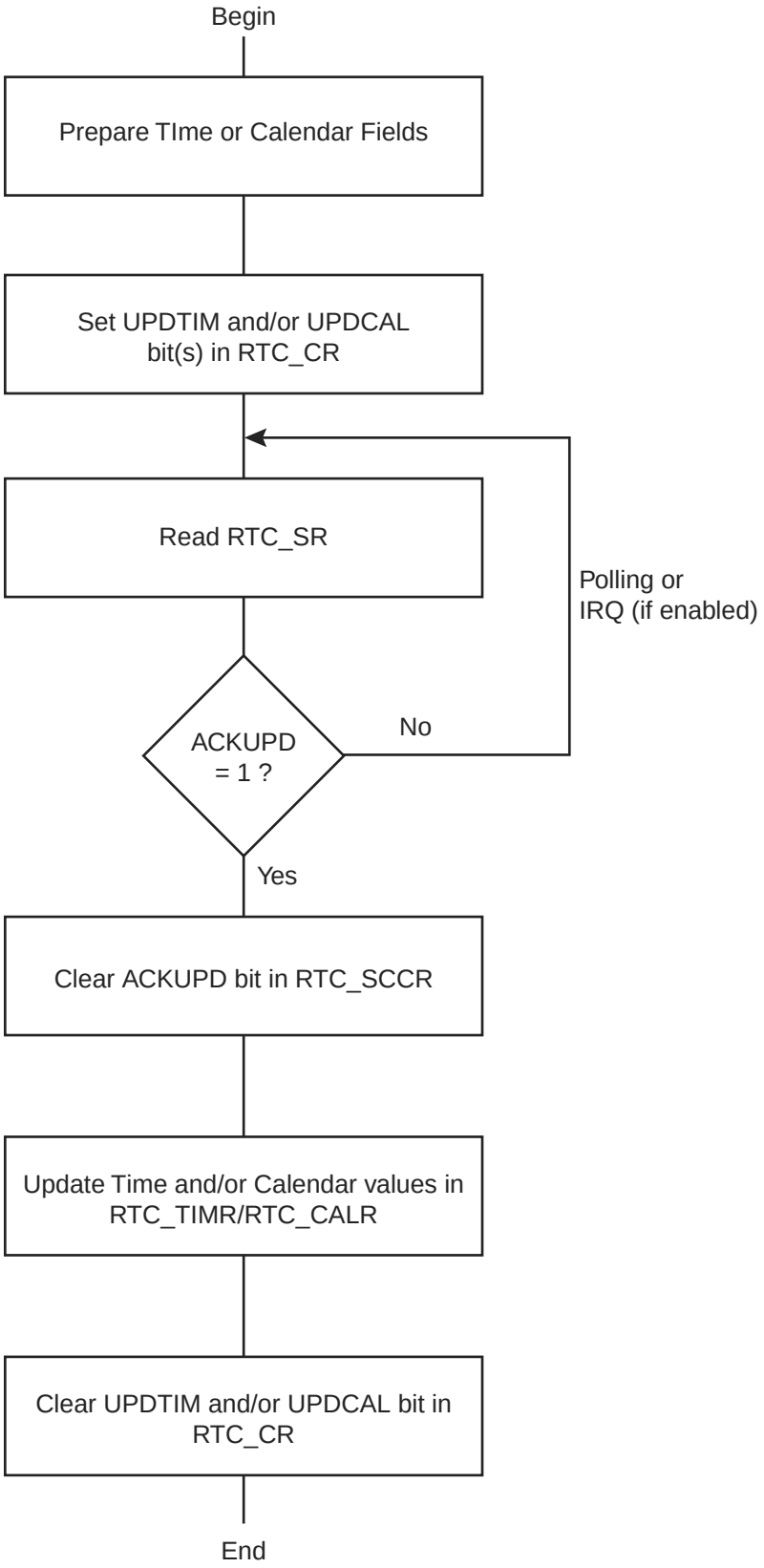
- When in User Reset:
  - A watchdog event is impossible because the Watchdog Timer is being reset by the proc_nreset signal.
  - A software reset is impossible, since the processor reset is being activated.
- When in Software Reset:
  - A watchdog event has priority over the current state.
  - The NRST has no effect.
- When in Watchdog Reset:
  - The processor reset is active and so a Software Reset cannot be programmed.
  - A User Reset cannot be entered.

19.4.6 Reset Controller Status Register

The Reset Controller Status Register (RSTC_SR) provides several status fields:

- RSTTYP field: This field gives the type of the last reset, as explained in previous sections.
- SRCMP bit: This bit indicates that a Software Reset Command is in progress and that no further software reset should be performed until the end of the current one. This bit is automatically cleared at the end of the current software reset.
- NRSTL bit: This bit gives the level of the NRST pin sampled on each MCK rising edge.

Figure 23-2. Update Sequence



The Master Clock is main clock divided by 16.

The Processor Clock is the Master Clock.

9. Selecting Programmable Clocks

   Programmable clocks are controlled via registers; PMC_SCER, PMC_SCDR and PMC_SCSR.

   Programmable clocks can be enabled and/or disabled via the PMC_SCER and PMC_SCDR. 3 programmable clocks can be used. The PMC_SCSR indicates which programmable clock is enabled. By default all programmable clocks are disabled.

   PMC_PCKx registers are used to configure programmable clocks.

   The CSS field is used to select the programmable clock divider source. Five clock options are available: main clock, slow clock, master clock, PLLACK, UPLLCK. The slow clock is the default clock source.

   The PRES field is used to control the programmable clock prescaler. It is possible to choose between different values (1, 2, 4, 8, 16, 32, 64). Programmable clock output is prescaler input divided by PRES parameter. By default, the PRES value is set to 0 which means that PCKx is equal to slow clock.

   Once the PMC_PCKx register has been configured, The corresponding programmable clock must be enabled and the user is constrained to wait for the PCKRDYx bit to be set in the PMC_SR. This can be done either by polling PCKRDYx in the PMC_SR or by waiting for the interrupt line to be raised if the associated interrupt source (PCKRDYx) has been enabled in the PMC_IER. All parameters in PMC_PCKx can be programmed in a single write operation.

   If the CSS and PRES parameters are to be modified, the corresponding programmable clock must be disabled first. The parameters can then be modified. Once this has been done, the user must re-enable the programmable clock and wait for the PCKRDYx bit to be set.

10. Enabling Peripheral Clocks

    Once all of the previous steps have been completed, the peripheral clocks can be enabled and/or disabled via registers PMC_PCERx and PMC_PCDRx.

26.2.13 Clock Switching Details

26.2.13.1 Master Clock Switching Timings

Table 26-1 and Table 26-2 give the worst case timings required for the Master Clock to switch from one selected clock to another one. This is in the event that the prescaler is de-activated. When the prescaler is activated, an additional time of 64 clock cycles of the new selected clock has to be added.

Table 26-1. Clock Switching Timings (Worst Case)

To	From		
	Main Clock	**SLCK**	**PLL Clock**
Main Clock	–	4 x SLCK + 2.5 x Main Clock	3 x PLL Clock + 4 x SLCK + 1 x Main Clock
SLCK	0.5 x Main Clock + 4.5 x SLCK	–	3 x PLL Clock + 5 x SLCK
PLL Clock	0.5 x Main Clock + 4 x SLCK + PLLCOUNT x SLCK + 2.5 x PLLx Clock	2.5 x PLL Clock + 5 x SLCK + PLLCOUNT x SLCK	2.5 x PLL Clock + 4 x SLCK + PLLCOUNT x SLCK

Notes: 1. PLL designates either the PLLA or the UPLL Clock.

2. PLLCOUNT designates either PLLACOUNT or UPLLCOUNT.

31.8.14 DMAC Channel x [x = 0..7] Destination Address Register

Name: DMAC_DADDRx [x = 0..7]

Address: 0xFFFFE640 (0)[0], 0xFFFFE668 (0)[1], 0xFFFFE690 (0)[2], 0xFFFFE6B8 (0)[3], 0xFFFFE6E0 (0)[4], 0xFFFFE708 (0)[5], 0xFFFFE730 (0)[6], 0xFFFFE758 (0)[7], 0xFFFFE840 (1)[0], 0xFFFFE868 (1)[1], 0xFFFFE890 (1)[2], 0xFFFFE8B8 (1)[3], 0xFFFFE8E0 (1)[4], 0xFFFFE908 (1)[5], 0xFFFFE930 (1)[6], 0xFFFFE958 (1)[7]

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
DADDR							

23	22	21	20	19	18	17	16
DADDR							

15	14	13	12	11	10	9	8
DADDR							

7	6	5	4	3	2	1	0
DADDR							

This register can only be written if the WPEN bit is cleared in “DMAC Write Protect Mode Register” .

- **DADDR: Channel x Destination Address**

This register must be aligned with the destination transfer width.

32.7.64 Overlay 2 Layer Control Register

Name: LCDC_OVRCTRL2

Address: 0xF0030264

Access: Read-Write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	DONEIEN	ADDIEN	DSCRIEN	DMAIEN	LFETCH	DFETCH

- **DFETCH: Transfer Descriptor Fetch Enable**

0: Transfer Descriptor fetch is disabled.

1: Transfer Descriptor fetch is enabled.

- **LFETCH: Lookup Table Fetch Enable**

0: Lookup Table DMA fetch is disabled.

1: Lookup Table DMA fetch is enabled.

- **DMAIEN: End of DMA Transfer Interrupt Enable**

0: DMA transfer completed interrupt is enabled.

1: DMA transfer completed interrupt is disabled.

- **DSCRIEN: Descriptor Loaded Interrupt Enable**

0: Transfer descriptor loaded interrupt is enabled.

1: Transfer descriptor loaded interrupt is disabled.

- **ADDIEN: Add Head Descriptor to Queue Interrupt Enable**

0: Transfer descriptor added to queue interrupt is enabled.

1: Transfer descriptor added to queue interrupt is enabled.

- **DONEIEN: End of List Interrupt Enable**

0: End of list interrupt is disabled.

1: End of list interrupt is enabled.

32.7.65 Overlay 2 Layer Next Register

Name: LCDC_OVRNEXT2

Address: 0xF0030268

Access: Read-Write

Reset: 0x00000000

31	30	29	28	27	26	25	24
NEXT							
23	22	21	20	19	18	17	16
NEXT							
15	14	13	12	11	10	9	8
NEXT							
7	6	5	4	3	2	1	0
NEXT							

- **NEXT: DMA Descriptor Next Address**

The transfer descriptor address must be aligned on a 64-bit boundary.

- **UDONE: End of List Interrupt for U or UV Chrominance Component Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **UOVR: Overflow Interrupt for U or UV Chrominance Component Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **VDMA: End of DMA Transfer for V Chrominance Component Interrupt Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **VDSCR: Descriptor Loaded for V Chrominance Component Interrupt Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **VADD: Head Descriptor Loaded for V Chrominance Component Interrupt Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **VDONE: End of List for V Chrominance Component Interrupt Disable Register**

0: No effect.

1: Interrupt source is disabled.

- **VOVR: Overflow for V Chrominance Component Interrupt Disable Register**

0: No effect.

1: Interrupt source is disabled.

32.7.140Hardware Cursor Layer Interrupt Enable Register

Name: LCDC_HCRIER

Address: 0xF003044C

Access: Write-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	OVR	DONE	ADD	DSCR	DMA	–	–

- **DMA: End of DMA Transfer Interrupt Enable Register**

0: No effect.

1: Interrupt source is enabled.

- **DSCR: Descriptor Loaded Interrupt Enable Register**

0: No effect.

1: Interrupt source is enabled.

- **ADD: Head Descriptor Loaded Interrupt Enable Register**

0: No effect.

1: Interrupt source is enabled.

- **DONE: End of List Interrupt Enable Register**

0: No effect.

1: Interrupt source is enabled.

- **OVR: Overflow Interrupt Enable Register**

0: No effect.

1: Interrupt source is enabled.

32.7.171Post Processing Layer Configuration 3 Register

Name: LCDC_PPCFG3

Address: 0xF0030578

Access: Read-Write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	CSCYOFF	CSCYB					
23	22	21	20	19	18	17	16
CSCYB				CSCYG			
15	14	13	12	11	10	9	8
CSCYG						CSCYR	
7	6	5	4	3	2	1	0
CSCYR							

- **CSCYR: Color Space Conversion R coefficient for Luminance component, signed format, step set to 1/1024**

Color Space Conversion coefficient format is 1 sign bit, 9 fractional bits.

- **CSCYG: Color Space Conversion G coefficient for Luminance component, signed format, step set to 1/512**

Color Space Conversion coefficient format is 1 sign bit, 9 fractional bits.

- **CSCYB: Color Space Conversion B coefficient for Luminance component, signed format, step set to 1/1024**

Color Space Conversion coefficient format is 1 sign bit, 9 fractional bits.

- **CSCYOFF: Color Space Conversion Luminance Offset**

0: The *Yoff* parameter value is set to 0.

1: The *Yoff* parameter value is set to 16.

32.7.175Overlay 1 CLUT Register x Register

Name: LCDC_OVR1CLUTx [x=0..255]

Address: 0xF0030A00

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
ACLUT							
23	22	21	20	19	18	17	16
RCLUT							
15	14	13	12	11	10	9	8
GCLUT							
7	6	5	4	3	2	1	0
BCLUT							

- **BCLUT: Blue Color entry**

This field indicates the 8-bit width Blue color of the color lookup table.

- **GCLUT: Green Color entry**

This field indicates the 8-bit width Green color of the color lookup table.

- **RCLUT: Red Color entry**

This field indicates the 8-bit width Red color of the color lookup table.

- **ACLUT: Alpha Color entry**

This field indicates the 8-bit width Alpha channel of the color lookup table.

33.5.23 DMA Codec Descriptor Address Register

Name: ISI_DMA_C_DSCR

Address: 0xF0034058

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
C_DSCR							
23	22	21	20	19	18	17	16
C_DSCR							
15	14	13	12	11	10	9	8
C_DSCR							
7	6	5	4	3	2	1	0
C_DSCR						–	–

- **C_DSCR: Codec Descriptor Base Address**

This address is word aligned.

34.7.3 UDPHS Interrupt Enable Register

Name: UDPHS_IEN

Address: 0xF8030010

Access: Read-write

31	30	29	28	27	26	25	24
DMA_7	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
EPT_15	EPT_14	EPT_13	EPT_12	EPT_11	EPT_10	EPT_9	EPT_8
15	14	13	12	11	10	9	8
EPT_7	EPT_6	EPT_5	EPT_4	EPT_3	EPT_2	EPT_1	EPT_0
7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	–

- **DET_SUSPD: Suspend Interrupt Enable**

0: Disable Suspend Interrupt.

1: Enable Suspend Interrupt.

- **MICRO_SOF: Micro-SOF Interrupt Enable**

0: Disable Micro-SOF Interrupt.

1: Enable Micro-SOF Interrupt.

- **INT_SOF: SOF Interrupt Enable**

0: Disable SOF Interrupt.

1: Enable SOF Interrupt.

- **ENDRESET: End Of Reset Interrupt Enable**

0: Disable End Of Reset Interrupt.

1: Enable End Of Reset Interrupt. Automatically enabled after USB reset.

- **WAKE_UP: Wake Up CPU Interrupt Enable**

0: Disable Wake Up CPU Interrupt.

1: Enable Wake Up CPU Interrupt.

- **ENDOFRSM: End Of Resume Interrupt Enable**

0: Disable Resume Interrupt.

1: Enable Resume Interrupt.

- **UPSTR_RES: Upstream Resume Interrupt Enable**

0: Disable Upstream Resume Interrupt.

1: Enable Upstream Resume Interrupt.

39.7.3.2 Master Mode Flow Diagram

Figure 39-6. Master Mode Flow Diagram

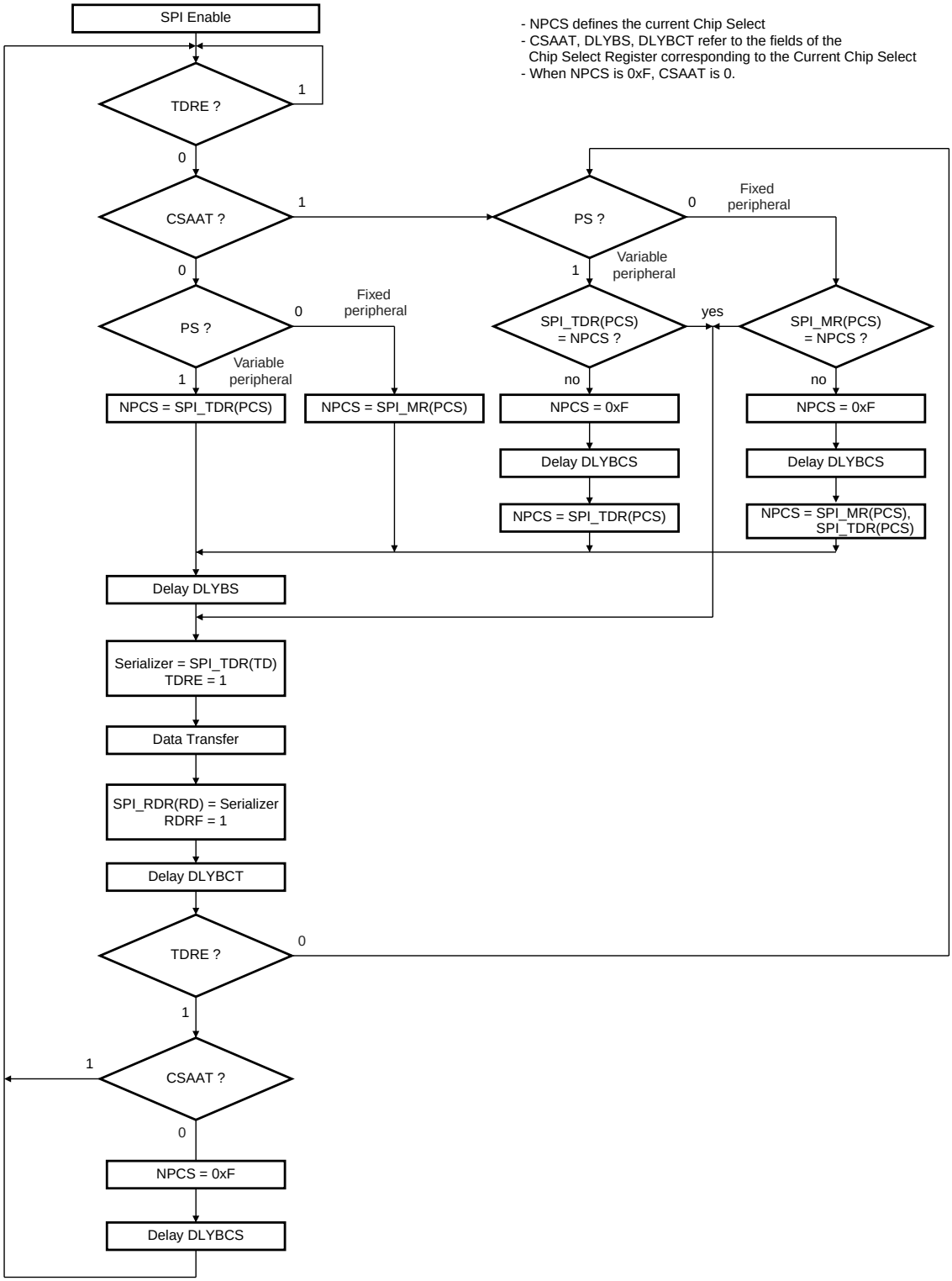
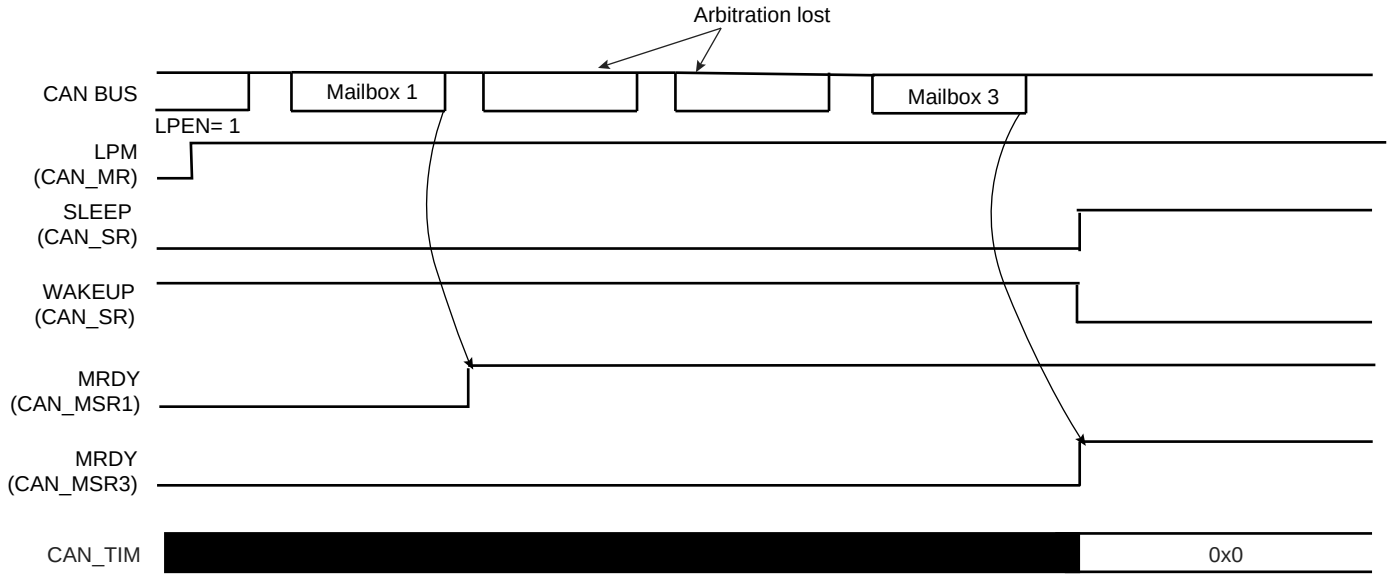


Figure 45-8. Enabling Low-power Mode



45.7.5.2 Disabling Low-power Mode

The CAN controller can be awake after detecting a CAN bus activity. Bus activity detection is done by an external module that may be embedded in the chip. When it is notified of a CAN bus activity, the software application disables Low-power Mode by programming the CAN controller.

To disable Low-power Mode, the software application must:

- Enable the CAN Controller clock. This is done by programming the Power Management Controller (PMC).
- Clear the LPM field in the CAN_MR

The CAN controller synchronizes itself with the bus activity by checking for eleven consecutive “recessive” bits. Once synchronized, the WAKEUP signal in the CAN_SR is set.

Depending on the corresponding mask in the CAN_IMR, an interrupt is generated while WAKEUP is set. The SLEEP signal in the CAN_SR is automatically cleared once WAKEUP is set. WAKEUP signal is automatically cleared once SLEEP is set.

If no message is being sent on the bus, then the CAN controller is able to send a message eleven bit times after disabling Low-power Mode.

If there is bus activity when Low-power mode is disabled, the CAN controller is synchronized with the bus activity in the next interframe. The previous message is lost (see Figure 45-9).

47.7.4 TC Stepper Motor Mode Register

Name: TC_SMMRx [x=0..2]

Address: 0xF0010008 (0)[0], 0xF0010048 (0)[1], 0xF0010088 (0)[2], 0xF8014008 (1)[0], 0xF8014048 (1)[1], 0xF8014088 (1)[2]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	DOWN	GCEN

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

- **GCEN: Gray Count Enable**

0: TIOAx [x=0..2] and TIOBx [x=0..2] are driven by internal counter of channel x.

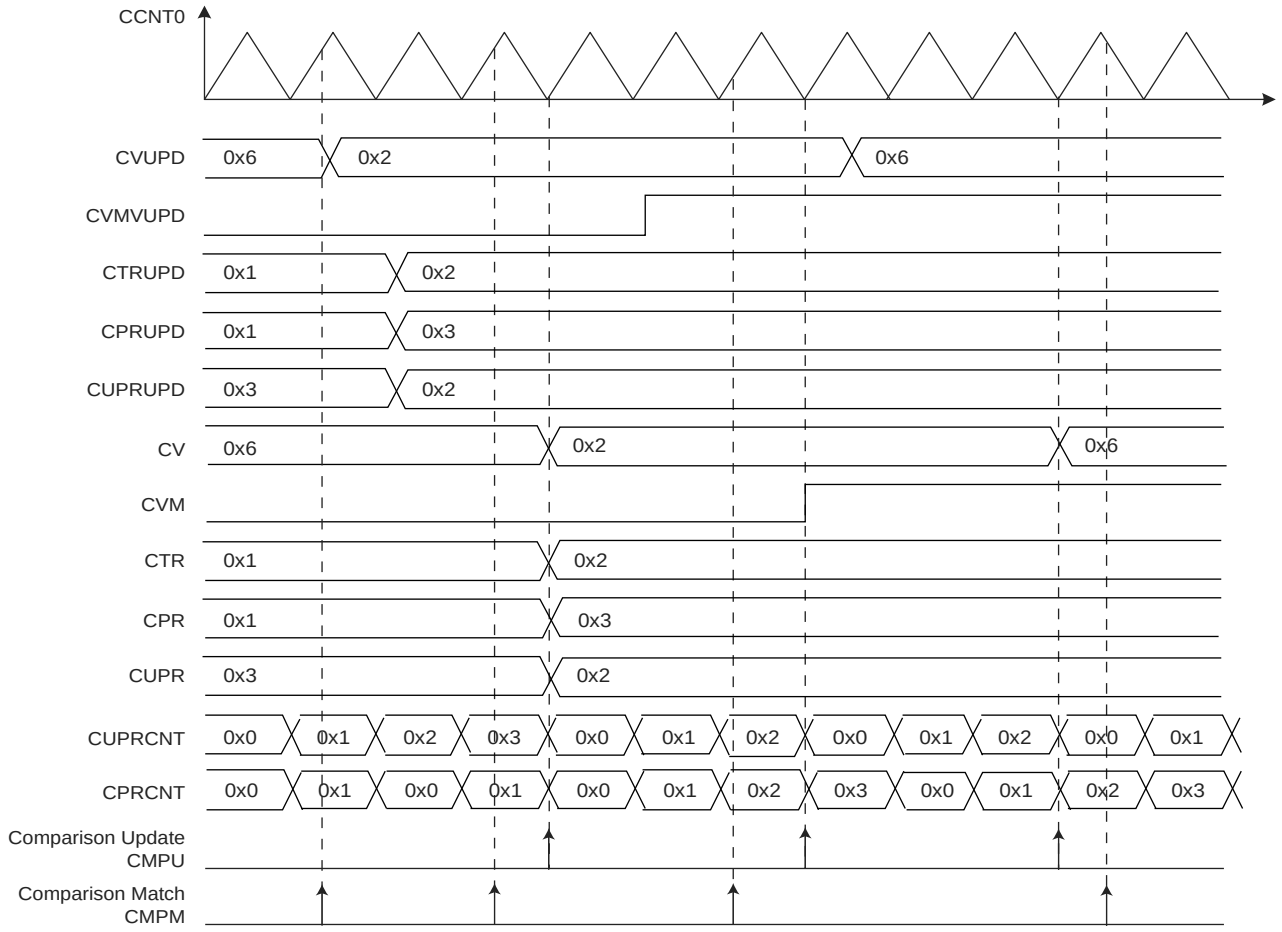
1: TIOAx [x=0..2] and TIOBx [x=0..2] are driven by a 2-bit gray counter.

- **DOWN: DOWN Count**

0: Up counter.

1: Down counter.

Figure 48-13.Comparison Waveform

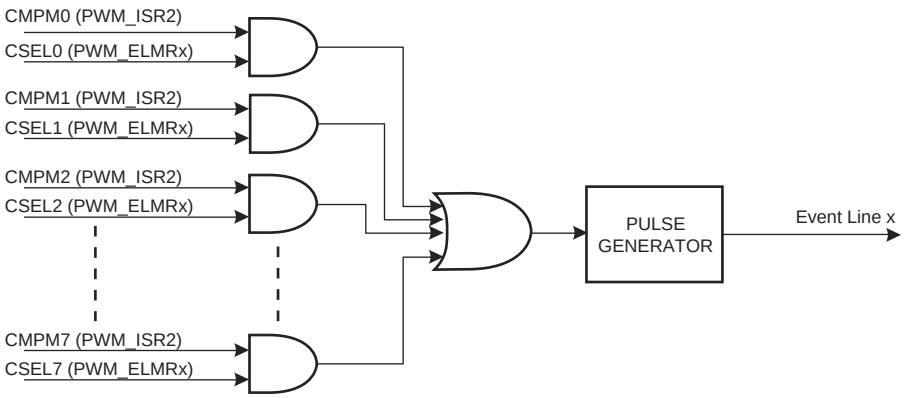


48.6.4 PWM Event Lines

The PWM provides 2 independent event lines intended to trigger actions in other peripherals (in particular for ADC (Analog-to-Digital Converter)).

A pulse (one cycle of the master clock (MCK)) is generated on an event line, when at least one of the selected comparisons is matching. The comparisons can be selected or unselected independently by the CSEL bits in the “PWM Event Line x Register” (PWM_ELMRx for the Event Line x).

Figure 48-14.Event Line Block Diagram



48.7.37 PWM Channel Duty Cycle Register

Name: PWM_CDTYx [x=0..3]

Address: 0xF002C204 [0], 0xF002C224 [1], 0xF002C244 [2], 0xF002C264 [3]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
CDTY							

15	14	13	12	11	10	9	8
CDTY							

7	6	5	4	3	2	1	0
CDTY							

Only the first 16 bits (channel counter size) are significant.

- **CDTY: Channel Duty-Cycle**

Defines the waveform duty-cycle. This value must be defined between 0 and CPRD (PWM_CPRx).

Doc. Rev. 11121B	Comments	Change Request Ref.
	Mechanical Characteristics: Added “Nominal Ball Diameter” and “Solder” rows in Table 55-4 “Package Information”.	 rfo
	Errata: Added the introduction paragraph in Section 57. “SAMA5D3 Series Errata”. Added Section 57.1.2 “Boot ROM: NAND Flash Detection using ONFI Parameters does Not Work”.	 rfo 8785

Doc. Rev. 11121A	Comments	Change Request Ref.
	First Issue	