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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf13k50t-i-so

REGISTER 2-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-x
—	—	—	—	—	PRI_SD	HFIOFL	LFIOFS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	q = depends on condition
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **PRI_SD:** Primary Oscillator Drive Circuit shutdown bit
1 = Oscillator drive circuit on
0 = Oscillator drive circuit off (zero power)

bit 1 **HFIOFL:** HFINTOSC Frequency Locked bit
1 = HFINTOSC is in lock
0 = HFINTOSC has not yet locked

bit 0 **LFIOFS:** LFINTOSC Frequency Stable bit
1 = LFINTOSC is stable
0 = LFINTOSC is not stable

2.6.1 OSCTUNE REGISTER

The HFINTOSC is factory calibrated, but can be adjusted in software by writing to the TUN<5:0> bits of the OSCTUNE register (Register 2-3).

The default value of the TUN<5:0> is '000000'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift, while giving no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. The operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

The OSCTUNE register also implements the INTSRC and SPLLEN bits, which control certain features of the internal oscillator block.

The INTSRC bit allows users to select which internal oscillator provides the clock source when the 31 kHz frequency option is selected. This is covered in greater detail in **Section 2.5.1 "LFINTOSC"**.

The SPLLEN bit controls the operation of the frequency multiplier. For more details about the function of the SPLLEN bit see **Section 2.9 "4x Phase Lock Loop Frequency Multiplier"**.

REGISTER 2-3: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	SPLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INTSRC:** Internal Oscillator Low-Frequency Source Select bit
1 = 31.25 kHz device clock derived from 16 MHz HFINTOSC source (divide-by-512 enabled)
0 = 31 kHz device clock derived directly from LFINTOSC internal oscillator

bit 6 **SPLLEN:** Software Controlled Frequency Multiplier PLL bit
1 = PLL enabled (for HFINTOSC 8 MHz only)
0 = PLL disabled

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
011111 = Maximum frequency
011110 =
• • •
000001 =
000000 = Oscillator module is running at the factory calibrated frequency.
111111 =
• • •
100000 = Minimum frequency

TABLE 2-4: LOW-SPEED USB CLOCK SETTINGS

Clock Mode	Clock Frequency	USBDIV	4x PLL Enabled	CPUDIV<1:0>	System Clock Frequency (MHz)
EC High/HS	12 MHz	1	Yes	00	48
				01	24
				10	16
				11	12
			No	00	12
				01	6
				10	4
				11	3
	6 MHz	0	Yes	00	24
				01	12
				10	8
				11	6
			No	00	6
				01	3
				10	2
				11	1.5

Note: The system clock frequency in Table 2-4 only applies if the OSCCON register bits SCS<1:0> = 00. By changing these bits, the system clock can operate down to 31 kHz.

TABLE 2-5: FULL-SPEED USB CLOCK SETTINGS

Clock Mode	Clock Frequency	4x PLL Enabled	CPUDIV<1:0>	System Clock Frequency (MHz)
EC High	48 MHz	No	00	48
			01	24
			10	16
			11	12
EC High/HS	12 MHz	Yes	00	48
			01	24
			10	16
			11	12

Note: The system clock frequency in the above table only applies if the OSCCON register bits SCS<1:0> = 00. By changing these bits, the system clock can operate down to 31 kHz.

7.8 RCON Register

The RCON register contains flag bits which are used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the IPEN bit which enables interrupt priorities.

The operation of the SBOREN bit and the Reset flag bits is discussed in more detail in **Section 23.1 "RCON Register"**.

REGISTER 7-10: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	SBOREN(1)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$(2)	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 **SBOREN:** BOR Software Enable bit(1)
If BOREN<1:0> = 01:
1 = BOR is enabled
0 = BOR is disabled
If BOREN<1:0> = 00, 10 or 11:
Bit is disabled and read as '0'.

bit 5 **Unimplemented:** Read as '0'

bit 4 **$\overline{RI}$:** RESET Instruction Flag bit
1 = The RESET instruction was not executed (set by firmware or Power-on Reset)
0 = The RESET instruction was executed causing a device Reset (must be set in firmware after a code-executed Reset occurs)

bit 3 **$\overline{TO}$:** Watchdog Time-out Flag bit
1 = Set by power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 2 **$\overline{PD}$:** Power-down Detection Flag bit
1 = Set by power-up or by the CLRWDT instruction
0 = Set by execution of the SLEEP instruction

bit 1 **$\overline{POR}$:** Power-on Reset Status bit(2)
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit(3)
1 = A Brown-out Reset has not occurred (set by firmware only)
0 = A Brown-out Reset occurred (must be set by firmware after a POR or Brown-out Reset occurs)

Note 1: If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'.
2: The actual Reset value of $\overline{POR}$ is determined by the type of device Reset. See the notes following this register and **Section 23.6 "Reset State of Registers"** for additional information.
3: See Table 23-3.

14.4 PWM (Enhanced Mode)

The Enhanced PWM Mode can generate a PWM signal on up to four different output pins with up to ten bits of resolution. It can do this through four different PWM output modes:

- Single PWM
- Half-Bridge PWM
- Full-Bridge PWM, Forward mode
- Full-Bridge PWM, Reverse mode

To select an Enhanced PWM mode, the P1M bits of the CCP1CON register must be set appropriately.

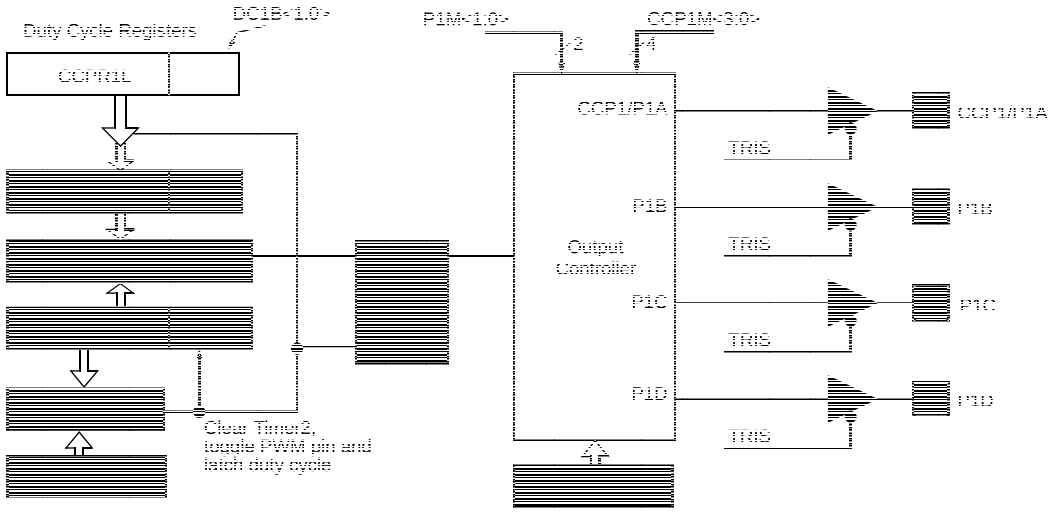
The PWM outputs are multiplexed with I/O pins and are designated P1A, P1B, P1C and P1D. The polarity of the PWM pins is configurable and is selected by setting the CCP1M bits in the CCP1CON register appropriately.

Table 14-2 shows the pin assignments for each Enhanced PWM mode.

Figure 14-3 shows an example of a simplified block diagram of the Enhanced PWM module.

Note:	To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

FIGURE 14-3: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE



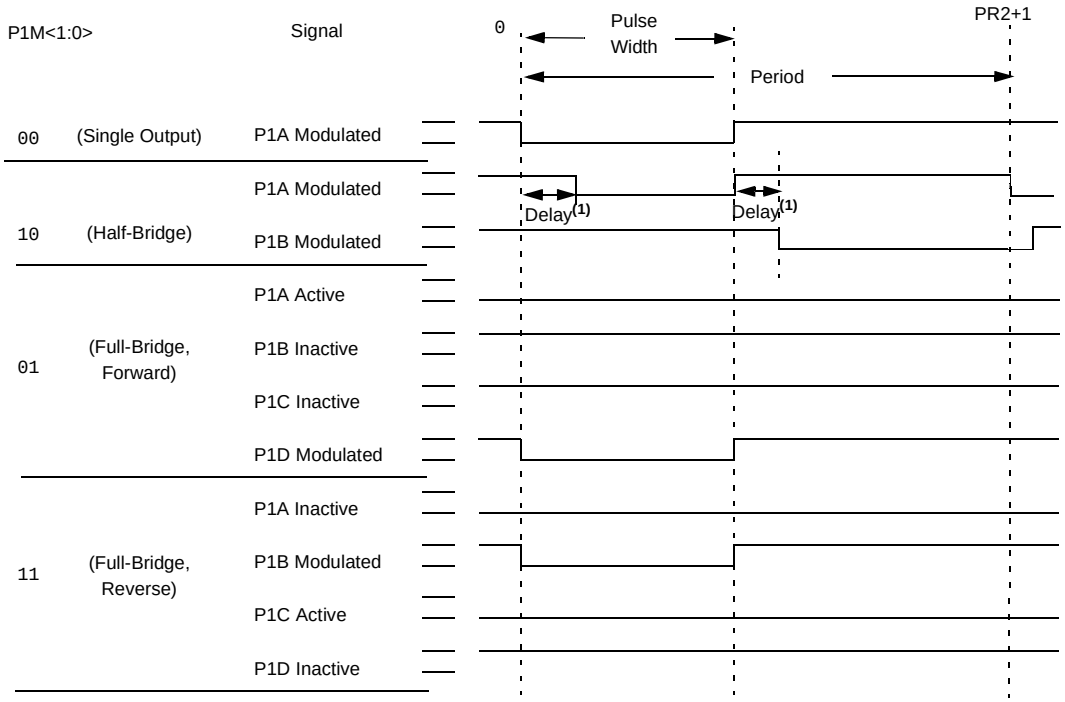
Note 1:	The TRIS register value for each PWM output must be configured appropriately.
2:	Any pin not used by an Enhanced PWM mode is available for alternate pin functions.

TABLE 14-2: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	P1M<1:0>	CCP1/P1A	P1B	P1C	P1D
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: Outputs are enabled by pulse steering in Single mode. See Register 14-4.

FIGURE 14-5: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



Relationships:

- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

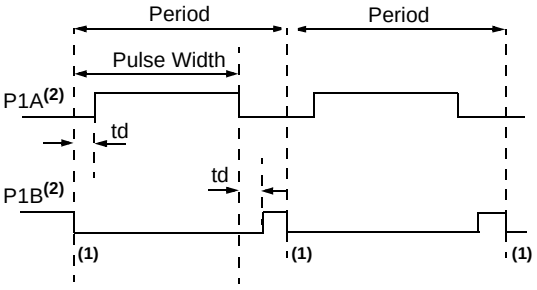
Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 14.4.6 "Programmable Dead-Band Delay mode"**).

14.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In Half-Bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (shoot-through current) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 14-14 for illustration. The lower seven bits of the associated PWM1CON register (Register 14-3) sets the delay period in terms of microcontroller instruction cycles (T_{CY} or 4 T_{OSC}).

FIGURE 14-14: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

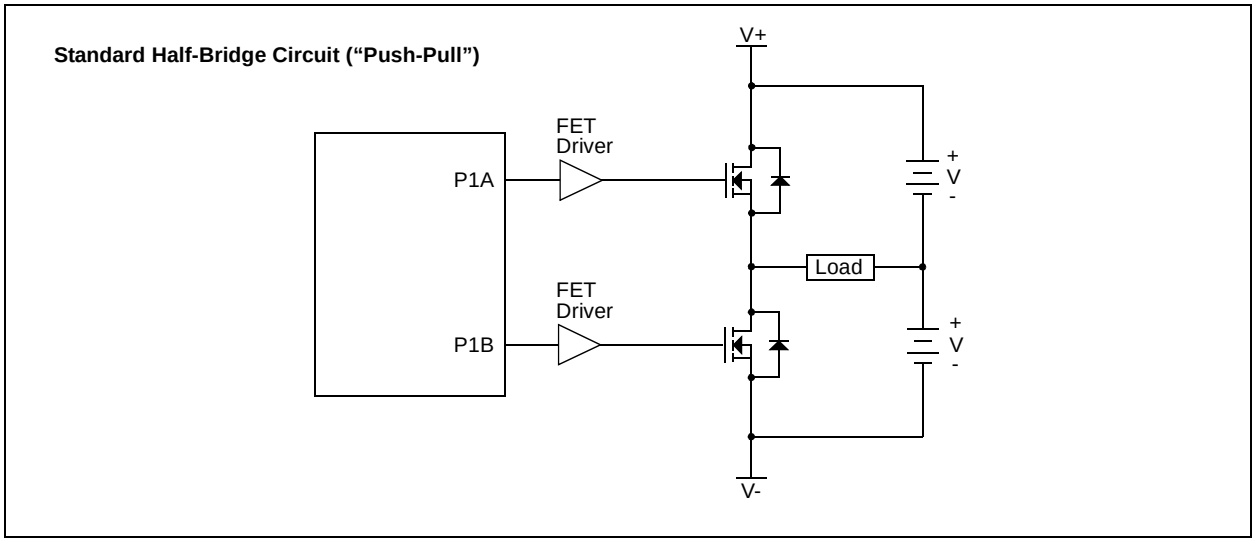


td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.

FIGURE 14-15: EXAMPLE OF HALF-BRIDGE APPLICATIONS



14.4.8 OPERATION IN POWER-MANAGED MODES

In Sleep mode, all clock sources are disabled. Timer2 will not increment and the state of the module will not change. If the ECCP pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state. If Two-Speed Start-ups are enabled, the initial start-up frequency from HFINTOSC and the postscaler may not be stable immediately.

In PRI_IDLE mode, the primary clock will continue to clock the ECCP module without change. In all other power-managed modes, the selected power-managed mode clock will clock Timer2. Other power-managed mode clocks will most likely be different than the primary clock frequency.

14.4.8.1 Operation with Fail-Safe Clock Monitor

If the Fail-Safe Clock Monitor is enabled, a clock failure will force the device into the RC_RUN Power-Managed mode and the OSCFIF bit of the PIR2 register will be set. The ECCP will then be clocked from the internal oscillator clock source, which may have a different clock frequency than the primary clock.

See the previous section for additional details.

14.4.9 EFFECTS OF A RESET

Both Power-on Reset and subsequent Resets will force all ports to Input mode and the CCP registers to their Reset states.

This forces the enhanced CCP module to reset to a state compatible with the standard CCP module.

17.1.6 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital Conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared by software.

Note:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the Interrupt Service Routine. Please see **Section 17.1.6 "Interrupts"** for more information.

TABLE 17-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (TAD)		Device Frequency (FOSC)			
ADC Clock Source	**ADCS<2:0>**	**48 MHz**	**16 MHz**	**4 MHz**	**1 MHz**
FOSC/2	000	41.67 ns(2)	125 ns(2)	500 ns(2)	2.0 μs
FOSC/4	100	83.33 ns(2)	250 ns(2)	1.0 μs	4.0 μs
FOSC/8	001	167 ns(2)	500 ns(2)	2.0 μs	8.0 μs(3)
FOSC/16	101	333 ns(2)	1.0 μs	4.0 μs	16.0 μs(3)
FOSC/32	010	667 ns(2)	2.0 μs	8.0 μs(3)	32.0 μs(3)
FOSC/64	110	1.33 μs	4.0 μs	16.0 μs(3)	64.0 μs(3)
FRC	x11	1-4 μs(1,4)	1-4 μs(1,4)	1-4 μs(1,4)	1-4 μs(1,4)

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 1.7 μs.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

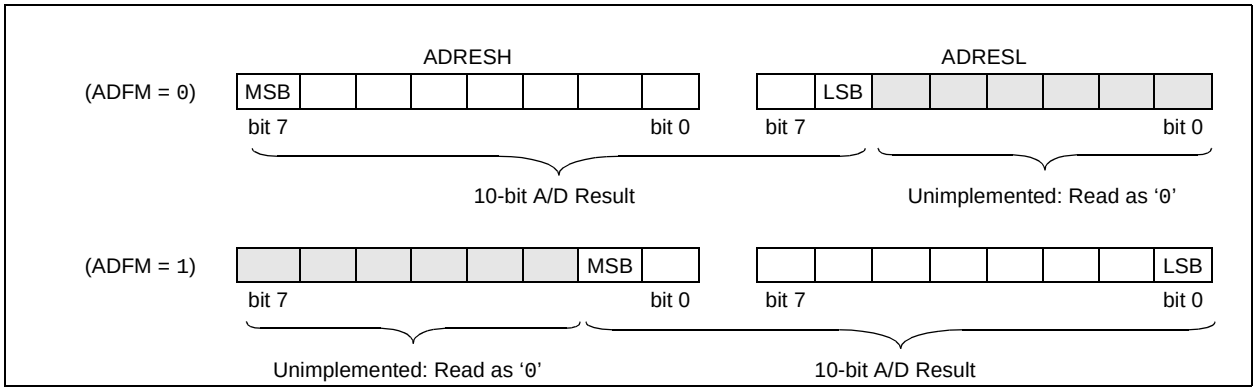
4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

17.1.7 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON2 register controls the output format.

Figure 17-2 shows the two output formats.

FIGURE 17-2: 10-BIT A/D CONVERSION RESULT FORMAT



17.2.10 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

Note:	Analog pin control is performed by the ANSEL and ANSELH registers. For ANSEL and ANSELH registers, see Register 9-15 and Register 9-16, respectively.

REGISTER 17-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-2 **CHS<3:0>: Analog Channel Select bits**

0000 = Reserved
0001 = Reserved
0010 = Reserved
0011 = AN3
0100 = AN4
0101 = AN5
0110 = AN6
0111 = AN7
1000 = AN8
1001 = AN9
1010 = AN10
1011 = AN11
1100 = Reserved
1101 = Reserved
1110 = DAC
1111 = FVR

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

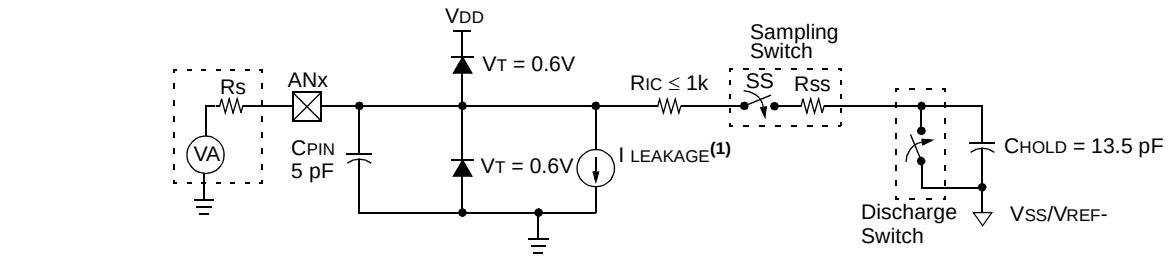
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

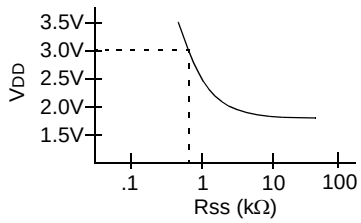
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: Selecting reserved channels will yield unpredictable results as unimplemented input channels are left floating.

FIGURE 17-5: ANALOG INPUT MODEL

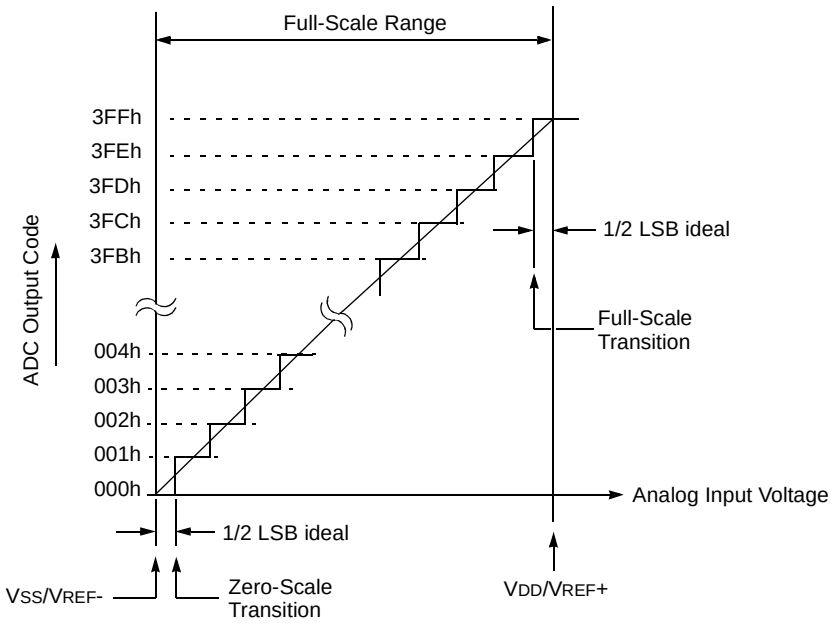


Legend: CPIN = Input Capacitance
VT = Threshold Voltage
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance



Note 1: See **Section 27.0 "Electrical Specifications"**.

FIGURE 17-6: ADC TRANSFER FUNCTION



19.5.3 EXIT BY RESET

Exiting Sleep and Idle modes by Reset causes code execution to restart at address 0. See **Section 23.0 "Reset"** for more details.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator. Exit delays are summarized in Table 19-2.

19.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode, where the primary clock source is not stopped and
- the primary clock source is not any of the LP, XT, HS or HSPLL modes.

In these instances, the primary clock source either does not require an oscillator start-up delay since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (RC, EC, INTOSC, and INTOSCIO modes). However, a fixed delay of interval TCSD following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 19-2: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Clock Source before Wake-up	Clock Source after Wake-up	Exit Delay	Clock Ready Status Bit (OSCCON)
Primary Device Clock (PRI_IDLE mode)	LP, XT, HS	T_{CSD}(1)	OSTS
	HSPLL		
	EC, RC		
	HFINTOSC(2)		IOSF
T1OSC or LFINTOSC(1)	LP, XT, HS	T_{OST}(3)	OSTS
	HSPLL	$T_{OST} + t_{PLL}$(3)	
	EC, RC	T_{CSD}(1)	
	HFINTOSC(1)	T_{IOBST}(4)	IOSF
HFINTOSC(2)	LP, XT, HS	T_{OST}(4)	OSTS
	HSPLL	$T_{OST} + t_{PLL}$(3)	
	EC, RC	T_{CSD}(1)	
	HFINTOSC(1)	None	IOSF
None (Sleep mode)	LP, XT, HS	T_{OST}(3)	OSTS
	HSPLL	$T_{OST} + t_{PLL}$(3)	
	EC, RC	T_{CSD}(1)	
	HFINTOSC(1)	T_{IOBST}(4)	IOSF

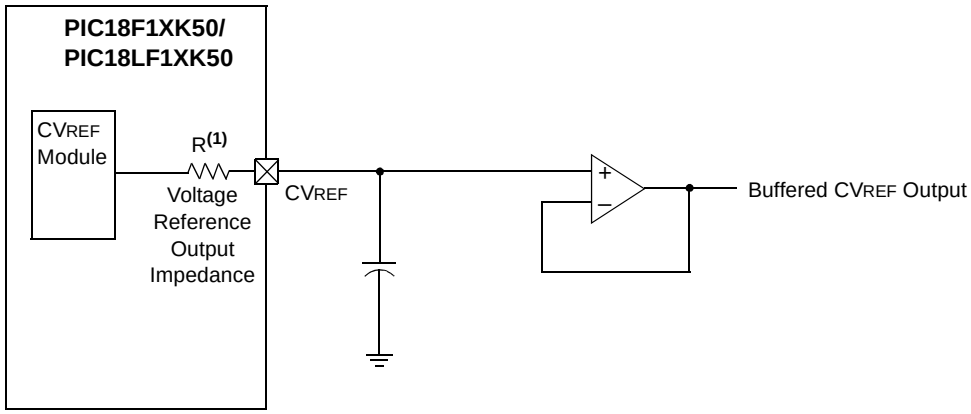
Note 1: TCSD is a required delay when waking from Sleep and all Idle modes and runs concurrently with any other required delays (see **Section 19.4 "Idle Modes"**). On Reset, HFINTOSC defaults to 1 MHz.

2: Includes both the HFINTOSC 16 MHz source and postscaler derived frequencies.

3: TOST is the Oscillator Start-up Timer. t_{PLL} is the PLL Lock-out Timer (parameter F12).

4: Execution continues during the HFINTOSC stabilization period, TIOBST.

FIGURE 21-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the voltage reference Configuration bits, CVR<3:0> and CVRR.

REGISTER 21-1: REFCON0: REFERENCE CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-1	U-0	U-0	U-0	U-0
FVR1EN	FVR1ST	FVR1S1	FVR1S0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **FVR1EN:** Fixed Voltage Reference 1 Enable bit
0 = FVR is disabled
1 = FVR is enabled

bit 6 **FVR1ST:** Fixed Voltage Reference 1 Stable bit
0 = FVR is not stable
1 = FVR is stable

bit 5-4 **FVR1S<1:0>:** Fixed Voltage Reference 1 Voltage Select bits
00 = Reserved, do not use
01 = 1.024V (x1)
10 = 2.048V (x2)
11 = 4.096V (x4)

bit 3-0 **Unimplemented:** Read as ‘0’

23.0 RESET

The PIC18(L)F1XK50 devices differentiate between various kinds of Reset:

a) Power-on Reset (POR)
b) $\overline{\text{MCLR}}$ Reset during normal operation
c) $\overline{\text{MCLR}}$ Reset during power-managed modes
d) Watchdog Timer (WDT) Reset (during execution)
e) Programmable Brown-out Reset (BOR)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset

This section discusses Resets generated by $\overline{\text{MCLR}}$, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in **Section 3.1.2.4 "Stack Full and Underflow Resets"**. WDT Resets are covered in **Section 24.2 "Watchdog Timer (WDT)"**.

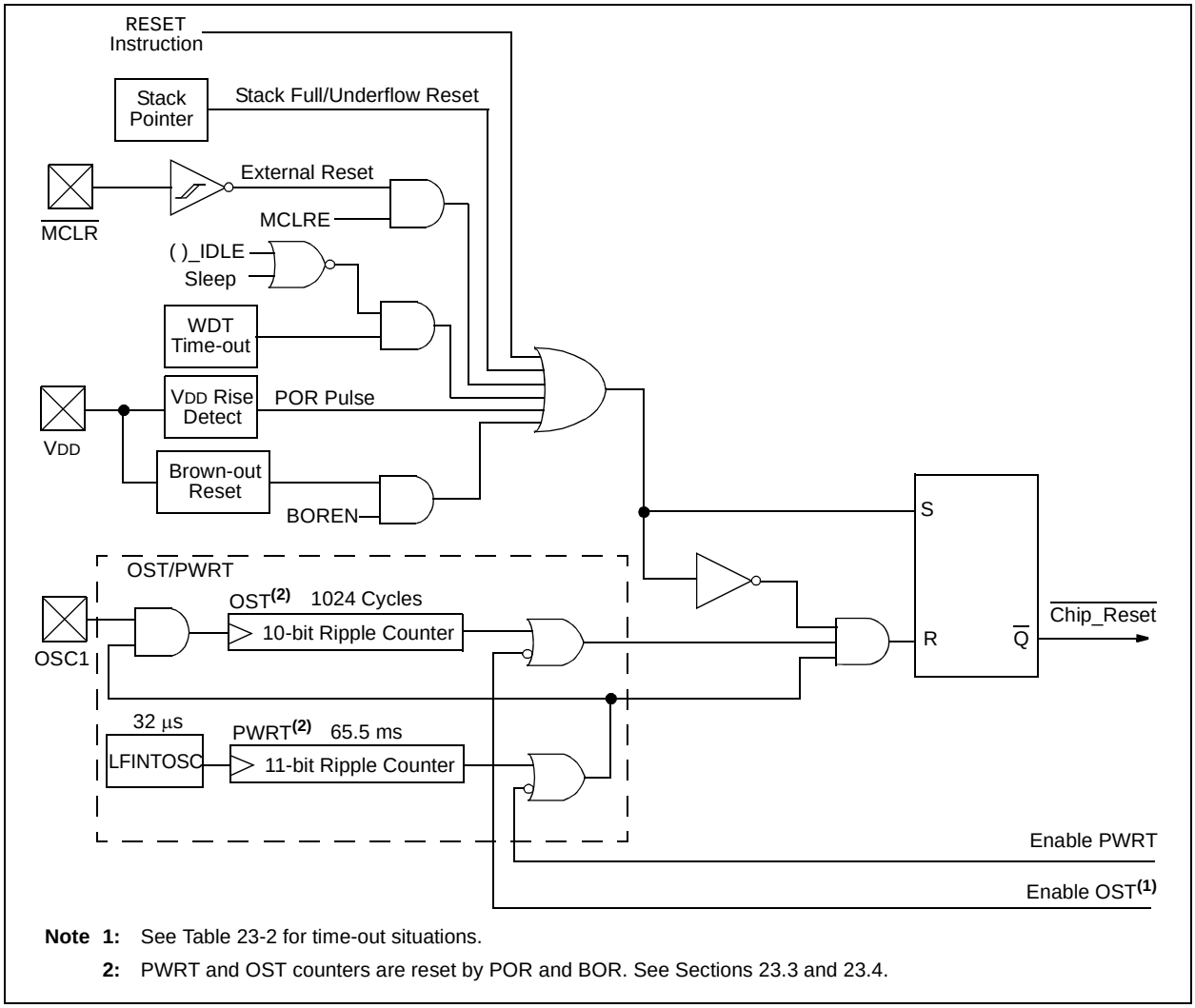
A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 23-1.

23.1 RCON Register

Device Reset events are tracked through the RCON register (Register 23-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 23.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in **Section 7.0 "Interrupts"**. BOR is covered in **Section 23.4 "Brown-out Reset (BOR)"**.

FIGURE 23-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: See Table 23-2 for time-out situations.

2: PWRT and OST counters are reset by POR and BOR. See Sections 23.3 and 23.4.

FIGURE 24-2: CODE-PROTECTED PROGRAM MEMORY FOR PIC18(L)F1XK50

<table>
<tr><td rowspan="3">Address (from/to)</td><td colspan="4">Device</td></tr>
<tr><td colspan="2">14K50</td><td colspan="2">13K50</td></tr>
<tr><td>BBSIZ = 1</td><td>BBSIZ = 0</td><td>BBSIZ = 1</td><td>BBSIZ = 0</td></tr>
<tr><td>0000h
01FFh</td><td rowspan="4">Boot Block, 2 KW
CPB, WRTB, EBTRB</td><td rowspan="2">Boot Block, 1 KW
CPB, WRTB, EBTRB</td><td rowspan="2">Boot Block, 1 KW
CPB, WRTB, EBTRB</td><td>Boot Block, 0.512 KW
CPB, WRTB, EBTRB</td></tr>
<tr><td>0200h
03FFh</td><td rowspan="3">Block 0
1.512 KW
CP0, WRT0, EBTR0</td></tr>
<tr><td>0400h
05FFh</td><td rowspan="3">Block 0
3 KW
CP0, WRT0, EBTR0</td><td rowspan="2">Block 0
1 KW
CP0, WRT0, EBTR0</td></tr>
<tr><td>0600h
07FFh</td></tr>
<tr><td>0800h
0FFFh</td><td>Block 0
2 KW
CP0, WRT0, EBTR0</td><td>Block 1
2 KW
CP1, WRT1, EBTR1</td><td>Block 1
2 KW
CP1, WRT1, EBTR1</td></tr>
<tr><td>1000h
1FFFh</td><td>Block 1
4 KW
CP1, WRT1, EBTR1</td><td>Block 1
4 KW
CP1, WRT1, EBTR1</td><td rowspan="19">Reads all ‘0’s</td><td rowspan="19">Reads all ‘0’s</td></tr>
<tr><td>2000h
27FFh</td><td rowspan="18">Reads all ‘0’s</td><td rowspan="18">Reads all ‘0’s</td></tr>
<tr><td>2800h
2FFFh</td></tr>
<tr><td>3000h
37FFh</td></tr>
<tr><td>3800h
3FFFh</td></tr>
<tr><td>4000h
47FFh</td></tr>
<tr><td>4800h
4FFFh</td></tr>
<tr><td>5000h
57FFh</td></tr>
<tr><td>5800h
5FFFh</td></tr>
<tr><td>6000h
67FFh</td></tr>
<tr><td>6800h
6FFFh</td></tr>
<tr><td>7000h
77FFh</td></tr>
<tr><td>7800h
7FFFh</td></tr>
<tr><td>8000h
FFFFh</td></tr>
</table>

Note: Refer to the test section for requirements on test memory mapping.

POP **Pop Top of Return Stack**

Syntax: POP

Operands: None

Operation: (TOS) → bit bucket

Status Affected: None

Encoding:

0000	0000	0000	0110

Description: The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	POP TOS value	No operation

Example:

```
POP
GOTO    NEW
```

Before Instruction
TOS = 0031A2h
Stack (1 level down) = 014332h
After Instruction
TOS = 014332h
PC = NEW

PUSH **Push Top of Return Stack**

Syntax: PUSH

Operands: None

Operation: (PC + 2) → TOS

Status Affected: None

Encoding:

0000	0000	0000	0101

Description: The PC + 2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing a software stack by modifying TOS and then pushing it onto the return stack.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	PUSH PC + 2 onto return stack	No operation	No operation

Example:

```
PUSH
```

Before Instruction
TOS = 345Ah
PC = 0124h
After Instruction
PC = 0126h
TOS = 0126h
Stack (1 level down) = 345Ah

TABLE 27-5: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
		Internal Program Memory Programming Specifications(1)					
D110	VPP	Voltage on $\overline{\text{MCLR}}$/VPP/RA3 pin	8	—	9	V	**(Note 3, Note 4)**
D113	IDDP	Supply Current during Programming	—	—	10	mA	
		Data EEPROM Memory(2)					
D120	ED	Byte Endurance	100K	—	—	E/W	-40°C to +85°C
D121	VDRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V	Using EECON to read/write
D122	TDEW	Erase/Write Cycle Time	—	3	4	ms	
D123	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(2)	1M	10M	—	E/W	-40°C to +85°C
D130		**Program Flash Memory**					
	EP	Cell Endurance	10k	—	—	E/W	Temperature during programming: 10°C ≤ TA ≤ 40°C
D131	VPR	VDD for Read	VDDMIN	—	VDDMAX	V	
D131A		Voltage on $\overline{\text{MCLR}}$/VPP during Erase/Program	8.0	—	9.0	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
D131B	VBE	VDD for Bulk Erase	2.7	—	VDDMAX	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
D132	VPEW	VDD for Write or Row Erase	2.2 VDDMIN	— —	VDDMAX VDDMAX	V	PIC18LF1XK50 PIC18F1XK50
D132A	IPPPGM	Current on $\overline{\text{MCLR}}$/VPP during Erase/Write	—	1.0	—	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
D132B	IDDPGM	Current on VDD during Erase/Write	—	5.0	—	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
D133	TPEW	Erase/Write cycle time	—	2.0	2.8	ms	Temperature during programming: 10°C ≤ TA ≤ 40°C
D134	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

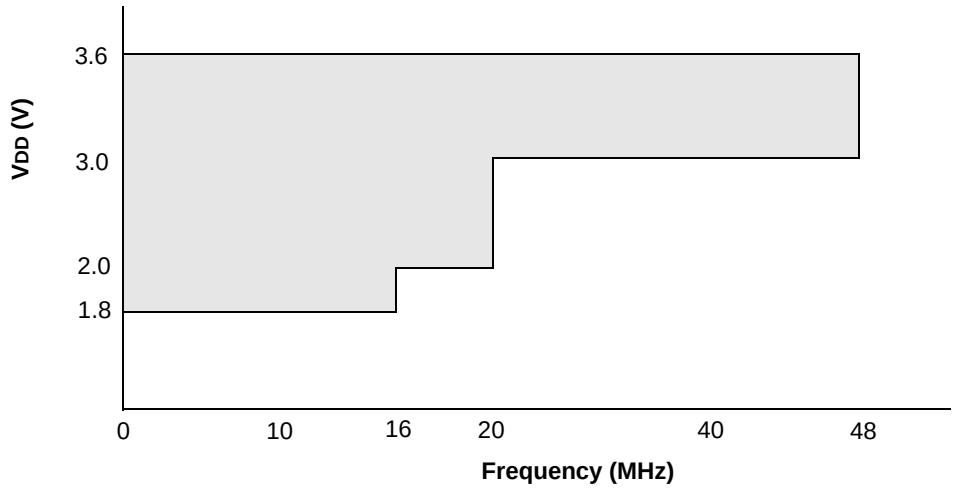
Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: Refer to **Section 5.8 "Using the Data EEPROM"** for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

4: The MPLAB ICD 2 does not support variable VPP output. Circuitry to limit the ICD 2 VPP voltage must be placed between the ICD 2 and target system when programming or debugging with the ICD 2.

FIGURE 27-5: PIC18LF1XK50 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 27-8 for each Oscillator mode's supported frequencies.

FIGURE 27-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

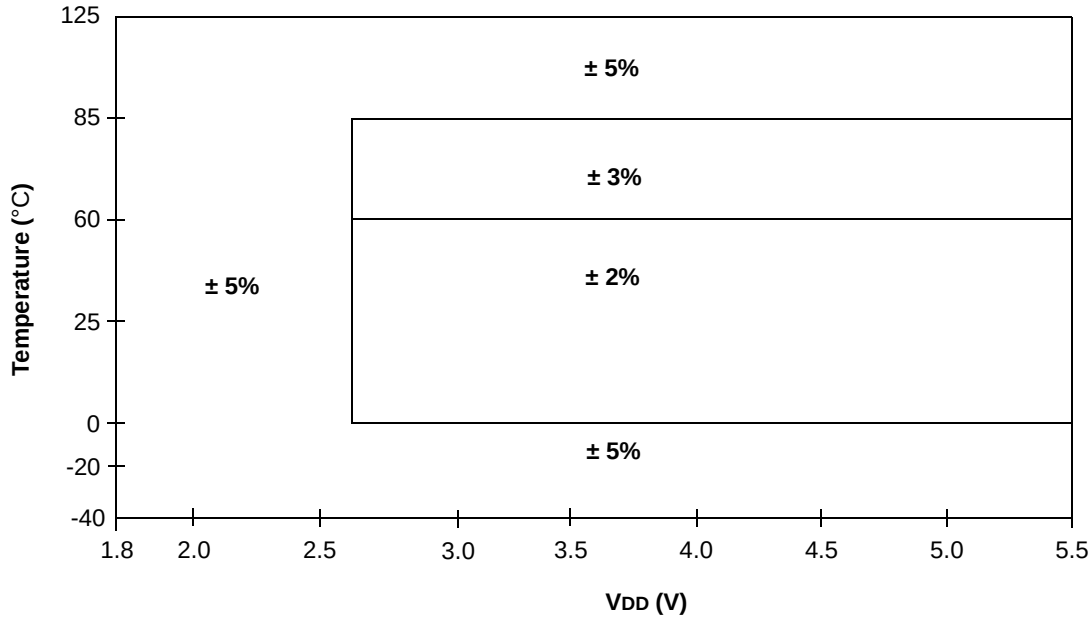


TABLE 27-12: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2 5	— —	— —	µs µs	VDD = 3.3-5V, -40°C to +85°C VDD = 3.3-5V
31	TWDT	Standard Watchdog Timer Time-out Period	10 10	17 17	27 30	ms ms	VDD = 3.3V-5V, -40°C to +85°C VDD = 3.3V-5V
31A	TWDTLP	Low Power Watchdog Timer Time-out Period	10 10	18 18	27 33	ms ms	VDD = 3.3V-5V, -40°C to +85°C VDD = 3.3V-5V
32	TOST	Oscillator Start-up Timer Period**(1,2,3)**	—	1024	—	Tosc	
33*	TPWRT	Power-up Timer Period, $\overline{PWRTE}$ = 0	40	65	140	ms	
34*	TIOZ	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.73	µs	
35	VBOR	Brown-out Reset Voltage	1.75 2.05 2.35 2.65	1.9 2.2 2.7 2.85	2.05 2.35 2.85 3.05	V V V V	BORV = 1.9V BORV = 2.2V BORV = 2.7V BORV = 2.85V
36*	VHYST	Brown-out Reset Hysteresis	—	25	50	mV	-40°C to +85°C
37*	TBORDC	Brown-out Reset DC Response Time	0	3	35	µs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

APPENDIX A: REVISION HISTORY

Revision A (May 2008)

Original data sheet for PIC18F1XK50/PIC18LF1XK50 devices.

Revision B (June 2008)

Revised 27.4 DC Characteristics table.

Revision C (04/2009)

Revised data sheet title; Revised Features section; Revised Table 1-2; Revised Table 3-1, Table 3-2; Added Note 3 in Section 9.1; Revised Register 14-1; Revised Example 16-1; Revised Section 18.8.4; Revised Register 18-3; Revised Table 20-2; Revised Sections 22.2.1, 22.2.2, 22.5.1.1, 22.7; Revised Tables 23-4, 27-1, 27-2, 27-3 27-4, 27-8.

Revision D (05/2010)

Revised the 20-pin PDIP, SSOP, SOIC Diagram; Added the 20-pin QFN Diagram; Revised Table 1, Table 1-1; Revised Figure 2-1; Added Note below Section 2.11.1 (Low-Speed Operation); Revised Table 3-1, Table 3-2; Revised Section 4 (Flash Program Memory) and Section 5 (Data EEPROM Memory); Revised Example 5-2, Table 5-1; Deleted Note 1 from Registers 7-4, 7-8; Revised Tables 9-1, 9-3; Revised Sections 14.1 (ECCP Outputs and Configuration), 14.4.4 (Enhanced PWM Auto-Shutdown Mode); Added Note 4 below Register 14-2; Revised Figure 14-10; Revised Equation 17-1; Revised Table 18-3 and Table 20-3; Revised Equation 21-1; Deleted Section 21.1.3 (Output Clamped to VSS); Revised Figure 21-1; Revised Table 21-1, Table 23-4 and Table 24-1; Added Note 2 to Table 24-1; Revised Register 24-6; Deleted Note 1 from Table 24-3; Revised Section 27 (tables); Added 20-Lead QFN Package Marking Information and Package Details; Revised the Product Identification System Section; Other minor corrections.

Revision E (10/2010)

Updated Section 27.0 Electrical Specifications.

Revision F (04/2015)

Updated Figures 1, 2 and 22-5, Table 1, Register 14-2; Updated note in Section 2.11.1; Updated Section 7.2 (Interrupt Priority), Section 27.0 (Electrical Specifications), Section 29.0 (Packaging Information) and the Product Identification System page; Added graphs in Section 28.0 (DC and AC Characteristics Graphs and Charts); Changed data sheet status from Preliminary to Final; Other minor corrections.