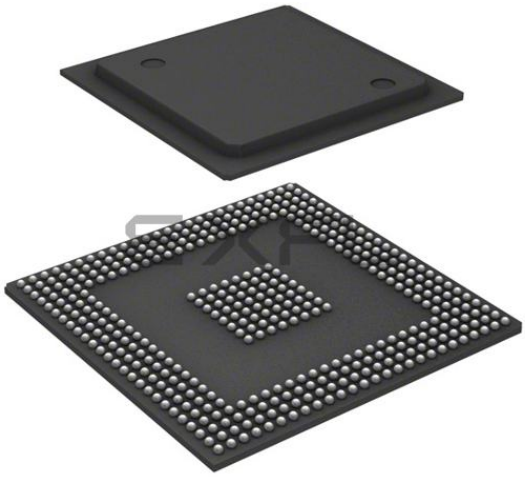

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Details	
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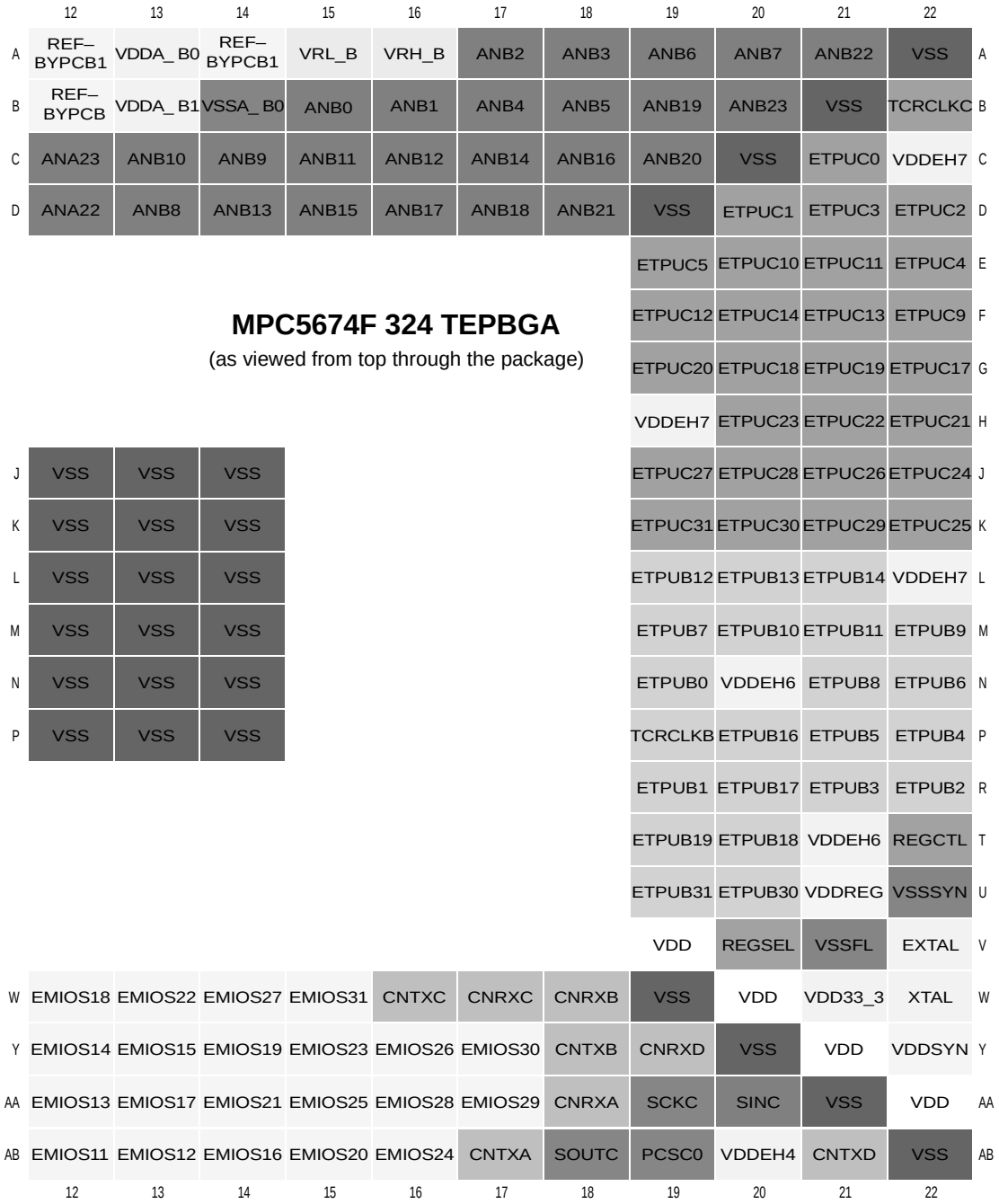
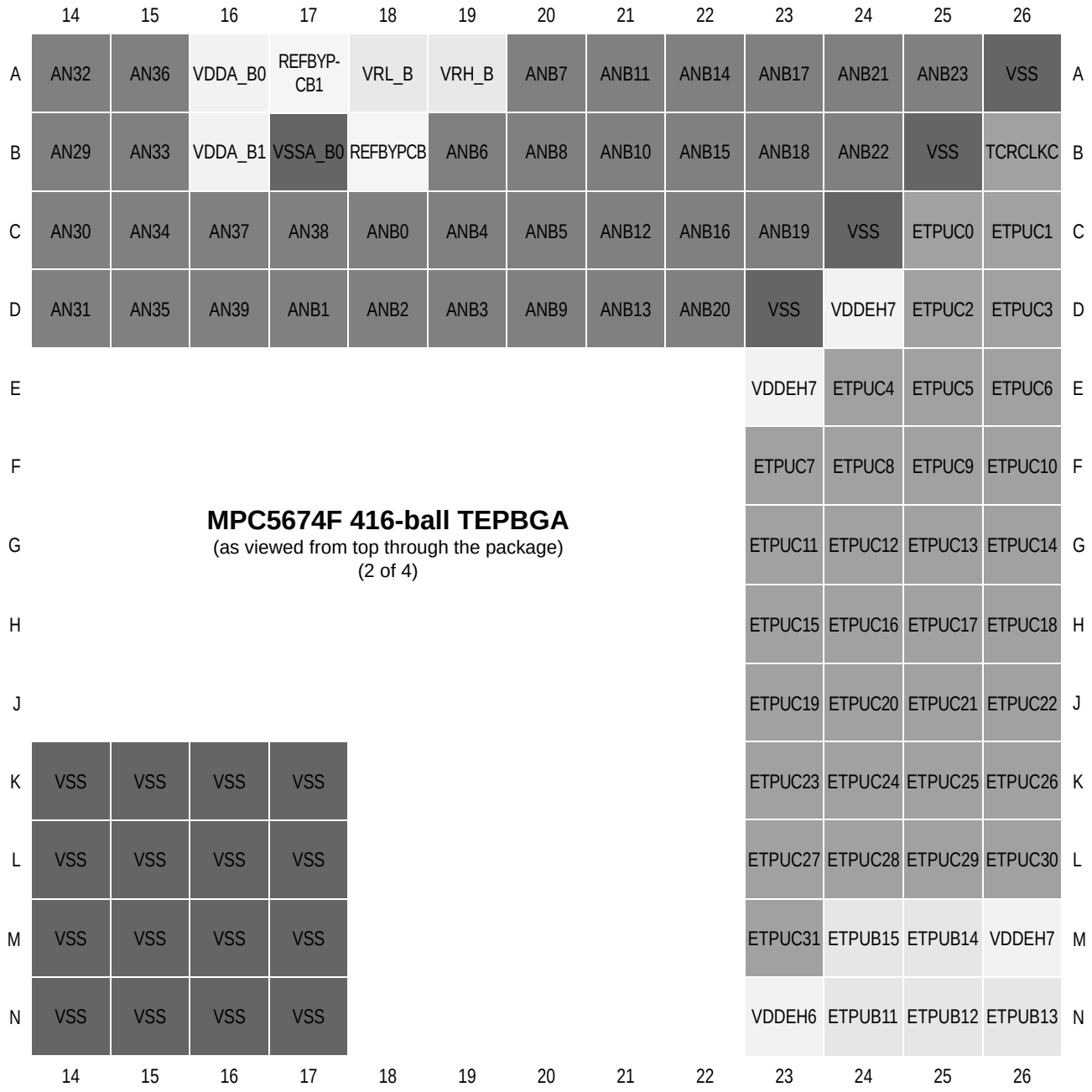
Number of I/O	32
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673ff3mvr2r



	12	13	14	15	16	17	18	19	20	21	22	
A	REF–BYPCB1	VDDA_ B0	REF–BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	REF–BYPCB	VDDA_ B1	VSSA_ B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
E								ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
F								ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
G								ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
H								VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	VSS	VSS	VSS					ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	VSS	VSS	VSS					ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	VSS	VSS	VSS					ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	VSS	VSS	VSS					ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VSS	VSS	VSS					ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	VSS	VSS	VSS					TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
R								ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
T								ETPUB19	ETPUB18	VDDEH6	REGCTL	T
U								ETPUB31	ETPUB30	VDDREG	VSSSYN	U
V								VDD	REGSEL	VSSFL	EXTAL	V
W	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB
	12	13	14	15	16	17	18	19	20	21	22	

Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN32	AN36	VDDA_B0	REFBYP-CB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	AN29	AN33	VDDA_B1	VSSA_B0	REFBYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E										VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F										ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G										ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H										ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J										ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)

Table 5. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	25	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	20	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
Junction to Board [5]	$R_{\theta JB}$	10	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. Thermal Characteristics, 324-pin Package[1]

MPC5674F Thermal Characteristic	Symbol	Value	Unit
Junction to ambient [2, 3], natural convection (one-layer board)	$R_{\theta JA}$	29	°C/W
Junction to ambient [1, 4], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	19	°C/W
Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	23	°C/W
Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	16	°C/W
Junction to board [5] (four-layer board 2s2p)	$R_{\theta JB}$	10	°C/W
Junction to case [6]	$R_{\theta JC}$	7	°C/W
Junction to package top [7], natural convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
4c	—	LVD 1.2V Hysteresis	15	20	25	mV
4d	$V_{LVDSTEP12}$	Trimming step LVD 1.2V	—	10	—	mV
5	I_{REGCTL}	VRC DC current output on REGCTL	—	—	20	mA
6	—	Voltage regulator 1.2V current consumption VDDREG	—	3	—	mA
7	$V_{DD33OUT}$	Nominal V_{REG} 3.3V output	—	3.3	—	V
7a	—	Untrimmed V_{REG} 3.3V output variation before band gap trim (unloaded) **Note:** Rising VDDSYN	$V_{DD33OUT}$ – 6%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7b	—	Trimmed V_{REG} 3.3V output variation after band gap trim (max. load 80mA)	$V_{DD33OUT}$ – 5%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7c	$V_{STEPV33}$	Trimming step VDDSYN	—	30	—	mV
8	V_{LVD33}	Nominal rising LVD 3.3V **Note:** ~$V_{DD33OUT}$ × 0.872	—	2.950	—	V
8a	—	Untrimmed LVD 3.3V variation before band gap trim **Note:** Rising VDDSYN	V_{LVD33} – 5%	V_{LVD33}	V_{LVD33} + 5%	V
8b	—	Trimmed LVD 3.3V variation after bad gap trim **Note:** Rising VDDSYN	V_{LVD33} – 3%	V_{LVD33}	V_{LVD33} + 3%	V
8c	—	LVD 3.3V Hysteresis	—	30	—	mV
8d	$V_{LVDSTEP33}$	Trimming step LVD 3.3V	—	30	—	mV
9	I_{DD33}	V_{REG} = 4.5 V, max DC output current V_{REG} = 4.25 V, max DC output current, crank condition **Note:** Max current supplied by VDDSYN that does not cause it to drop below V_{LVD33}	— —	— —	80 40	mA mA
10	—	Voltage regulator 3.3V current consumption VDDREG **Note:** Except I_{DD33}	—	2	—	mA
11	V_{PORREG}	POR rising on VDDREG	—	2.00	—	V
11a	—	POR VDDREG variation	V_{PORREG} – 30%	V_{PORREG}	V_{PORREG} + 30%	V
11b	—	POR VDDREG hysteresis	—	250	—	mV
12	V_{LVDREG}	Nominal rising LVD VDDREG (LDO3V / LDO5V mode)	—	2.950	—	V
12a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
12b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V

Table 19. Oscillator Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Crystal Mode Differential Amplitude[2] (Min differential voltage between EXTAL and XTAL)	$V_{crystal\_diff\_amp}$	$\lvert V_{extal} - V_{xtal} \rvert$ > 0.4 V	—	V
2	Crystal Mode: Internal Differential Amplifier Noise Rejection	$V_{crystal\_diff\_amp\_nr}$	—	$\lvert V_{extal} - V_{xtal} \rvert$ < 0.2 V	V
3	EXTAL Input High Voltage Bypass mode, External Reference	V_{IHEXT}	((V_{DD33}/2) + 0.4 V)	—	V
4	EXTAL Input Low Voltage Bypass mode, External Reference	V_{ILEXT}	—	(V_{DD33}/2) – 0.4 V	V
5	XTAL Current[3]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	($2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[4])	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	($2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[4])	pF

1 All values given are initial design targets and subject to change.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.

3 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

4 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

4.9 eQADC Electrical Characteristics

Table 20. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles Single Ended Conversion Cycles 12 bit resolution Single Ended Conversion Cycles 10 bit resolution Single Ended Conversion Cycles 8 bit resolution **Note:** Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here.	CC	 2 + 14 2 + 12 2 + 10	 128 + 14 128 + 12 128 + 10	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB

4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 22. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in Figure 43 and Figure 44.

Figure 43. 324 TEPBGA Package (1 of 2)

6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5674F Microprocessor Reference Manual* (document number MPC5674FRM).

Appendix A Signal Properties and Muxing

The following table shows the signals properties for each pin on the MPC5674F. For each port pin that has an associated SIU_PCR*n* register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See Figure 49.

Table 2. Signal Properties Summary

GPIO/ PCR[1]	Signal Name[2]	P/ F/ G	Function[3]	Function Summary	I/O	Pad Type
113	TCRCLKA_IRQ7_GPIO113	P	TCRCLKA	eTPU A TCR clock	I	5V M
		A1	IRQ7	External interrupt request	I	
		A2	—	—	—	
		G	GPIO113	GPIO	I/O	

Primary Functions are listed First

Secondary Functions are alternate functions

GPIO Functions are listed **Last**

Function not implemented on this device

Figure 49. Supported Functions Example

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO131	GPIO	I/O							
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO132	GPIO	I/O							
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO133	GPIO	I/O							
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E1	F2	F2
		A1	IRQ8	External interrupt request	I							
		A2	—	—	—							
		G	GPIO134	GPIO	I/O							
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C1	F3	F3
		A1	IRQ9	External interrupt request	I							
		A2	—	—	—							
		G	GPIO135	GPIO	I/O							
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E2	F4	F4
		A1	IRQ10	External interrupt request	I							
		A2	—	—	—							
		G	GPIO136	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
149	ETPUB2_ETPUB18_ GPIO149	P	ETPUB2	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R22	T26	U23
		A1	ETPUB18	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO149	GPIO	I/O							
150	ETPUB3_ETPUB19_ GPIO150	P	ETPUB3	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R21	R23	T22
		A1	ETPUB19	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO150	GPIO	I/O							
151	ETPUB4_ETPUB20_ GPIO151	P	ETPUB4	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P22	R24	U24
		A1	ETPUB20	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO151	GPIO	I/O							
152	ETPUB5_ETPUB21_ GPIO152	P	ETPUB5	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P21	R25	U25
		A1	ETPUB21	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO152	GPIO	I/O							
153	ETPUB6_ETPUB22_ GPIO153	P	ETPUB6	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N22	R26	U26
		A1	ETPUB22	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO153	GPIO	I/O							
154	ETPUB7_ETPUB23_ GPIO154	P	ETPUB7	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M19	P23	T23
		A1	ETPUB23	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO154	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
464	ETPUC23_PCSD5_ GPIO464[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H20	K23	J23
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	MAA0	ADC A Mux Address 0	O							
		A3	MAB0	ADC B Mux Address 0	O							
		G	GPIO464	GPIO	I/O							
465	ETPUC24_PCSD4_ GPIO465[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J22	K24	J24
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	MAA1	ADC A Mux Address 1	O							
		A4	MAB1	ADC B Mux Address 1	O							
		G	GPIO465	GPIO	I/O							
466	ETPUC25_PCSD3_ GPIO466[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K22	K25	K21
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	MAA2	ADC A Mux Address 2	O							
		A3	MAB2	ADC B Mux Address 2	O							
		G	GPIO466	GPIO	I/O							
467	ETPUC26_PCSD2_ GPIO467[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J21	K26	J25
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO467	GPIO	I/O							
468	ETPUC27_PCSD1_ GPIO468[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J19	L23	J26
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO468	GPIO	I/O							
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J20	L24	K22
		A1	PCSD0	DSPI D peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO469	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
96	PCSA0_PCSD2_ GPIO96	P	PCSA0	DSPI A peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	AB6	AE6	AD6
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO96	GPIO	I/O							
97	PCSA1_ GPIO97	P	PCSA1	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC6	AC6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO97	GPIO	I/O							
98	PCSA2_ GPIO98	P	PCSA2	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC7	AF6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO98	GPIO	I/O							
99	PCSA3_ GPIO99	P	PCSA3	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AE7	AD7
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO99	GPIO	I/O							
100	PCSA4_ GPIO100	P	PCSA4	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AE5	AE5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO100	GPIO	I/O							
101	PCSA5_ETRIG1_ GPIO101	P	PCSA5	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AA6	AD6	AA8
		A1	ETRIG1	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO101	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
EBI												
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	—/Up	—	—	AD9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO256	GPIO	I/O							
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	—/Up	—	—	U1
		A1	D_ADD_DAT31	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO257	GPIO	I/O							
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	—/Up	—	—	T6
		A1	D_TEA	EBI transfer error acknowledge	I							
		A2	—	—	—							
		G	GPIO258	GPIO	I/O							
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO259	GPIO	I/O							
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO260	GPIO	I/O							
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO261	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
273	D_ADD26_D_ADD_DAT26_ GPIO273	P	D_ADD26	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE11
		A1	D_ADD_DAT26	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO273	GPIO	I/O							
274	D_ADD27_D_ADD_DAT27_ GPIO274	P	D_ADD27	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF11
		A1	D_ADD_DAT27	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO274	GPIO	I/O							
275	D_ADD28_D_ADD_DAT28_ GPIO275	P	D_ADD28	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD12
		A1	D_ADD_DAT28	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO275	GPIO	I/O							
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB12
		A1	D_ADD_DAT29	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO276	GPIO	I/O							
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE12
		A1	D_ADD_DAT30	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO277	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO283	GPIO	I/O							
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO284	GPIO	I/O							
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO285	GPIO	I/O							
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO286	GPIO	I/O							
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO287	GPIO	I/O							

Table 46 lists the pin locations of the power and ground signals on the 516 TEPBGA package.

Table 46. 516-pin Power Supply Locations

VDD

A2	B3	C4	D5	E6	N4	AB4	AB23	AC3	AC12	AC24	AD2	AD25	AE1	AE26

VDD33

M1	P6	L21	AA4	AA11	AA14	AA23

VDDE10

F16	F17	F19	F21	N21	P21	AA22

VDDE2

N10	P10	P11	R10	R11	T1	T10	T11	T12	U10	U11	U12	W4	AC1	AC5	AF2

VDDE8

F6	F8	F10	F11	N6	AA5

VDDE9

AA13	AB6	AB7	AB18	AB19	AB20	AB21

VDDEH1

B1	P4

VDDEH3

AC10	AF5

VDDEH4

AC11	AF22

VDDEH5

AC21	AF25

VDDEH6

N23	AC25

VDDEH7

D24	E23	M26

VSS

A25	B2	B25	B26	C3	C24	D4	D23	E5	E7	E8	E9	E10	E11	E12	E13	E14	E15
E16	E17	E18	E19	E21	E22	F5	F13	F14	K10	K11	K12	K13	K14	K15	K16	K17	L10
L11	L12	L13	L14	L15	L16	L17	M10	M11	M12	M13	M14	M15	M16	M17	N11	N12	N13
N14	N15	N16	N17	P12	P13	P14	P15	P16	P17	R12	R13	R14	R15	R16	R17	T13	T14
T15	T16	T17	U13	U14	U15	U16	U17	AA6	AA21	AB5	AB22	AC4	AC23	AD3	AD24	AE2	AE25