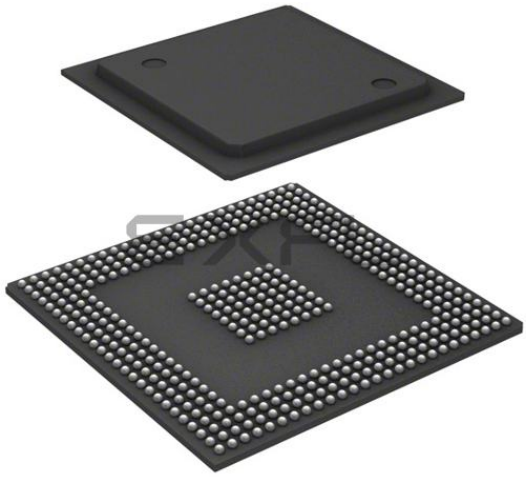

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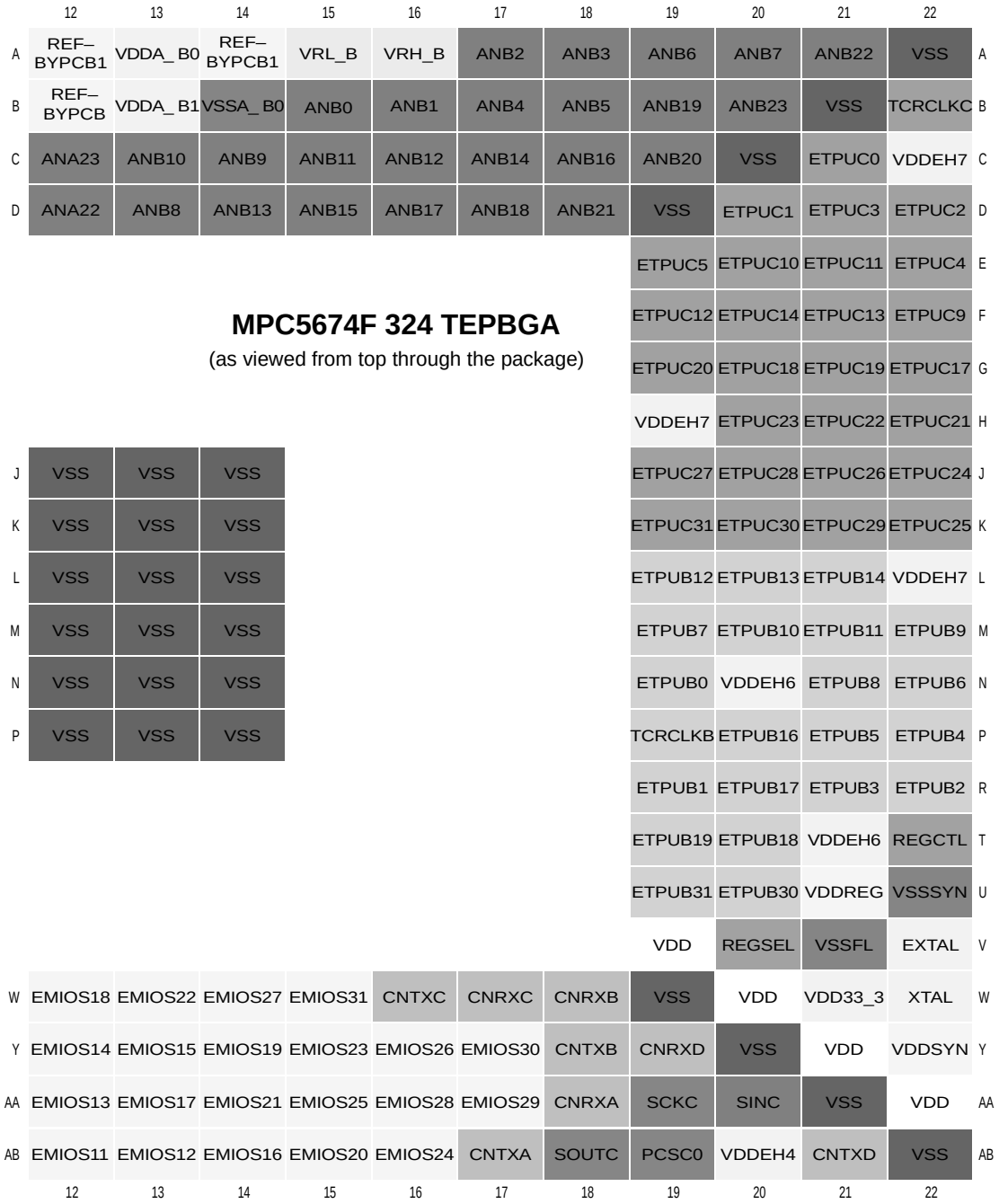
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673fk0mvr2



	12	13	14	15	16	17	18	19	20	21	22	
A	REF–BYPCB1	VDDA_ B0	REF–BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	REF–BYPCB	VDDA_ B1	VSSA_ B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
E								ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
F								ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
G								ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
H								VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	VSS	VSS	VSS					ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	VSS	VSS	VSS					ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	VSS	VSS	VSS					ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	VSS	VSS	VSS					ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VSS	VSS	VSS					ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	VSS	VSS	VSS					TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
R								ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
T								ETPUB19	ETPUB18	VDDEH6	REGCTL	T
U								ETPUB31	ETPUB30	VDDREG	VSSSYN	U
V								VDD	REGSEL	VSSFL	EXTAL	V
W	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB
	12	13	14	15	16	17	18	19	20	21	22	

Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)

3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

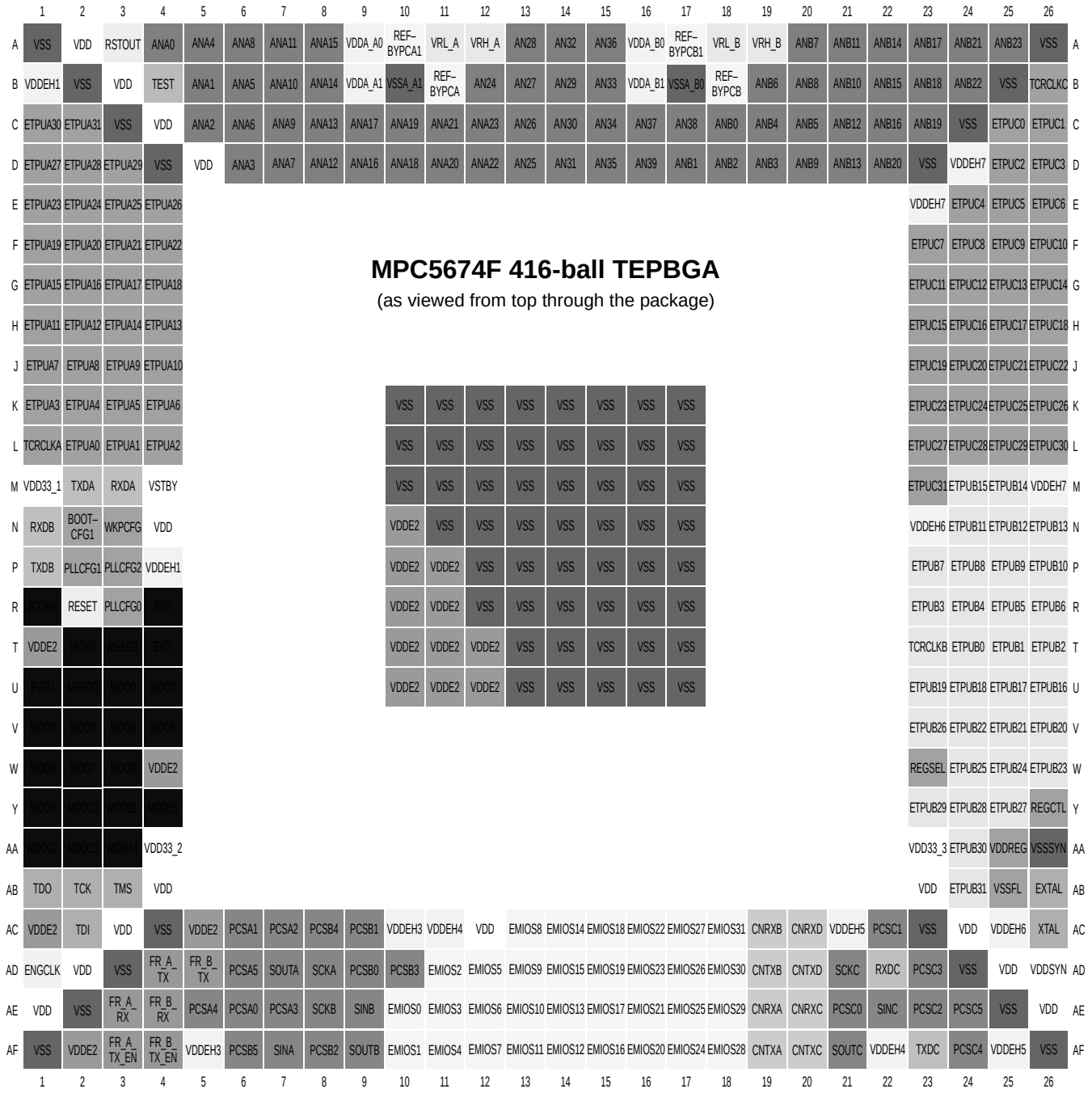


Figure 6. MPC5674F 416-ball TEPBGA (full diagram)

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	–0.3	2.0 [2]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	6.4 [3,4]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	5.3 [4,5]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	5.3 [4,5]	V
5	Analog Supply Voltage (reference to V_{SSA}[6])	V_{DDA}[7]	–0.3	6.4 [3,4]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	5.3 [4,5]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	6.4 [3,4]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	6.4 [3,4]	V
9	Analog Reference High Voltage (reference to V_{RL}[8])	V_{RH}[9]	–0.3	6.4 [3,4]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	6.4 [3,4]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [10] (per pin, applies to all digital pins)	I_{MAXD}	–3 [11]	3 [11]	mA
16	Maximum Analog Input Current [12] (per pin, applies to all analog pins)	I_{MAXA}	– 3 [7]	3 [7,11]	mA
17	Maximum Operating Temperature Range [13] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [14] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [15]	MSL	—	3	—

Table 20. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 22. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

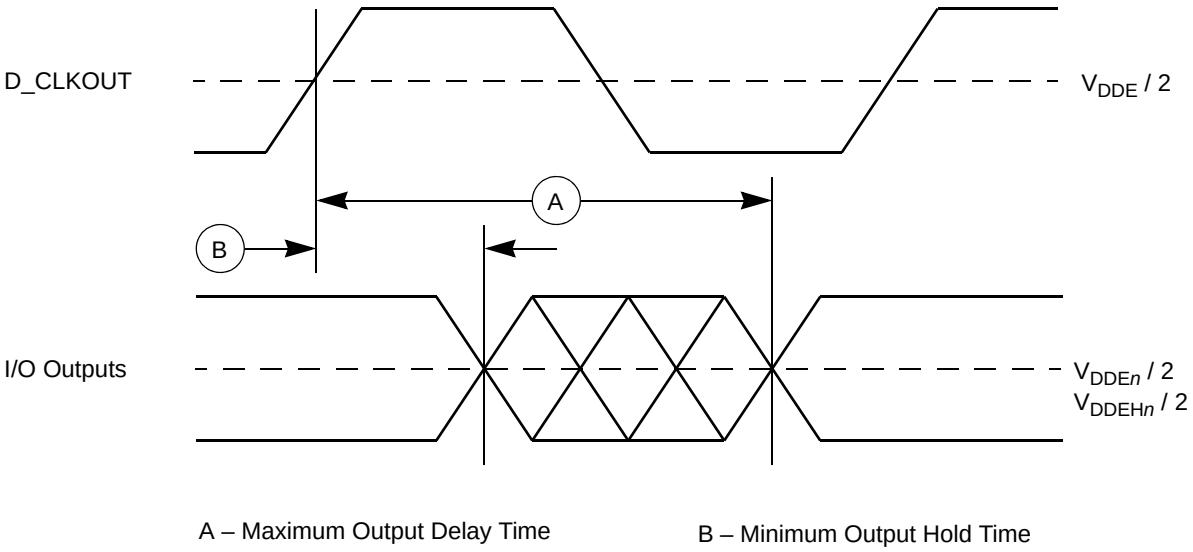


Figure 18. Generic Output Delay/Hold Timing

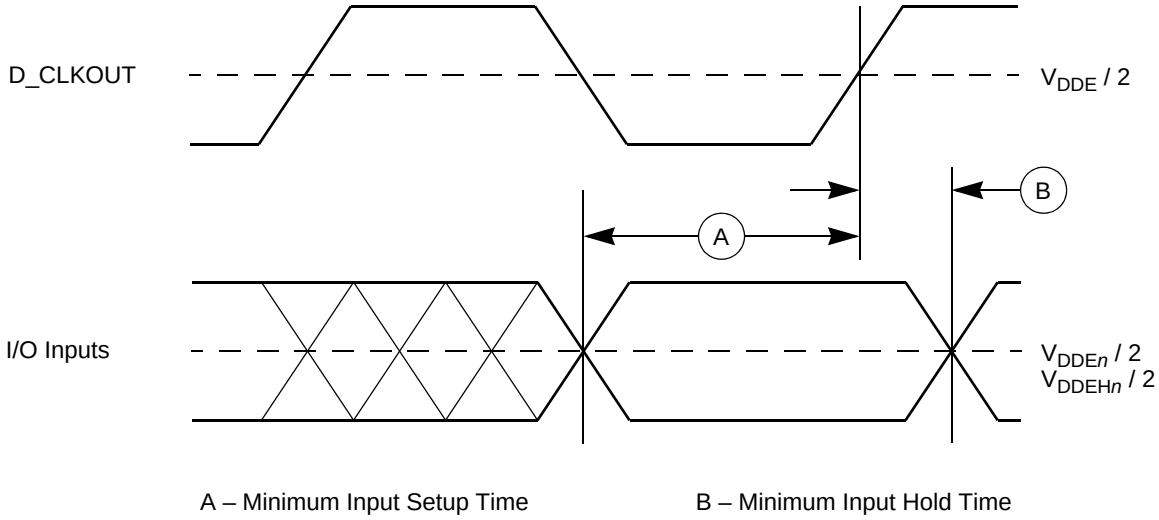


Figure 19. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 33. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1 Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

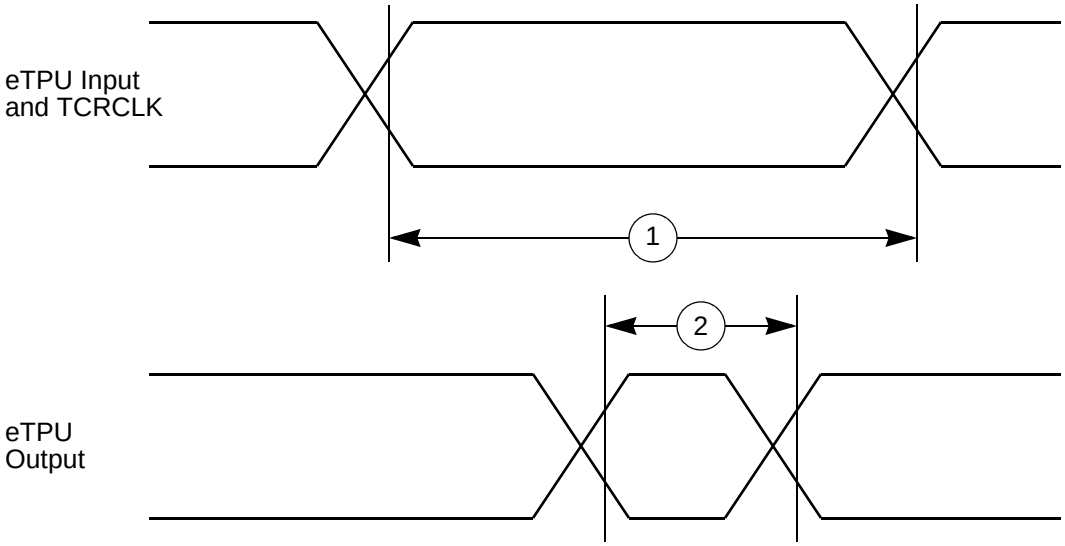


Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 39. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H1	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO119	GPIO	I/O							
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H2	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO120	GPIO	I/O							
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	J1	H2
		A1	ETPUA19	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO121	GPIO	I/O							
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	J2	H3
		A1	ETPUA20	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO122	GPIO	I/O							
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H3	J3	J3
		A1	ETPUA21	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO123	GPIO	I/O							
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G1	J4	K6
		A1	ETPUA22	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO124	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO125	GPIO	I/O							
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO126	GPIO	I/O							
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO127	GPIO	I/O							
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO128	GPIO	I/O							
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO129	GPIO	I/O							
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO130	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO131	GPIO	I/O							
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO132	GPIO	I/O							
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO133	GPIO	I/O							
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E1	F2	F2
		A1	IRQ8	External interrupt request	I							
		A2	—	—	—							
		G	GPIO134	GPIO	I/O							
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C1	F3	F3
		A1	IRQ9	External interrupt request	I							
		A2	—	—	—							
		G	GPIO135	GPIO	I/O							
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E2	F4	F4
		A1	IRQ10	External interrupt request	I							
		A2	—	—	—							
		G	GPIO136	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	E1	E1
		A1	IRQ11	External interrupt request	I							
		A2	—	—	—							
		G	GPIO137	GPIO	I/O							
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E2	E2
		A1	IRQ12	External interrupt request	I							
		A2	—	—	—							
		G	GPIO138	GPIO	I/O							
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	E3	E3
		A1	IRQ13	External interrupt request	I							
		A2	—	—	—							
		G	GPIO139	GPIO	I/O							
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	E4	E4
		A1	IRQ14	External interrupt request	I							
		A2	—	—	—							
		G	GPIO140	GPIO	I/O							
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	D1	D1
		A1	IRQ15	External interrupt request	I							
		A2	—	—	—							
		G	GPIO141	GPIO	I/O							
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO142	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
155	ETPUB8_ETPUB24_ GPIO155	P	ETPUB8	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N21	P24	T24
		A1	ETPUB24	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO155	GPIO	I/O							
156	ETPUB9_ETPUB25_ GPIO156	P	ETPUB9	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M22	P25	R22
		A1	ETPUB25	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO156	GPIO	I/O							
157	ETPUB10_ETPUB26_ GPIO157	P	ETPUB10	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M20	P26	T25
		A1	ETPUB26	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO157	GPIO	I/O							
158	ETPUB11_ETPUB27_ GPIO158	P	ETPUB11	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M21	N24	T26
		A1	ETPUB27	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO158	GPIO	I/O							
159	ETPUB12_ETPUB28_ GPIO159	P	ETPUB12	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L19	N25	R23
		A1	ETPUB28	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO159	GPIO	I/O							
160	ETPUB13_ETPUB29_ GPIO160	P	ETPUB13	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L20	N26	P22
		A1	ETPUB29	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO160	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E21	G23	G22
		A1	IRQ2	External interrupt request	I							
		A2	—	—	—							
		G	GPIO452	GPIO	I/O							
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F19	G24	G23
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO453	GPIO	I/O							
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F21	G25	G24
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO454	GPIO	I/O							
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F20	G26	G25
		A1	IRQ5	External interrupt request	I							
		A2	—	—	—							
		G	GPIO455	GPIO	I/O							
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H23	G26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO456	GPIO	I/O							
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O							
		A2	—	—	—							
		G	GPIO457	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
464	ETPUC23_PCSD5_ GPIO464[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H20	K23	J23
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	MAA0	ADC A Mux Address 0	O							
		A3	MAB0	ADC B Mux Address 0	O							
		G	GPIO464	GPIO	I/O							
465	ETPUC24_PCSD4_ GPIO465[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J22	K24	J24
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	MAA1	ADC A Mux Address 1	O							
		A4	MAB1	ADC B Mux Address 1	O							
		G	GPIO465	GPIO	I/O							
466	ETPUC25_PCSD3_ GPIO466[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K22	K25	K21
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	MAA2	ADC A Mux Address 2	O							
		A3	MAB2	ADC B Mux Address 2	O							
		G	GPIO466	GPIO	I/O							
467	ETPUC26_PCSD2_ GPIO467[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J21	K26	J25
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO467	GPIO	I/O							
468	ETPUC27_PCSD1_ GPIO468[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J19	L23	J26
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO468	GPIO	I/O							
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J20	L24	K22
		A1	PCSD0	DSPI D peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO469	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANA3	P	ANA3[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA3	ANA3	B6	D6	D6
—	ANA4	P	ANA4[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA4	ANA4	A6	A5	A5
—	ANA5	P	ANA5[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA5	ANA5	A7	B6	B6
—	ANA6	P	ANA6[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA6	ANA6	B7	C6	C6
—	ANA7	P	ANA7[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA7	ANA7	B8	D7	C7
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8	ANA8	C5	A6	D7
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9	ANA9	C7	C7	A6
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10	ANA10	C6	B7	B7
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11	ANA11	D6	A7	A7
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12	ANA12	D7	D8	D8
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13	ANA13	C8	C8	C8
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14	ANA14	D8	B8	B8
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15	ANA15	A8	A8	A8
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16	ANA16	D9	D9	D9
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17	ANA17	C9	C9	C9
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18	ANA18	D10	D10	D10
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19	ANA19	C10	C10	C10
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20	ANA20	D11	D11	D11
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21	ANA21	C11	C11	C11
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22	ANA22	D12	D12	C12
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23	ANA23	C12	C12	D12
—	AN24	P	AN24	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN24	AN24	—	B12	B12
—	AN25	P	AN25	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN25	AN25	—	D13	C13
—	AN26	P	AN26	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN26	AN26	—	C13	D13

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up	—/Up	—	N1	L5
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO92	GPIO	I/O							
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	—	AF23	AF23
		A1	ETRIG0	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO244	GPIO	I/O							
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up	—/Up	—	AD22	AD22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO245	GPIO	I/O							
DSPI												
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y7	AD8	AB8
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO93	GPIO	I/O							
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up	—/Up	AA7	AF7	AE7
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO94	GPIO	I/O							
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up	—/Up	AB7	AD7	AC7
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO95	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
262	D_ADD15_ GPIO262	P	D_ADD15	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO262	GPIO	I/O							
263	D_ADD16_D_ADD_DAT16_ GPIO263	P	D_ADD16	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R5
		A1	D_ADD_DAT16	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO263	GPIO	I/O							
264	D_ADD17_D_ADD_DAT17_ GPIO264	P	D_ADD17	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T5
		A1	D_ADD_DAT17	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO264	GPIO	I/O							
265	D_ADD18_D_ADD_DAT18_ GPIO265	P	D_ADD18	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T2
		A1	D_ADD_DAT18	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO265	GPIO	I/O							
266	D_ADD19_D_ADD_DAT19_ GPIO266	P	D_ADD19	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T3
		A1	D_ADD_DAT19	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO266	GPIO	I/O							
267	D_ADD20_D_ADD_DAT20_ GPIO267	P	D_ADD20	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T4
		A1	D_ADD_DAT20	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO267	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO305	GPIO	I/O							
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO306	GPIO	I/O							
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO307	GPIO	I/O							
Reset and Clocks												
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	RESET/Up	M2	R2	N5
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	RSTOUT/ High	A3	A3	A3
211	BOOTCFG0_IRQ2_ GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	BOOTCFG/ Down	—	—	L4
		A1	IRQ2		I							
		A2	—	—	—							
		G	GPIO211	GPIO	I/O							
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	Input/Down	L1	N2	L3
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO212	GPIO	I/O							

Table 45 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 44. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13	J14	J9
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13	M14	N11
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3							

Table 47. Revision History (continued)

Revision (Date)	Description of changes
9	Updated Table 1.,"Orderable Part Numbers" with actual available parts. Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200 MHz nom and max.—Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”. Updated footnotes of Table 3.,"Absolute Maximum Ratings" to: • 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining. • 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining. • 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining. Updated Table 6.,"Thermal Characteristics, 324-pin Package" to show MPC5674F thermal characteristics. In Table 10.,"PMC Operating conditions", updated the parameter “Supply voltage VDD 1.2V nominal" to “Core supply voltage". In Table 11.,"PMC Electrical Specifications", updated the following rows: • Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V. • The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%”, respectively. • The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%”, respectively. In Table 12.,"Power Sequence Pin States for MH and AE pads", updated the row (VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”. In Table 13.,"Power Sequence Pin States for F and FS pads", updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high), parameter “F and FS pad” to “Outputs Disabled”. In Table 14.,"DC Electrical Specifications", updated the spec 'Operating Current 1.2 V Supplies @ f_{SYS} = 264 MHz' with 'V_{DD} @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary. Updated current (mA) values in Table 15.,"V_{DDE}/V_{DDEH} I/O Pad Average DC Current" from Spec 5 to 13: • Spec 5 Current (mA) from 6.5 to 7.4 • Spec 6 Current (mA) from 9.4 to 10.5 • Spec 7 Current (mA) from 10.8 to 12.3 • Spec 8 Current (mA) from 33.3 to 35.2 • Spec 9 Current (mA) from 12.0 to 12.7 • Spec 10 Current (mA) from 6.2 to 6.7 • Spec 11 Current (mA) from 4.0 to 4.2 • Spec 12 Current (mA) from 2.4 to 2.6 • Spec 13 Current (mA) from8.9 to 9. In Table 35.,"Nexus Debug Port Timing", updated the footnote of parameter “tCYC” to “See Notes on tcyc in Table27”. Removed references to “Section I/O Pad VDD33 Current Specifications” .
10	Updated Figure 1.,"MPC5674F Orderable Part Number Description" with changes in “Revision of Silicon” and “Fab Revision ID”. Updated Table 1.,"Orderable Part Numbers" with changes in Part numbers and Package Description.
10.1	In Figure 1.,"MPC5674F Orderable Part Number Description", replaced “Revision of Silicon for TSMC is 0 for now. In future, it will be revision 1” with “0 = Rev 0 (TSMC14)”.