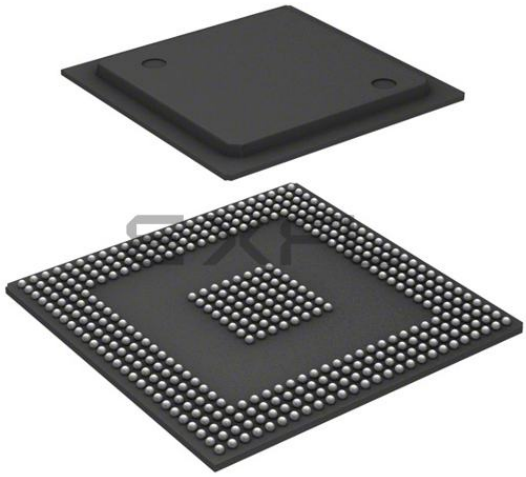

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673fk0mvr2r

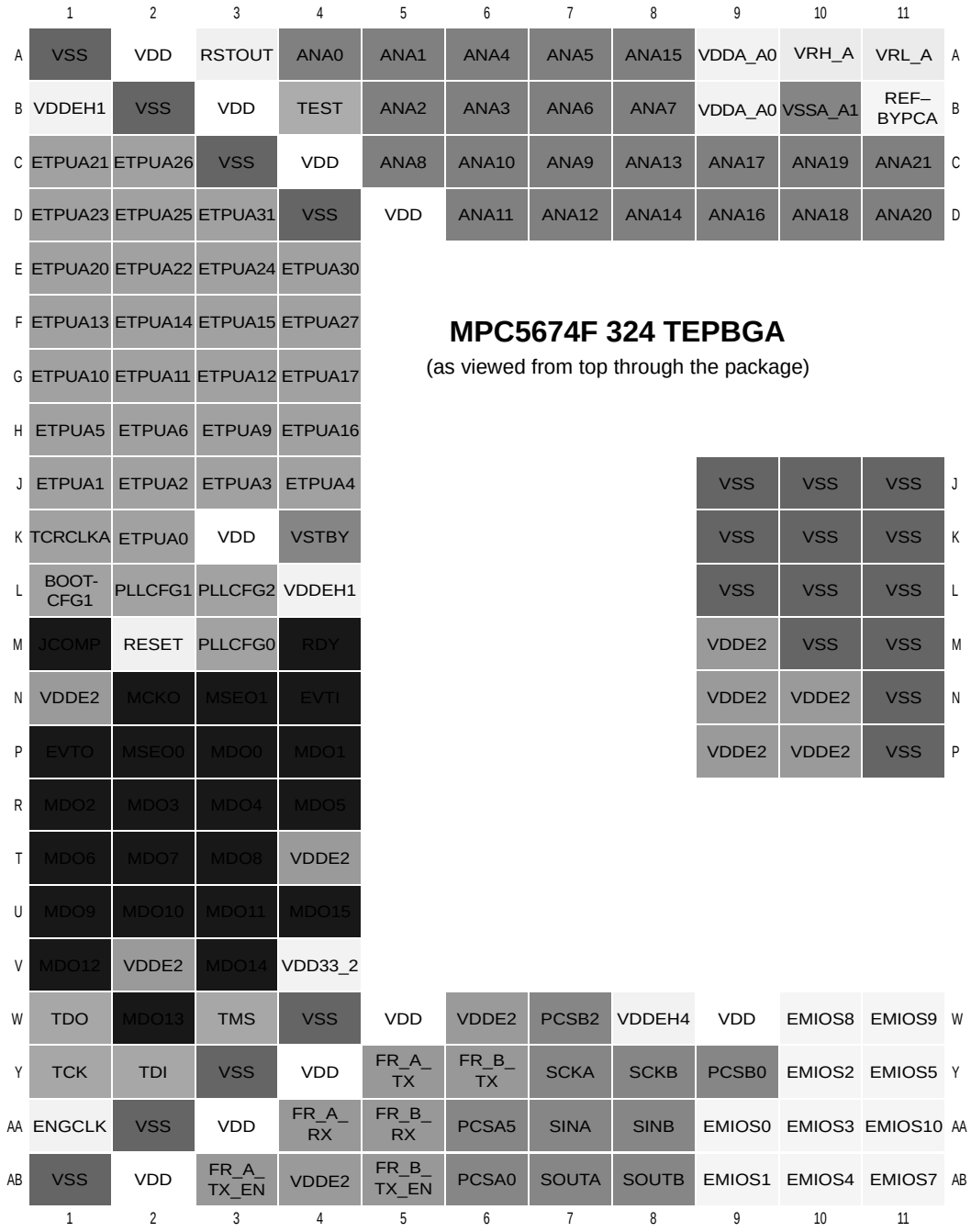
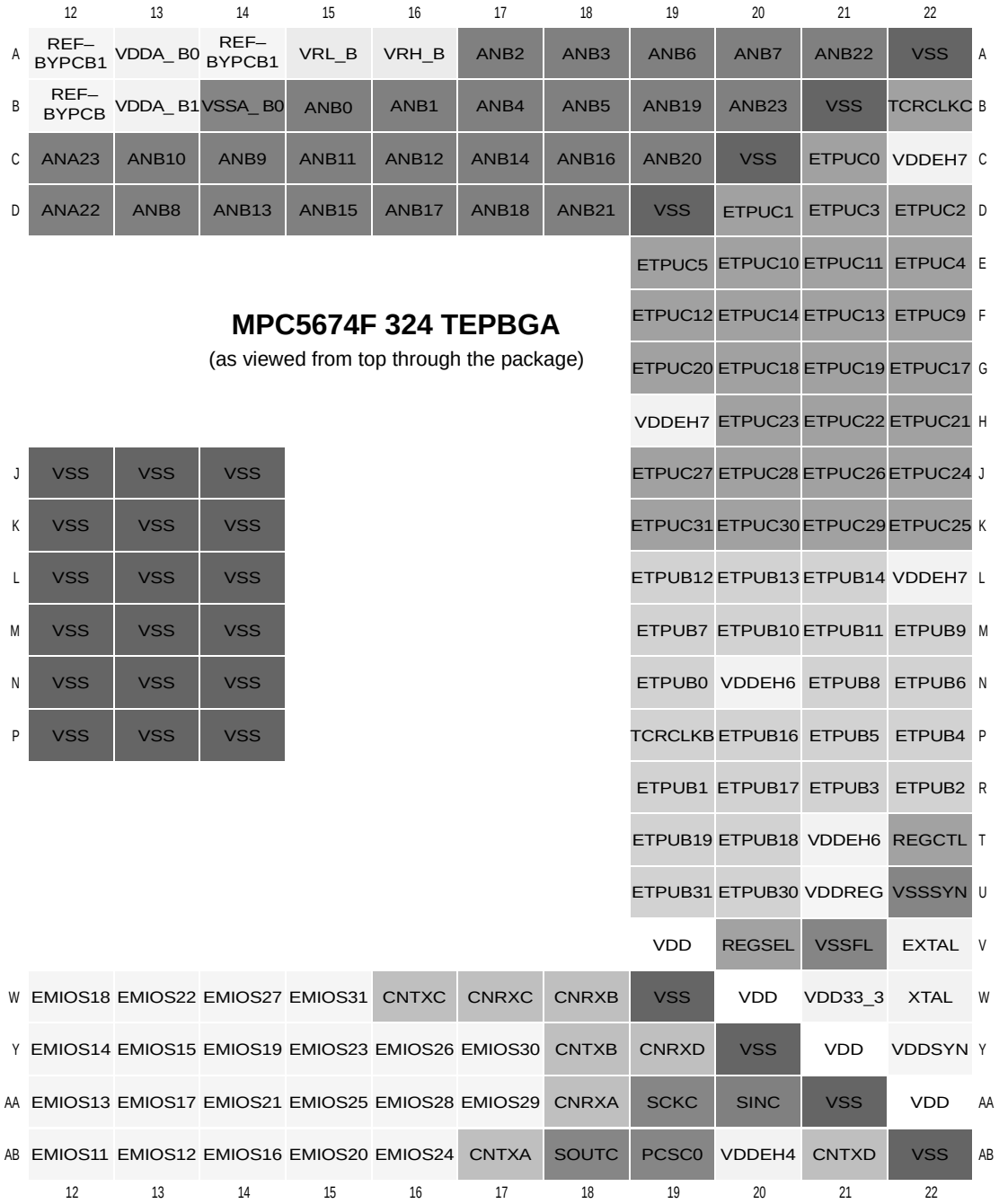


Figure 4. MPC5674F 324-ball TEPBGA (1 of 2)



	12	13	14	15	16	17	18	19	20	21	22	
A	REF–BYPCB1	VDDA_ B0	REF–BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	REF–BYPCB	VDDA_ B1	VSSA_ B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
E								ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
F								ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
G								ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
H								VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	VSS	VSS	VSS					ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	VSS	VSS	VSS					ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	VSS	VSS	VSS					ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	VSS	VSS	VSS					ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VSS	VSS	VSS					ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	VSS	VSS	VSS					TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
R								ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
T								ETPUB19	ETPUB18	VDDEH6	REGCTL	T
U								ETPUB31	ETPUB30	VDDREG	VSSSYN	U
V								VDD	REGSEL	VSSFL	EXTAL	V
W	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB
	12	13	14	15	16	17	18	19	20	21	22	

Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)

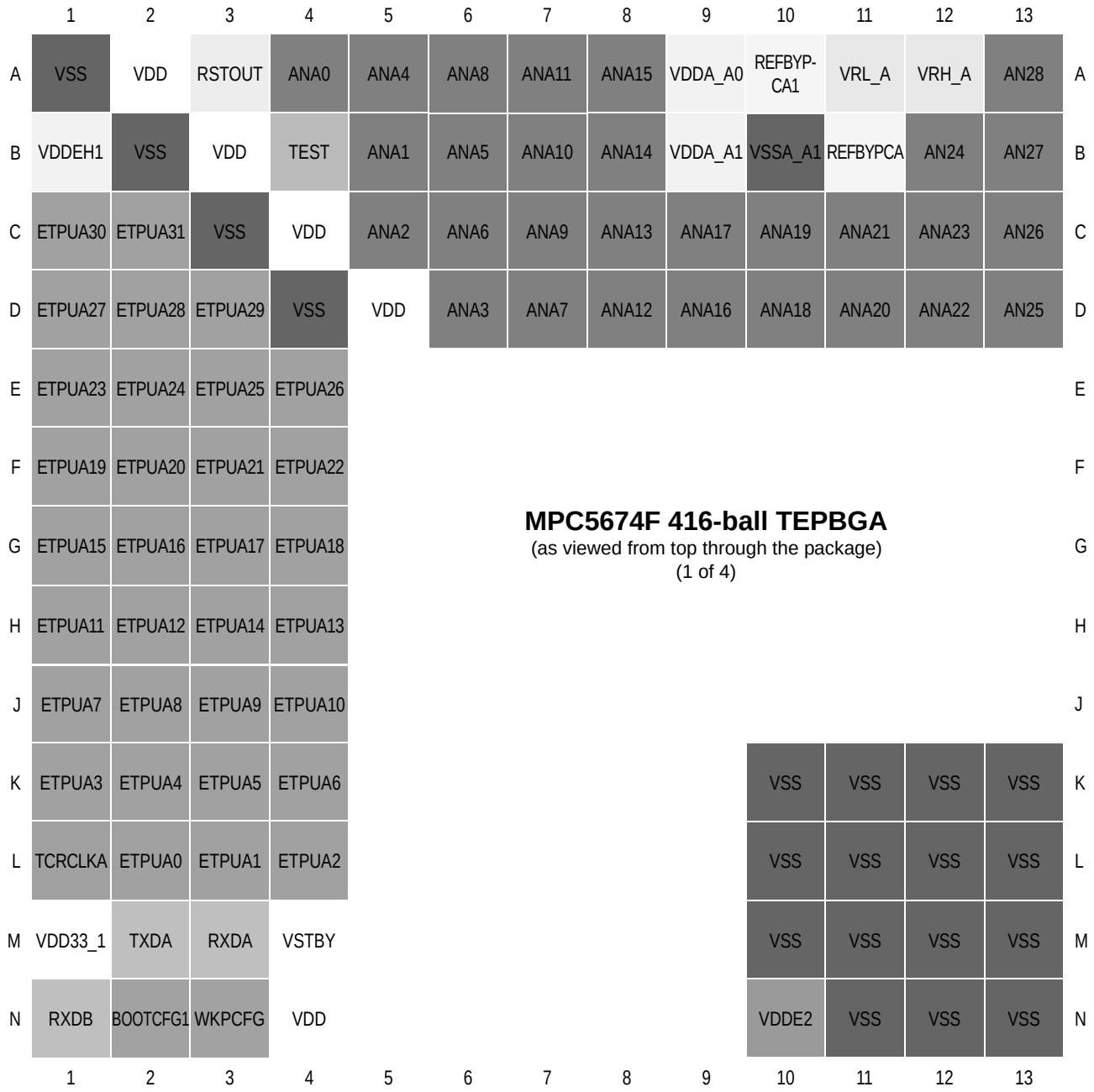


Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)

4 “FM on” = FM depth of ±2%

5 K = 30 dBµV

Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBµV	1
				50–150	48		
				150–500	48		
				500–1000	47		
				IEC and SAE level	G[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBµV	1
				50–150	44		
				150–500	41		
				500–1000	36		
				IEC and SAE level	G[2]	—	1, 3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 G = 48 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 “FM on” = FM depth of ±2%

4.4 ESD Characteristics

Table 9. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Note: For ADC internal resource measurements, see Table 21 in Section 4.9.1, “ADC Internal Resource Measurements.”

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
27	Operating Current V_{DDE}/V_{DDEH}[17] Supplies V_{DDE2} V_{DDEH1} V_{DDEH3} V_{DDEH4} V_{DDEH5} V_{DDEH6} V_{DDEH7}	 I_{DD2} I_{DD1} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7}	 — — — — — — —	 note[17]	 mA mA mA mA mA mA mA
28	Fast I/O Weak Pull Up/Down Current[18] 3.0 V–3.6 V	 I_{ACT_F}	 42	 158	 µA
29	Medium I/O Weak Pull Up/Down Current[19] 3.0 V–3.6 V 4.5 V–5.5 V	I_{ACT_S}	 15 35	 95 200	 µA µA
30	I/O Input Leakage Current[20]	I_{INACT_D}	–2.5	2.5	µA
31	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
32	Analog Input Current, Channel Off[21], AN[0:7], AN38, AN39 Analog Input Current, Channel Off, all other analog inputs AN[x]	I_{INACT_A}	–250 –150	250 150	nA nA
33	V_{SS} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
34	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 100	mV
35	V_{RL} Differential Voltage	$V_{RL} – V_{SSA}$	–100	100	mV
36	Analog Reference High Voltage	V_{RH}	V_{DDA} – 100	V_{DDA}	mV
37	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	4.75	5.25	V
38	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
39	Operating Temperature Range—Ambient (Packaged)	T_A (T_L to T_H)	–40.0	125.0	°C
40	Slew rate on power supply pins	—	—	25	V/ms
41	Weak Pull-Up/Down Resistance[22], 200 K Option	$R_{PUPD200K}$	130	280	kΩ
42	Weak Pull-Up/Down Resistance[22], 100 K Option	$R_{PUPD100K}$	65	140	kΩ
43	Weak Pull-Up/Down Resistance[22], 5 K Option	R_{PUPD5K}	1.4	7.5	kΩ
44	Pull-Up/Down Resistance Matching Ratios[23] (100K/200K)	$R_{PUPDMTCH}$	–2.5	+2.5	%

1 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

2 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

3 Assumed with DC load.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 V_{STBY} below 0.95 V the RAM will not retain states, but will be operational. V_{STBY} can be 0 V when bypass standby mode.

7 Regulator is functional with derated performance, with supply voltage down to 4.0 V for system with V_{DDREG} = 4.5 V (min).

8 2.7 V minimum operating voltage allowed during vehicle crank for system with V_{DDREG} = 3.0 V (min). Normal operating voltage should be either V_{DDREG} = 3.0 V (min) or 4.5 V (min) depending on the user regulation voltage system selected.

9 Required to be supplied when 3.3 V regulator is disabled. See Section 4.5, “PMC/POR/LVI Electrical Specifications.”

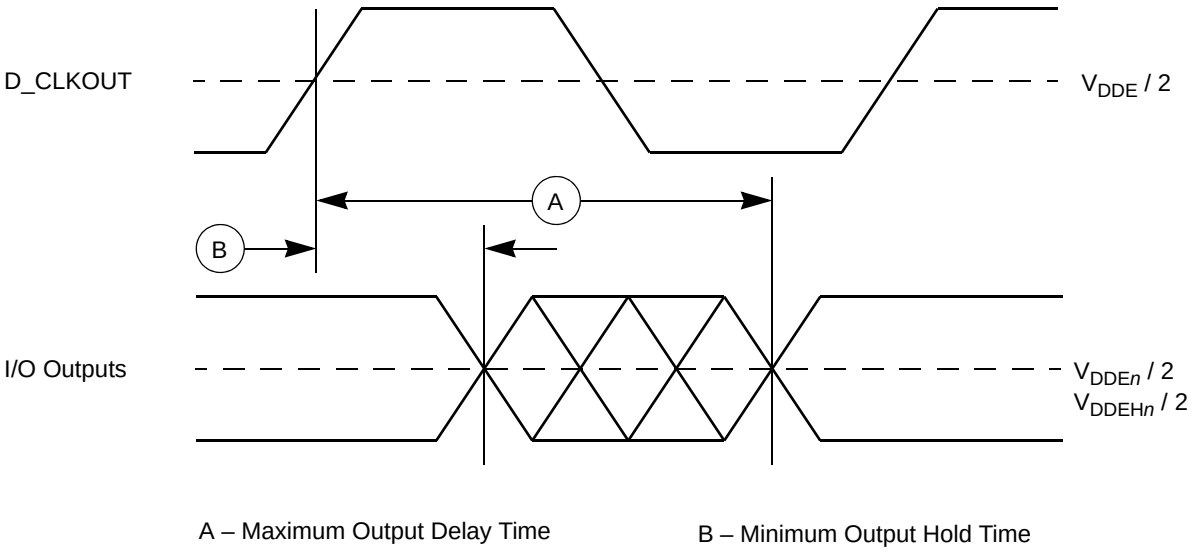


Figure 18. Generic Output Delay/Hold Timing

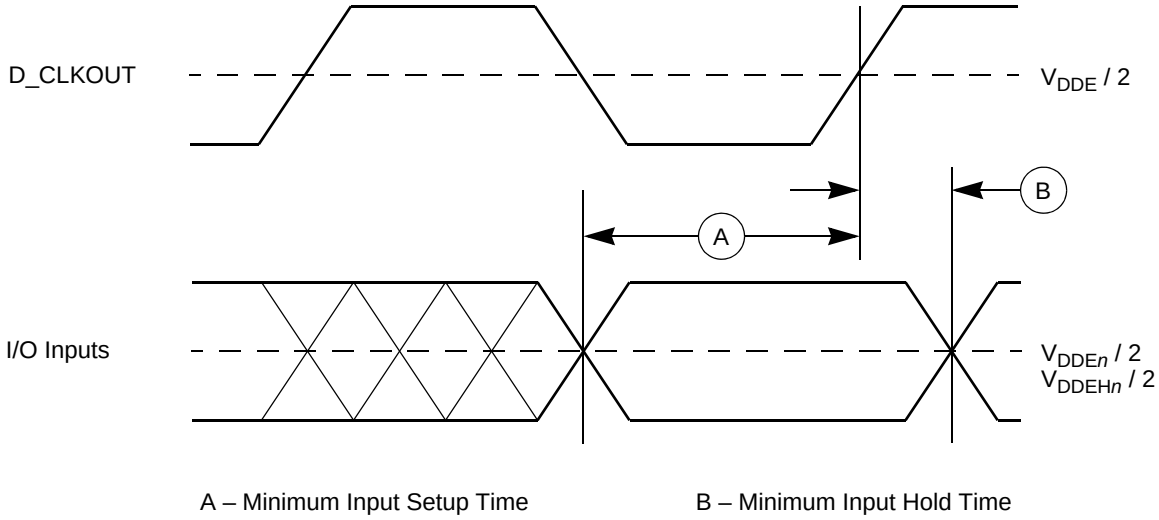


Figure 19. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 33. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1 Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

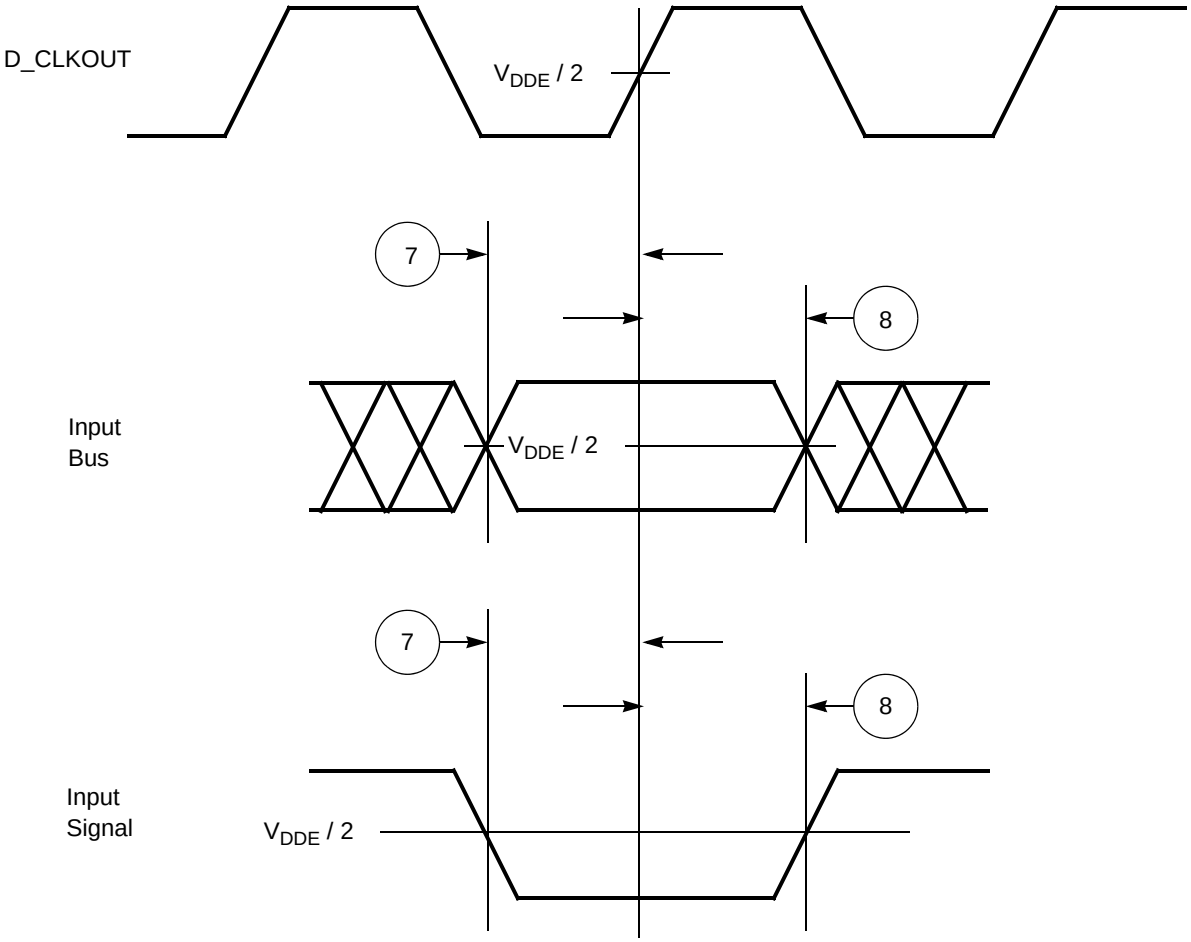


Figure 29. Synchronous Input Timing

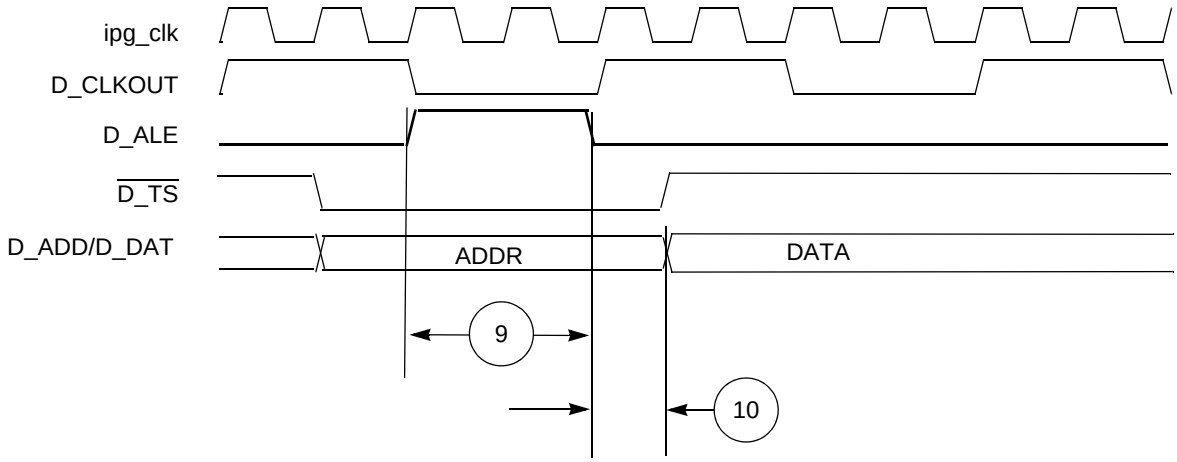


Figure 30. ALE Signal Timing

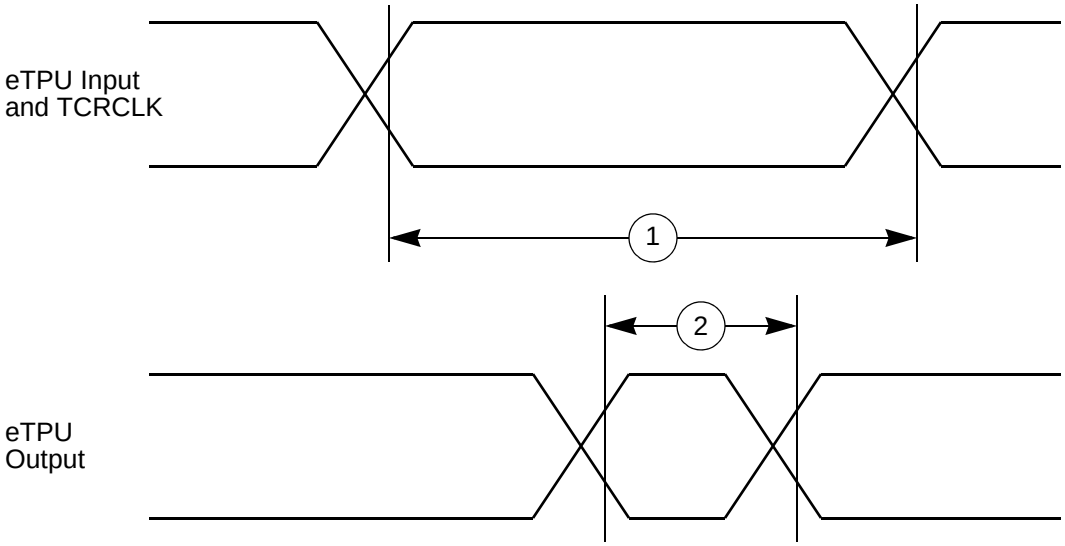


Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 39. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

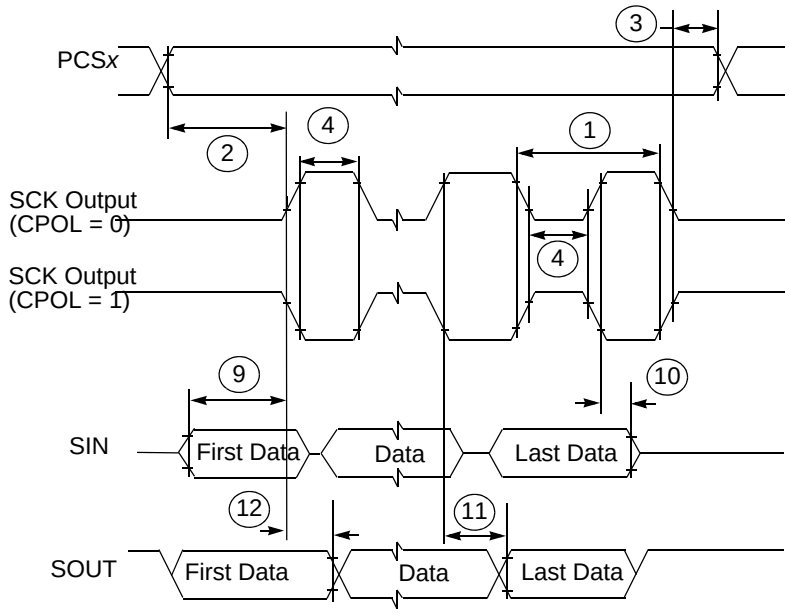


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

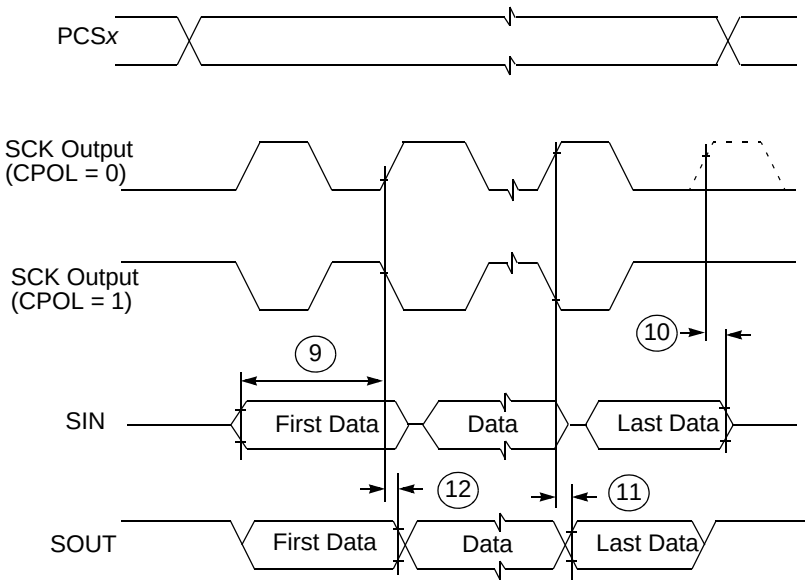


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

Table 43. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
eTPU_A												
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	K1	L1	K4
		A1	IRQ7	External interrupt request	I							
		A2	—	—	—							
		G	GPIO113	GPIO	I/O							
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO114	GPIO	I/O							
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO115	GPIO	I/O							
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO116	GPIO	I/O							
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO117	GPIO	I/O							
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO118	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
161	ETPUB14_ETPUB30_ GPIO161	P	ETPUB14	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L21	M25	R24
		A1	ETPUB30	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO161	GPIO	I/O							
162	ETPUB15_ETPUB31_ GPIO162	P	ETPUB15	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	M24	R25
		A1	ETPUB31	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO162	GPIO	I/O							
163	ETPUB16_PCSA1_ GPIO163	P	ETPUB16	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P20	U26	V24
		A1	PCSA1	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO163	GPIO	I/O							
164	ETPUB17_PCSA2_ GPIO164	P	ETPUB17	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R20	U25	T21
		A1	PCSA2	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO164	GPIO	I/O							
165	ETPUB18_PCSA3_ GPIO165	P	ETPUB18	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T20	U24	W26
		A1	PCSA3	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO165	GPIO	I/O							
166	ETPUB19_PCSA4_ GPIO166	P	ETPUB19	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T19	U23	W25
		A1	PCSA4	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO166	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27	AN27	—	B13	B13
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28	AN28	—	A13	A13
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29	AN29	—	B14	A14
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30	AN30	—	C14	B14
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31	AN31	—	D14	C14
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32	AN32	—	A14	B15
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33	AN33	—	B15	D14
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34	AN34	—	C15	C15
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35	AN35	—	D15	D15
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36	AN36	—	A15	A15
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37	AN37	—	C16	C17
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38	AN38	—	C17	D16
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39	AN39	—	D16	C16
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0	ANB0	B15	C18	C18
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1	ANB1	B16	D17	D17
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2	ANB2	A17	D18	D18
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3	ANB3	A18	D19	D19
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4	ANB4	B17	C19	B19
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5	ANB5	B18	C20	A20
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6	ANB6	A19	B19	C20
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7	ANB7	A20	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	ANB8	D13	B20	B20

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	ANB9	C14	D20	A21
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	ANB10	C13	B21	B21
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	ANB11	C15	A21	C21
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	ANB12	C16	C21	A22
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	ANB13	D14	D21	B22
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	ANB14	C17	A22	D20
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	ANB15	D15	B22	C22
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	ANB16	C18	C22	D21
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	ANB17	D16	A23	D22
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	ANB18	D17	B23	A23
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	ANB19	B19	C23	B23
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	ANB20	C19	D22	C23
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	ANB21	D18	A24	A24
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	ANB22	A21	B24	B24
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	ANB23	B20	A25	E20
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	VRH_A	A10	A12	A12
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	VRL_A	A11	A11	A11
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	VRH_B	A16	A19	A19
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	VRL_B	A15	A18	A18
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	REFBYPCB	B12	B18	B18
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	REFBYPCA	B11	B11	B11
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	VDDA_A0	A9	A9	A9
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	VDDA_A1	B9	B9	B9
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	REFBYPCA1	A12	A10	A10
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	VSSA_A1	B10	B10	B10
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	VDDA_B0	A13	A16	A16
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	VDDA_B1	B13	B16	B16

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AB5	AF4	AF4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO253	GPIO	I/O							
FlexCAN												
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AB17	AF19	AE19
		A1	TXDA	eSCI A transmit	O							
		A2	—	—	—							
		G	GPIO83	GPIO	I/O							
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up	—/Up	AA18	AE19	AD19
		A1	RXDA	eSCI A receive	I							
		A2	—	—	—							
		G	GPIO84	GPIO	I/O							
85	CNTXB_PCSC3_ GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V_{DDEH4}	—/Up	—/Up	Y18	AD19	AC19
		A1	PCSC3	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO85	GPIO	I/O							
86	CNRXB_PCSC4_ GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V_{DDEH4}	—/Up	—/Up	W18	AC19	AA19
		A1	PCSC4	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO86	GPIO	I/O							
87	CNTXC_PCSD3_ GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	W16	AF20	AF20
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO87	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up	—/Up	—	N1	L5
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO92	GPIO	I/O							
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	—	AF23	AF23
		A1	ETRIG0	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO244	GPIO	I/O							
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up	—/Up	—	AD22	AD22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO245	GPIO	I/O							
DSPI												
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y7	AD8	AB8
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO93	GPIO	I/O							
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up	—/Up	AA7	AF7	AE7
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO94	GPIO	I/O							
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up	—/Up	AB7	AD7	AC7
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO95	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
102	SCKB_ GPIO102	P	SCKB	DSPI B clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y8	AE8	AC8
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO102	GPIO	I/O							
103	SINB_ GPIO103	P	SINB	DSPI B data input	I	MH	V_{DDEH3}	—/Up	—/Up	AA8	AE9	AB9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO103	GPIO	I/O							
104	SOUTB_ GPIO104	P	SOUTB	DSPI B data output	O	MH	V_{DDEH3}	—/Up	—/Up	AB8	AF9	AA10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO104	GPIO	I/O							
105	PCSB0_PCSD2_ GPIO105	P	PCSB0	DSPI B peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y9	AD9	AF8
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO105	GPIO	I/O							
106	PCSB1_PCSD0_ GPIO106	P	PCSB1	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC9	AE8
		A1	PCSD0	DSPI D peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO106	GPIO	I/O							
107	PCSB2_SOUTC_ GPIO107	P	PCSB2	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	W7	AF8	AD8
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO107	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
273	D_ADD26_D_ADD_DAT26_ GPIO273	P	D_ADD26	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE11
		A1	D_ADD_DAT26	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO273	GPIO	I/O							
274	D_ADD27_D_ADD_DAT27_ GPIO274	P	D_ADD27	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF11
		A1	D_ADD_DAT27	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO274	GPIO	I/O							
275	D_ADD28_D_ADD_DAT28_ GPIO275	P	D_ADD28	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD12
		A1	D_ADD_DAT28	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO275	GPIO	I/O							
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB12
		A1	D_ADD_DAT29	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO276	GPIO	I/O							
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE12
		A1	D_ADD_DAT30	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO277	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO278	GPIO	I/O							
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO279	GPIO	I/O							
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO280	GPIO	I/O							
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO281	GPIO	I/O							
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO282	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO283	GPIO	I/O							
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO284	GPIO	I/O							
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO285	GPIO	I/O							
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO286	GPIO	I/O							
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO287	GPIO	I/O							