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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673fk0mvy2

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

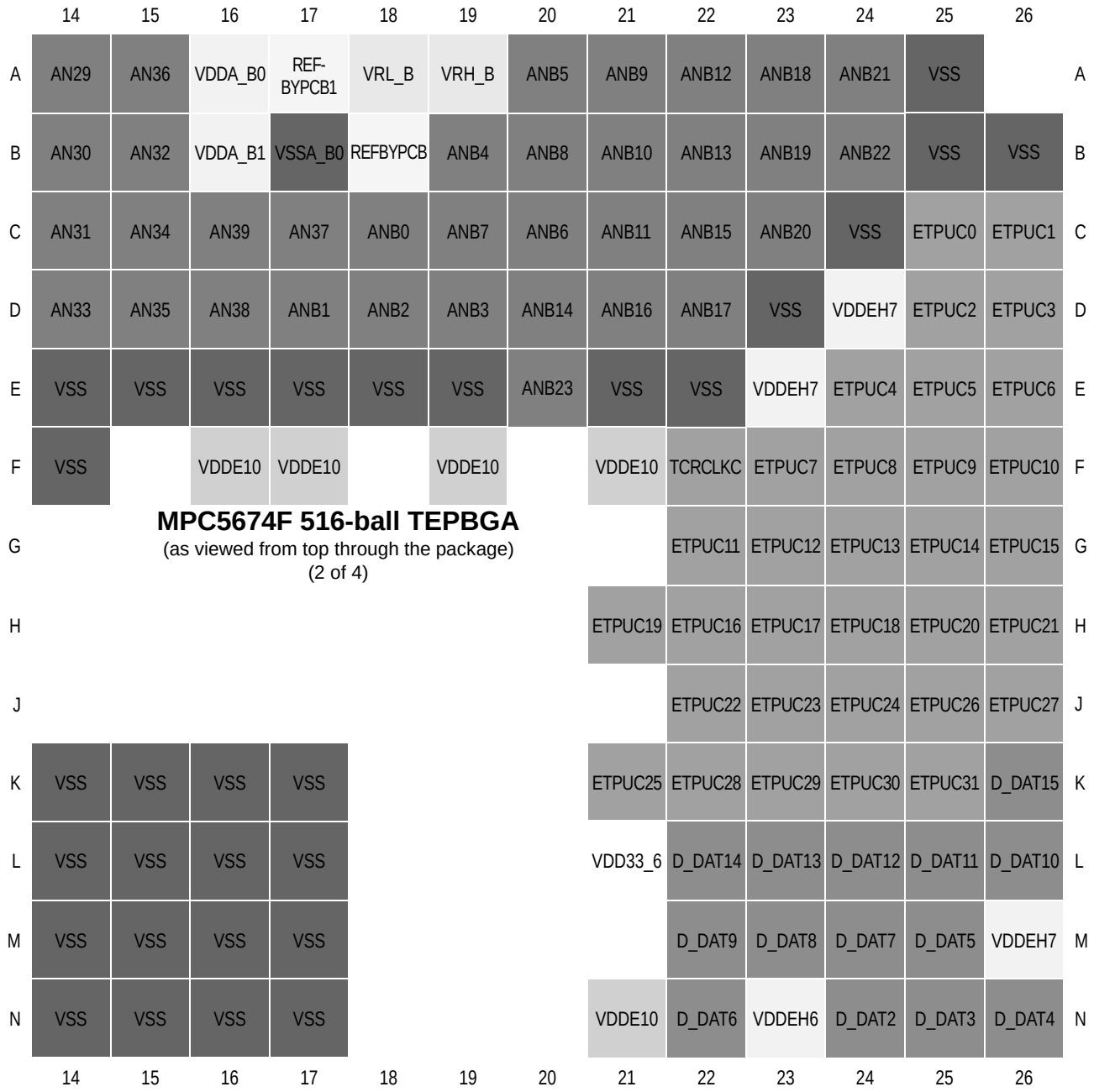

Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)

Table 10. PMC Operating conditions

Name	Parameter	Condition	Min	Typ	Max	Unit	Note
V_{DDREG}	Supply voltage VDDREG 5V nominal	LDO5V / SMPS5V mode	4.5	5	5.5	V	1
V_{DDREG}	Supply voltage VDDREG 3V nominal	LDO3V mode	3.0	3.3	3.6	V	1
V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3V nominal	LDO3V mode	3.0	3.3	3.6	V	2
V_{DD}	Core supply voltage	—	1.14	1.2	1.32	V	3

1 Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

2 Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

3 Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, "untrimmed” means “at reset" and "trimmed” means “after reset".

Table 11. PMC Electrical Specifications

ID	Name	Parameter	Min	Typ	Max	Unit
1	V_{BG}	Nominal bandgap reference voltage	0.608	0.620	0.632	V
1a	—	Untrimmed bandgap reference voltage	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
2	$V_{DD12OUT}$	Nominal VRC regulated 1.2V output VDD	—	1.27	—	V
2a	—	Untrimmed VRC 1.2V output variation before band gap trim (unloaded) **Note:** Voltage should be higher than maximum V_{LVD12} to avoid LVD event	$V_{DD12OUT}$ – 14%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	V
2b	—	Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max. 1A)[1]	$V_{DD12OUT}$ – 10%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 5%	V
2c	$V_{STEPV12}$	Trimming step $V_{DD12OUT}$	—	10	—	mV
3	V_{PORC}	POR rising VDD 1.2V	—	0.7	—	V
3a	—	POR VDD 1.2V variation	V_{PORC} – 30%	V_{PORC}	V_{PORC} + 30%	
3b	—	POR 1.2V hysteresis	—	75	—	mV
4	V_{LVD12}	Nominal rising LVD 1.2V **Note:** ~$V_{DD12OUT}$ × 0.87	—	1.100	—	V
4a	—	Untrimmed LVD 1.2V variation before band gap trim **Note:** Rising VDD	V_{LVD12} – 6%	V_{LVD12}	V_{LVD12} + 6%	V
4b	—	Trimmed LVD 1.2V variation after band gap trim Rising VDD	V_{LVD12} – 3%	V_{LVD12}	V_{LVD12} + 3%	V

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

4.6.2 Power-Down

If V_{DD} is powered down first, then all drivers are tristated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

4.6.3 Power Sequencing and POR Dependent on V_{DDA}

During power up or down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggers POR (ADC monitors on V_{DDEH1} segment which powers the RESET pin) if the leakage current path created, when V_{DDA} is sufficiently low, causes sufficient voltage drop on V_{DDEH1} node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially V_{DDEH1}) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since $V_{DD} = 1.32$ V max.

4.7 DC Electrical Specifications

Table 14. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (External Regulation)	V_{DD}	1.14	1.32[1,2]	V
1a	Core Supply Voltage (Internal Regulation)[3]	V_{DD}	1.08	1.32	V
2	I/O Supply Voltage (fast I/O pads)	V_{DDE}	3.0	3.6[1,4]	V
3	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	3.0	5.25[1,5]	V
4	3.3 V I/O Buffer Voltage	V_{DD33}	3.0	3.6[1,4]	V
5	Analog Supply Voltage	V_{DDA}	4.75	5.25[1,5]	V
6a	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_LOW}	0.95[6]	1.2	V
6b	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_HIGH}	2	6	V
7	Voltage Regulator Control Input Voltage[7]	V_{DDREG}	2.7[8]	5.5[1,5]	V

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 850 0.10 0.15	 mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[14] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[14] 7[15]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[16] 1.0 22	 mA mA mA

4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 22. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

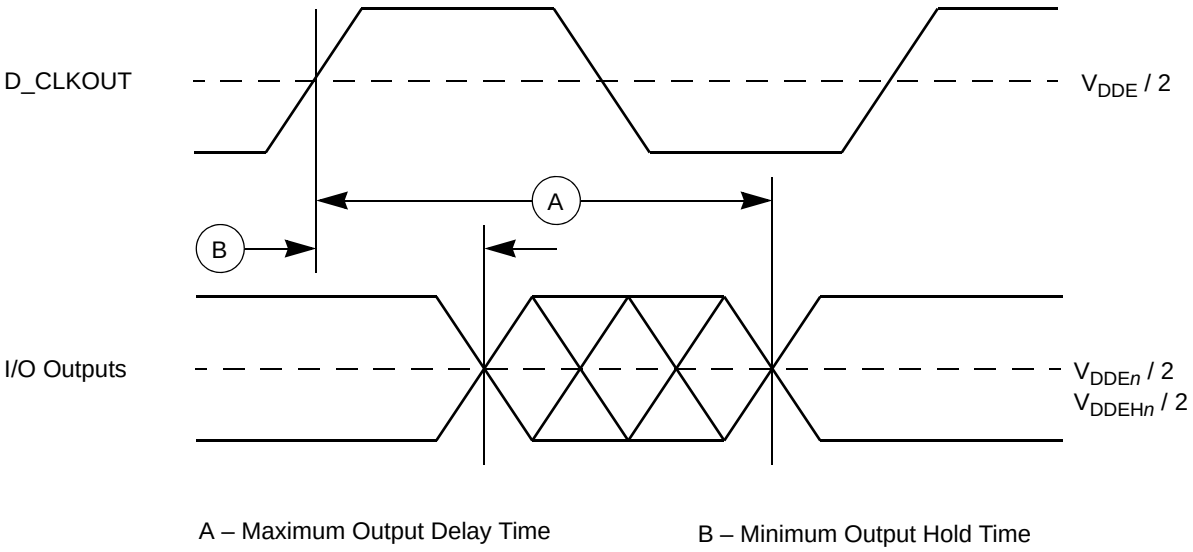

Figure 18. Generic Output Delay/Hold Timing

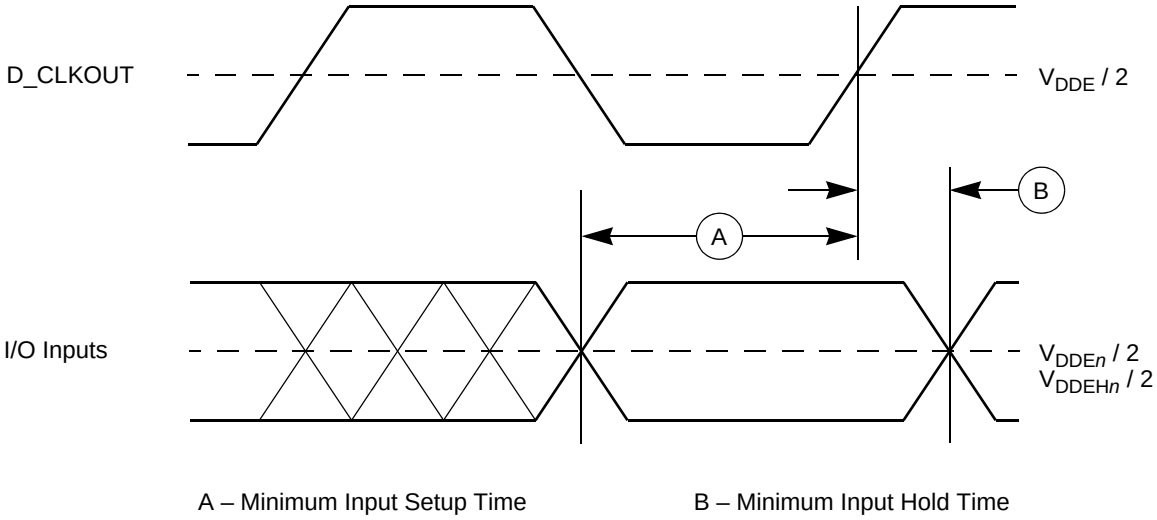

Figure 19. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 33. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1 Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

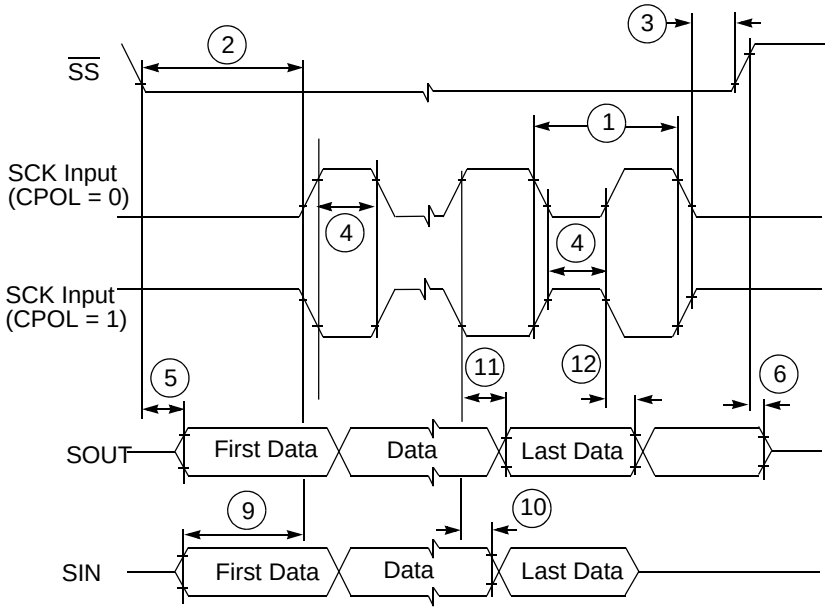

Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

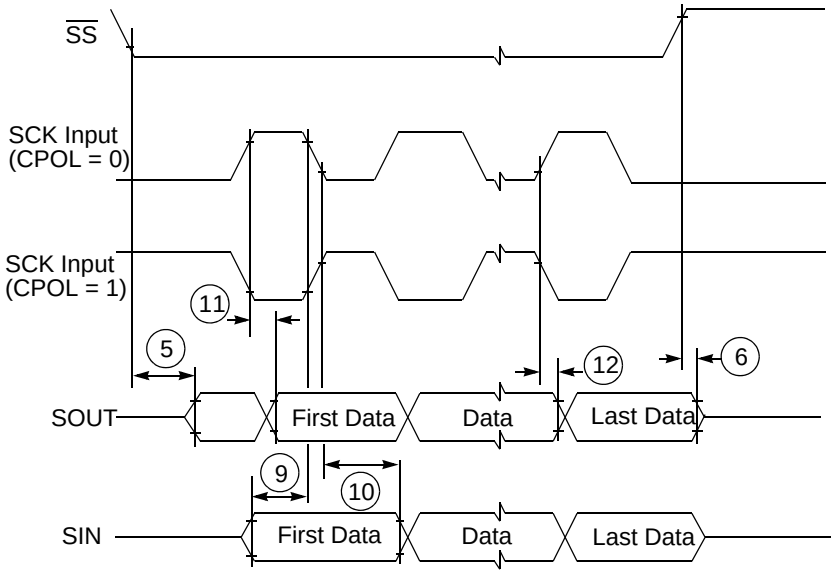

Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

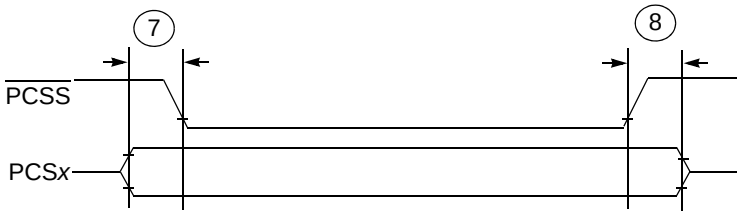

Figure 42. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

5.2 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 45 and Figure 46.

Figure 45. 416 TEPBGA Package (1 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	E1	E1
		A1	IRQ11	External interrupt request	I							
		A2	—	—	—							
		G	GPIO137	GPIO	I/O							
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E2	E2
		A1	IRQ12	External interrupt request	I							
		A2	—	—	—							
		G	GPIO138	GPIO	I/O							
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	E3	E3
		A1	IRQ13	External interrupt request	I							
		A2	—	—	—							
		G	GPIO139	GPIO	I/O							
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	E4	E4
		A1	IRQ14	External interrupt request	I							
		A2	—	—	—							
		G	GPIO140	GPIO	I/O							
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	D1	D1
		A1	IRQ15	External interrupt request	I							
		A2	—	—	—							
		G	GPIO141	GPIO	I/O							
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO142	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E21	G23	G22
		A1	IRQ2	External interrupt request	I							
		A2	—	—	—							
		G	GPIO452	GPIO	I/O							
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F19	G24	G23
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO453	GPIO	I/O							
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F21	G25	G24
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO454	GPIO	I/O							
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F20	G26	G25
		A1	IRQ5	External interrupt request	I							
		A2	—	—	—							
		G	GPIO455	GPIO	I/O							
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H23	G26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO456	GPIO	I/O							
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O							
		A2	—	—	—							
		G	GPIO457	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
464	ETPUC23_PCSD5_ GPIO464[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H20	K23	J23
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	MAA0	ADC A Mux Address 0	O							
		A3	MAB0	ADC B Mux Address 0	O							
		G	GPIO464	GPIO	I/O							
465	ETPUC24_PCSD4_ GPIO465[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J22	K24	J24
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	MAA1	ADC A Mux Address 1	O							
		A4	MAB1	ADC B Mux Address 1	O							
		G	GPIO465	GPIO	I/O							
466	ETPUC25_PCSD3_ GPIO466[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K22	K25	K21
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	MAA2	ADC A Mux Address 2	O							
		A3	MAB2	ADC B Mux Address 2	O							
		G	GPIO466	GPIO	I/O							
467	ETPUC26_PCSD2_ GPIO467[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J21	K26	J25
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO467	GPIO	I/O							
468	ETPUC27_PCSD1_ GPIO468[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J19	L23	J26
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO468	GPIO	I/O							
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J20	L24	K22
		A1	PCSD0	DSPI D peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO469	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
96	PCSA0_PCSD2_ GPIO96	P	PCSA0	DSPI A peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	AB6	AE6	AD6
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO96	GPIO	I/O							
97	PCSA1_ GPIO97	P	PCSA1	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC6	AC6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO97	GPIO	I/O							
98	PCSA2_ GPIO98	P	PCSA2	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC7	AF6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO98	GPIO	I/O							
99	PCSA3_ GPIO99	P	PCSA3	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AE7	AD7
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO99	GPIO	I/O							
100	PCSA4_ GPIO100	P	PCSA4	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AE5	AE5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO100	GPIO	I/O							
101	PCSA5_ETRIG1_ GPIO101	P	PCSA5	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AA6	AD6	AA8
		A1	ETRIG1	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO101	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB11
		A1	D_ADD_DAT21	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO268	GPIO	I/O							
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD10
		A1	D_ADD_DAT22	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO269	GPIO	I/O							
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE10
		A1	D_ADD_DAT23	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO270	GPIO	I/O							
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF10
		A1	D_ADD_DAT24	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO271	GPIO	I/O							
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD11
		A1	D_ADD_DAT25	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO272	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO288	GPIO	I/O							
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO289	GPIO	I/O							
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO290	GPIO	I/O							
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO291	GPIO	I/O							
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO292	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V_{DDE10}	—/Up	—/Up	—	—	P24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO299	GPIO	I/O							
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO300	GPIO	I/O							
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V_{DDE9}	—/Up	—/Up	—	—	AB10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO301	GPIO	I/O							
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V_{DDE8}	—/Up	—/Up	—	—	M2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO302	GPIO	I/O							
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO303	GPIO	I/O							
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO304	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
231	MDO12_GPIO231	–[13]	MDO12[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V1	AA1	Y5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO231	GPIO	I/O							
232	MDO13_GPIO232	–[13]	MDO13[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W2	AA2	AA1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO232	GPIO	I/O							
233	MDO14_GPIO233	–[13]	MDO14[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V3	AA3	AA2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO233	GPIO	I/O							
234	MDO15_GPIO234	–[13]	MDO15[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U4	Y4	AA3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO234	GPIO	I/O							
224	$\overline{\text{MSEO0}}$	–[13]	MSEO0[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	P2	U2	U6
225	$\overline{\text{MSEO1}}$	–[13]	MSEO1[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	N3	T3	U5
226	RDY	–[13]	RDY	Nexus ready output	O	F	V_{DDE2}	O/Low	RDY/HI	M4	R4	U3
—	TCK	–[13]	TCK	JTAG test clock input	I	F	V_{DDE2}	TCK/Down	TCK/Down	Y1	AB2	AB2
—	TDI	–[13]	TDI	JTAG test data input	I	F	V_{DDE2}	TDI/Up	TDI/Up	Y2	AC2	AC2
228	TDO	–[13]	TDO	JTAG test data output	O	F	V_{DDE2}	TDO/Up	TDO/Up	W1	AB1	AB1
—	TMS	–[13]	TMS	JTAG test mode select input	I	F	V_{DDE2}	TMS/Up	TMS/Up	W3	AB3	AB3
—	JCOMP	–[13]	JCOMP	JTAG TAP controller enable	I	F	V_{DDE2}	JCOMP/Down	JCOMP/Down	M1	R1	U2
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down	TEST/Down	B4	B4	B4
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I	VDDE	V_{DDSYN}	VDDSYN	VDDSYN	Y22	AD26	AD26

Appendix B Revision History

Table 47 describes the changes made to this document between revisions.

Table 47. Revision History

Revision (Date)	Description of changes
2 (Sept 2008)	Initial release, NDA Required.
3 (Nov 2009)	**Changes between Rev.2 and Rev. 3:**
	Added 516-pin package figures.
	Signals table: Updates throughout entire table.
	Updated Section 4.6, “Power Up/Down Sequencing”
	Updated features list. Updated flash PFCPR1 settings table. Fixed JTAG Test Clock Input Timing figure so the spec #’s in table matched figure.
	Updated Orderable Part numbers table.
	Moved signals table to be an appendix.
	Added 324-pin package thermals. Updated part numbers in orderable parts table (missing F: MPC5674F).
	FMPLL Electrical Spec table: Spec #1 changed min values of 4 to 8 Removed last sentence of footnote 2 Added note "Upper tolerance of less than 1% is allowed on 40MHz crystal."
	Oscillator Electrical Spec table: Moved predivider op. frequency spec from this table to the FMPLL Electrical Spec table Removed footnote #3 (since VDDE9 is an external supply and has no relation to the oscillator, PMC, or PLL).
	Added maximum solder temperature to Absolute Max Ratings table.
	PMC Operating Conditions table: Removed JTemp row. Changed VDDR to VDDREG (naming consistency) Changed VDD12 to VDD (naming consistency)
	PMC Electrical Spec table: Added VDDREG to this parameter “Trimmed bandgap reference voltage / voltage dependence (V_{DDREG})” Changed VDDSTEP to LVDSTEP12 (naming consistency)
	Added two conditons to the opening statements of Section 4.6, “Power Up/Down Sequencing.”
	DC Electrical Specifications table: spec #9 (Fast I/O Input High Voltage) spec #10 (Fast I/O Input Low Voltage) spec #24 (Operating Current 1.2 V Supplies; IDD) spec #25 (Operating Current 3.3 V Supplies; IDDSYN) spec #32 (Analog Input Current, Channel Off; IINACT_A) footnote #12 ("IOH_S = {11.6} mA...")