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Details

Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673fk0mvy2r

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VDD	RSTOUT	ANA0	ANA1	ANA4	ANA5	ANA15	VDDA_A0	VRH_A	VRL_A	REF-BYPCB1	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA2	ANA3	ANA6	ANA7	VDDA_A0	VSSA_A1	REF-BYPCA	REF-BYPCB	VDDA_B1	VSSA_B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ETPUA21	ETPUA26	VSS	VDD	ANA8	ANA10	ANA9	ANA13	ANA17	ANA19	ANA21	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ETPUA23	ETPUA25	ETPUA31	VSS	VDD	ANA11	ANA12	ANA14	ANA16	ANA18	ANA20	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
E	ETPUA20	ETPUA22	ETPUA24	ETPUA30															ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
F	ETPUA13	ETPUA14	ETPUA15	ETPUA27															ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
G	ETPUA10	ETPUA11	ETPUA12	ETPUA17															ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
H	ETPUA5	ETPUA6	ETPUA9	ETPUA16															VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA3	ETPUA4															ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	TCRCLKA	ETPUA0	VDD	VSTBY															ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	BOOT-CFG1	PLLCFG1	PLLCFG2	VDDEH1															ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	JCOMP	RESET	PLLCFG0	RDY															ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VDDE2	MCKO	MSE01	EVT1															ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	EVT0	MSE00	MDO0	MDO1															TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
R	MDO2	MDO3	MDO4	MDO5															ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
T	MDO6	MDO7	MDO8	VDDE2															ETPUB19	ETPUB18	VDDEH6	REGCTL	T
U	MDO9	MDO10	MDO11	MDO15															ETPUB31	ETPUB30	VDDREG	VSSSYN	U
V	MDO12	VDDE2	MDO14	VDD33_2															VDD	REGSEL	VSSFL	EXTAL	V
W	TDO	MDO13	TMS	VSS	VDD	VDDE2	PCSB2	VDDEH4	VDD	EMIOS8	EMIOS9	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	TCK	TDI	VSS	VDD	FR_A_TX	FR_B_TX	SCKA	SCKB	PCSB0	EMIOS2	EMIOS5	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	ENGCLK	VSS	VDD	FR_A_RX	FR_B_RX	PCSA5	SINA	SINB	EMIOS0	EMIOS3	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	VSS	VDD	FR_A_TX_EN	VDDE2	FR_B_TX_EN	PCSA0	SOUTA	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB

MPC5674F 324 TEPBGA
(as viewed from top through the package)

VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VDDE2	VSS	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VSS	VSS	VSS	VSS

Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0	ANA4	ANA8	ANA11	ANA15	VDDA_A0	REF-BYPCA1	VRL_A	VRH_A	AN28	AN32	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REF-BYPCA	AN24	AN27	AN29	AN33	VDDA_B1	VSSA_B0	REF-BYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLK	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA9	ANA13	ANA17	ANA19	ANA21	ANA23	AN26	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA7	ANA12	ANA16	ANA18	ANA20	ANA22	AN25	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6																			ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2																			ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VDD33_1	TXDA	RXDA	VSTBY																			ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOT-CFG1	WKPCFG	VDD																			VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1																			ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VDDE2	RESET	PLLCFG0	BDV																			ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MDIO0	MDIO1	MDIO2																			TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	MDIO3	MDIO4	MDIO5	MDIO6																			ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDIO7	MDIO8	MDIO9	MDIO10																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDIO11	MDIO12	MDIO13	MDIO14																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDIO15	MDIO16	MDIO17	MDIO18																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDIO19	MDIO20	MDIO21	MDIO22																			VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSFL	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)

VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS
VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS

Figure 6. MPC5674F 416-ball TEPBGA (full diagram)

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current¹ (continued)

Spec	Pad Type	Symbol	Frequency (MHz)	Load ² (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
9	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.7
10			50	50	3.6	10	6.7
11			33.33	50	3.6	01	4.2
12			20	50	3.6	00	2.6
13			20	200	3.6	00	9.1

¹ These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

² All loads are lumped.

4.7.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The V_{DD33} current draw on fast speed pads can be calculated from Table 16 dependent on the voltage, frequency, and load on all F type pins. The V_{DD33} current draw on medium pads can be calculated from Table 16 dependent on voltage and independent on the frequency and load on all MH type pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 16.

The AC timing of these pads are described in the Section 4.11.2, “Pad AC Specifications.”

Table 16. V_{DD33} Pad Average DC Current¹

Spec	Pad Type	Symbol	Frequency (MHz)	Load ² (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{33_MH}	—	—	3.6	5.5	—	0.0007
2	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.92
3			66	20	3.6	3.6	01	1.14
4			66	30	3.6	3.6	10	1.50
5			66	50	3.6	3.6	11	2.19
6	Fast w/ Slew Control	I_{33_FSR}	66	50	3.6	3.6	11	0.74
7			50	50	3.6	3.6	10	0.52
8			33.33	50	3.6	3.6	00	0.19
9			20	50	3.6	3.6	00	0.19
10			20	200	3.6	3.6	00	0.19

¹ These are average IDDE for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

² All loads are lumped.

Table 19. Oscillator Electrical Specifications¹
($V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}$, $V_{SS} = V_{SSSYN} = 0 \text{ V}$, $T_A = T_L \text{ to } T_H$)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Crystal Mode Differential Amplitude ² (Min differential voltage between EXTAL and XTAL)	$V_{\text{crystal_diff_amp}}$	$ V_{\text{extal}} - V_{\text{xtal}} > 0.4 \text{ V}$	—	V
2	Crystal Mode: Internal Differential Amplifier Noise Rejection	$V_{\text{crystal_diff_amp_nr}}$	—	$ V_{\text{extal}} - V_{\text{xtal}} < 0.2 \text{ V}$	V
3	EXTAL Input High Voltage Bypass mode, External Reference	V_{IHEXT}	$((V_{DD33}/2) + 0.4 \text{ V})$	—	V
4	EXTAL Input Low Voltage Bypass mode, External Reference	V_{ILEXT}	—	$(V_{DD33}/2) - 0.4 \text{ V}$	V
5	XTAL Current ³	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	$C_{\text{S_XTAL}}$	—	1.5	pF
7	Total On-chip stray capacitance on EXTAL	$C_{\text{S_EXTAL}}$	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	$C_{\text{L_EXTAL}}$	—	$(2 \times C_L - C_{\text{S_EXTAL}} - C_{\text{PCB_EXTAL}})$ ⁴	pF
10	Discrete load capacitance to be connected to XTAL	$C_{\text{L_XTAL}}$	—	$(2 \times C_L - C_{\text{S_XTAL}} - C_{\text{PCB_XTAL}})$ ⁴	pF

¹ All values given are initial design targets and subject to change.

² This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{\text{extal}} - V_{\text{xtal}} \geq 400 \text{ mV}$ criterion has to be met for oscillator's comparator to produce output clock.

³ I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

⁴ $C_{\text{PCB_EXTAL}}$ and $C_{\text{PCB_XTAL}}$ are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

4.9 eQADC Electrical Characteristics

Table 20. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles Single Ended Conversion Cycles 12 bit resolution Single Ended Conversion Cycles 10 bit resolution Single Ended Conversion Cycles 8 bit resolution Note: Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here.	CC	2 + 14 2 + 12 2 + 10	128 + 14 128 + 12 128 + 10	ADCLK cycles
3	Stop Mode Recovery Time ¹	T_{SR}	10	—	μs
4	Resolution ²	—	1.25	—	mV
5	INL: 8 MHz ADC Clock ³	INL8	-4^4	4^4	LSB ⁵
6	INL: 16 MHz ADC Clock ³	INL16	-8^4	8^4	LSB
7	DNL: 8 MHz ADC Clock ³	DNL8	-3^4	3^4	LSB
8	DNL: 16 MHz ADC Clock ³	DNL16	-3^4	3^4	LSB

4.12.4 Nexus Timing

Table 35. Nexus Debug Port Timing¹

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2 ²	8	t_{CYC} ³
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid ⁴	t_{MDOV}	−0.1	0.2	t_{MCYC}
4	MCKO Low to MSEO Data Valid ⁴	t_{MSEOV}	−0.1	0.2	t_{MCYC}
5	MCKO Low to EVTO Data Valid ⁴	t_{EVTOV}	−0.1	0.2	t_{MCYC}
6	EVTI Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC} ³
7	EVTO Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4 ⁵	—	t_{CYC} ³
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	RDY Valid to MCKO ⁶	—	—	—	—

¹ All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{DD} = 1.08\text{ V}$ to 1.32 V , $V_{DDE} = 3.0\text{ V}$ to 3.6 V , V_{DD33} and $V_{DDSYN} = 3.0\text{ V}$ to 3.6 V , $T_A = T_L$ to T_H , and $C_L = 30\text{ pF}$ with $DSC = 0b10$.

² The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

³ See Notes on t_{cyc} in Table 28 in Section 4.11.1 Clocking.

⁴ MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.

⁵ Lower frequency is required to be fully compliant to standard.

⁶ The RDY pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

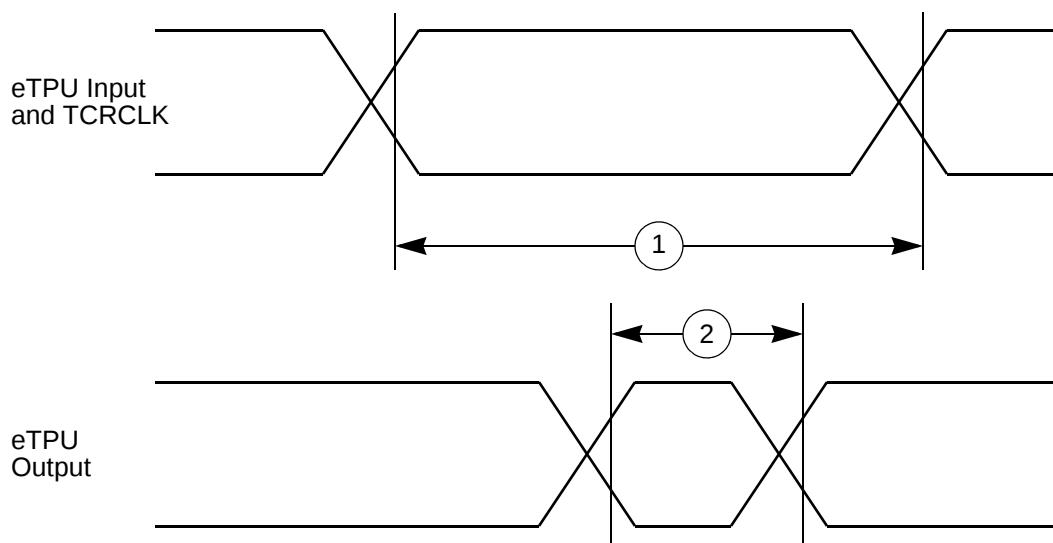


Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 39. eMIOS Timing¹

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}^2
2	eMIOS Output Pulse Width	t_{MOPW}	1 ³	—	t_{cyc}^2

¹ eMIOS timing specified at $V_{DD} = 1.08\text{ V}$ to 1.32 V , $V_{DDEH} = 3.0\text{ V}$ to 5.5 V , V_{DD33} and $V_{DDSYN} = 3.0\text{ V}$ to 3.6 V , $T_A = T_L$ to T_H , and $C_L = 50\text{ pF}$ with $SRC = 0b00$.

² See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

³ This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Table 40. DSPI Timing^{1 2} (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs	t_{SUI}			
	Master (MTFE = 0)		20	—	ns
	Slave		4	—	ns
	Master (MTFE = 1, CPHA = 0) ⁸		6	—	ns
	Master (MTFE = 1, CPHA = 1)		20	—	ns
10	Data Hold Time for Inputs	t_{HI}			
	Master (MTFE = 0)		–3	—	ns
	Slave		7	—	ns
	Master (MTFE = 1, CPHA = 0) ⁸		12	—	ns
	Master (MTFE = 1, CPHA = 1)		–3	—	ns
11	Data Valid (after SCK edge)	t_{SUO}			
	Master (MTFE = 0)		—	5	ns
	Slave		—	25	ns
	Master (MTFE = 1, CPHA = 0)		—	13	ns
	Master (MTFE = 1, CPHA = 1)		—	5	ns
12	Data Hold Time for Outputs	t_{HO}			
	Master (MTFE = 0)		–5	—	ns
	Slave		2.5	—	ns
	Master (MTFE = 1, CPHA = 0)		3	—	ns
	Master (MTFE = 1, CPHA = 1)		–5	—	ns

¹ DSPI timing specified at $V_{DD} = 1.08\text{ V}$ to 1.32 V , $V_{DDEH} = 3.0\text{ V}$ to 5.5 V , V_{DD33} and $V_{DDSYN} = 3.0\text{ V}$ to 3.6 V , and $T_A = T_L$ to T_H

² Speed is the nominal maximum frequency of platform clock (f_{platt}). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock (f_{sys}) + 2% FM.

³ The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

⁴ The actual minimum SCK cycle time is limited by pad performance.

⁵ The maximum value is programmable in DSPI_CTAR n [PSSCK] and DSPI_CTAR n [CSSCK].

⁶ The maximum value is programmable in DSPI_CTAR n [PASC] and DSPI_CTAR n [ASC].

⁷ For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

⁸ This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 41. DSPI LVDS Timing^{1, 2}

Characteristic	Symbol	Min	Max	Unit
LVDS Clock to Data/Chip Select Outputs	$t_{LVDS\text{DATA}}$	$-0.25 \times t_{SCYC}$	$+0.25 \times t_{SCYC}$	ns

¹ These are typical values that are estimated from simulation.

² See DSPI LVDS Pad related data in Table 17.

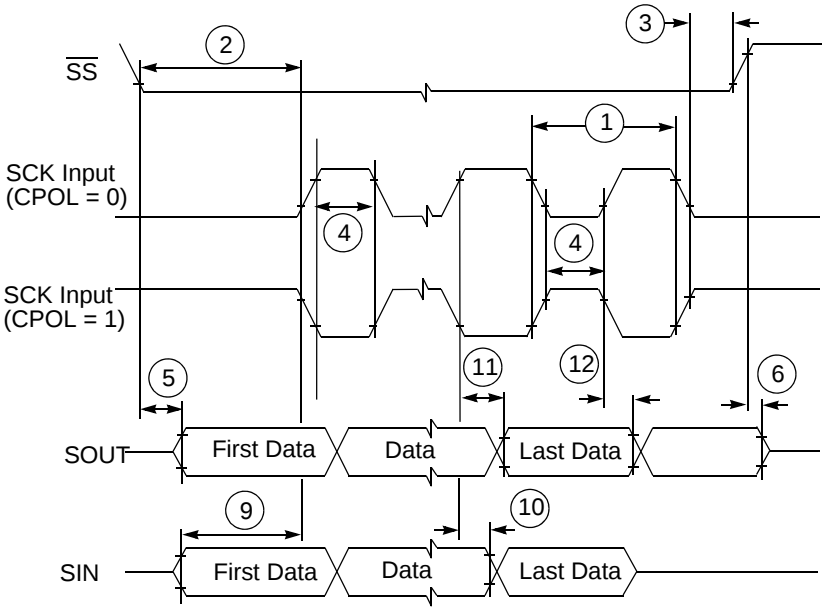


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

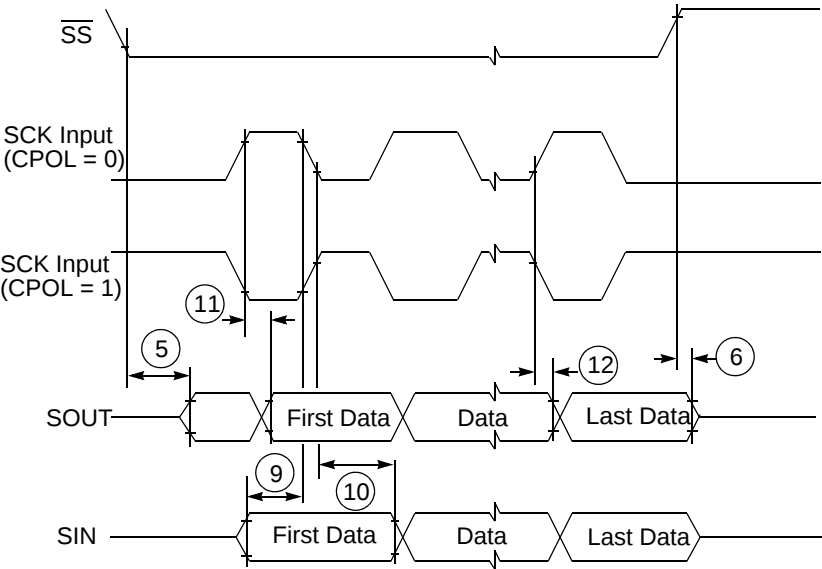


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

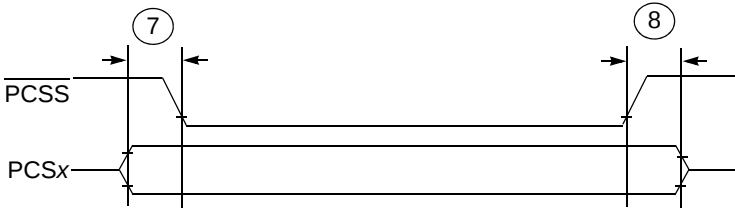


Figure 42. DSPI PCS Strobe (PCSS) Timing

5.3 516-Pin Package

The package drawings of the 516-pin TEPBGA package are shown in Figure 47 and Figure 48.

Figure 47. 516 TEPBGA Package (1 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	H1	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO119	GPIO	I/O							
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	H2	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO120	GPIO	I/O							
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	J1	H2
		A1	ETPUA19	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO121	GPIO	I/O							
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	J2	H3
		A1	ETPUA20	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO122	GPIO	I/O							
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	H3	J3	J3
		A1	ETPUA21	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO123	GPIO	I/O							
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	G1	J4	K6
		A1	ETPUA22	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO124	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO131	GPIO	I/O							
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO132	GPIO	I/O							
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO133	GPIO	I/O							
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	E1	F2	F2
		A1	IRQ8	External interrupt request	I							
		A2	—	—	—							
		G	GPIO134	GPIO	I/O							
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	C1	F3	F3
		A1	IRQ9	External interrupt request	I							
		A2	—	—	—							
		G	GPIO135	GPIO	I/O							
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	E2	F4	F4
		A1	IRQ10	External interrupt request	I							
		A2	—	—	—							
		G	GPIO136	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
452	ETPUC11_IRQ2_ GPIO452 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	E21	G23	G22
		A1	IRQ2	External interrupt request	I							
		A2	—	—	—							
		G	GPIO452	GPIO	I/O							
453	ETPUC12_IRQ3_ GPIO453 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	F19	G24	G23
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO453	GPIO	I/O							
454	ETPUC13_3_IRQ4_ GPIO454 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	F21	G25	G24
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO454	GPIO	I/O							
455	ETPUC14_4_IRQ5_ GPIO455 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	F20	G26	G25
		A1	IRQ5	External interrupt request	I							
		A2	—	—	—							
		G	GPIO455	GPIO	I/O							
456	ETPUC15_ GPIO456 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	—	H23	G26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO456	GPIO	I/O							
457	ETPUC16_FR_A_TX_ GPIO457 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	—	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O							
		A2	—	—	—							
		G	GPIO457	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
188	EMIOS9_ETPUA9_GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	W11	AD13	AF15
		A1	ETPUA9	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO188	GPIO	I/O							
189	EMIOS10_SCKD_GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AA11	AE13	AE15
		A1	SCKD	DSPI D clock	O							
		A2	—	—	—							
		G	GPIO189	GPIO	I/O							
190	EMIOS11_SIND_GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AB12	AF13	AB14
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO190	GPIO	I/O							
191	EMIOS12_SOUTC_GPIO191	P	EMIOS12	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AB13	AF14	AD15
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO191	GPIO	I/O							
192	EMIOS13_SOUTD_GPIO192	P	EMIOS13	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AA12	AE14	AC15
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO192	GPIO	I/O							
193	EMIOS14_IRQ0_GPIO193	P	EMIOS14	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	Y12	AC14	AF17
		A1	IRQ0	External interrupt request	I							
		A2	CNTXD	FlexCAN D transmit	O							
		G	GPIO193	GPIO	I/O							

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V _{DDEH1}	—/Up	—/Up	—	N1	L5
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO92	GPIO	I/O							
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V _{DDEH4}	—/Up	—/Up	—	AF23	AF23
		A1	ETRIG0	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO244	GPIO	I/O							
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V _{DDEH5}	—/Up	—/Up	—	AD22	AD22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO245	GPIO	I/O							
DSPI												
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V _{DDEH3}	—/Up	—/Up	Y7	AD8	AB8
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO93	GPIO	I/O							
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V _{DDEH3}	—/Up	—/Up	AA7	AF7	AE7
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO94	GPIO	I/O							
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V _{DDEH3}	—/Up	—/Up	AB7	AD7	AC7
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO95	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AB11
		A1	D_ADD_DAT21	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO268	GPIO	I/O							
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AD10
		A1	D_ADD_DAT22	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO269	GPIO	I/O							
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AE10
		A1	D_ADD_DAT23	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO270	GPIO	I/O							
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AF10
		A1	D_ADD_DAT24	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO271	GPIO	I/O							
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AD11
		A1	D_ADD_DAT25	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO272	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	L26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO288	GPIO	I/O							
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	L25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO289	GPIO	I/O							
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	L24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO290	GPIO	I/O							
291	D_ADD_DAT13_ GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	L23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO291	GPIO	I/O							
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	L22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO292	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V _{DDE10}	—/Up	—/Up	—	—	P24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO299	GPIO	I/O							
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AF9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO300	GPIO	I/O							
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V _{DDE9}	—/Up	—/Up	—	—	AB10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO301	GPIO	I/O							
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V _{DDE8}	—/Up	—/Up	—	—	M2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO302	GPIO	I/O							
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V _{DDE8}	—/Up	—/Up	—	—	N2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO303	GPIO	I/O							
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V _{DDE8}	—/Up	—/Up	—	—	N3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO304	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	P1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO305	GPIO	I/O							
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	P2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO306	GPIO	I/O							
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	P3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO307	GPIO	I/O							
Reset and Clocks												
—	RESET	P	RESET	External reset input	I	MH	V _{DDEH1}	RESET/Up	RESET/Up	M2	R2	N5
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V _{DDEH1}	RSTOUT/Low	RSTOUT/High	A3	A3	A3
211	BOOTCFG0_IRQ2_GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V _{DDEH1}	BOOTCFG/Down	BOOTCFG/Down	—	—	L4
		A1	IRQ2		I							
		A2	—	—	—							
		G	GPIO211	GPIO	I/O							
212	BOOTCFG1_IRQ3_GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V _{DDEH1}	BOOTCFG/Down	Input/Down	L1	N2	L3
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO212	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V _{DDSYN}	VSSSYN	VSSSYN	U22	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V _{DDEH1}	VSTBY	VSTBY	K4	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V _{DDREG}	REGSEL	REGSEL	V20	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V _{DDREG}	REGCTL	REGCTL	T22	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V _{SS}	I	VSS	V _{DDREG}	VSSFL	VSSFL	V21	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V _{DDREG}	VDDREG	VDDREG	U21	AA25	AA25

¹ The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

² The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

³ P/A/G stands for Primary/Alternate/GPIO. This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

⁴ Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

⁵ MH = High voltage, medium speed

F = Fast speed

FS = Fast speed with slew

AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)

VHV = Very high voltage

⁶ VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

⁷ The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

⁸ The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

⁹ This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU_C.

¹⁰ During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

¹¹ NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.