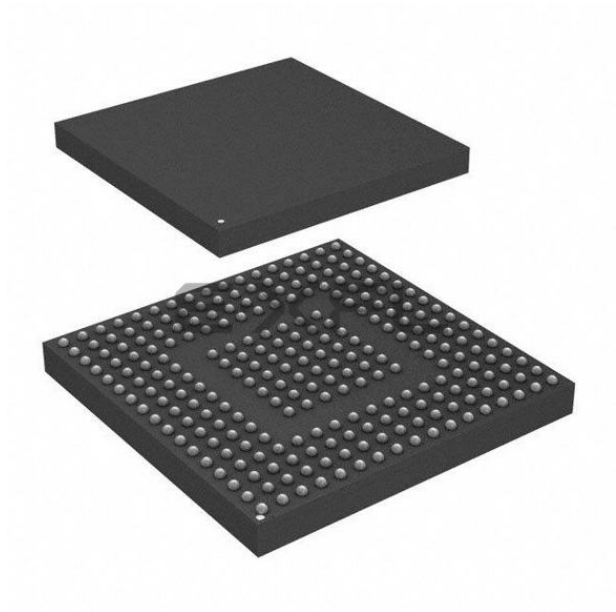


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673kavmm1

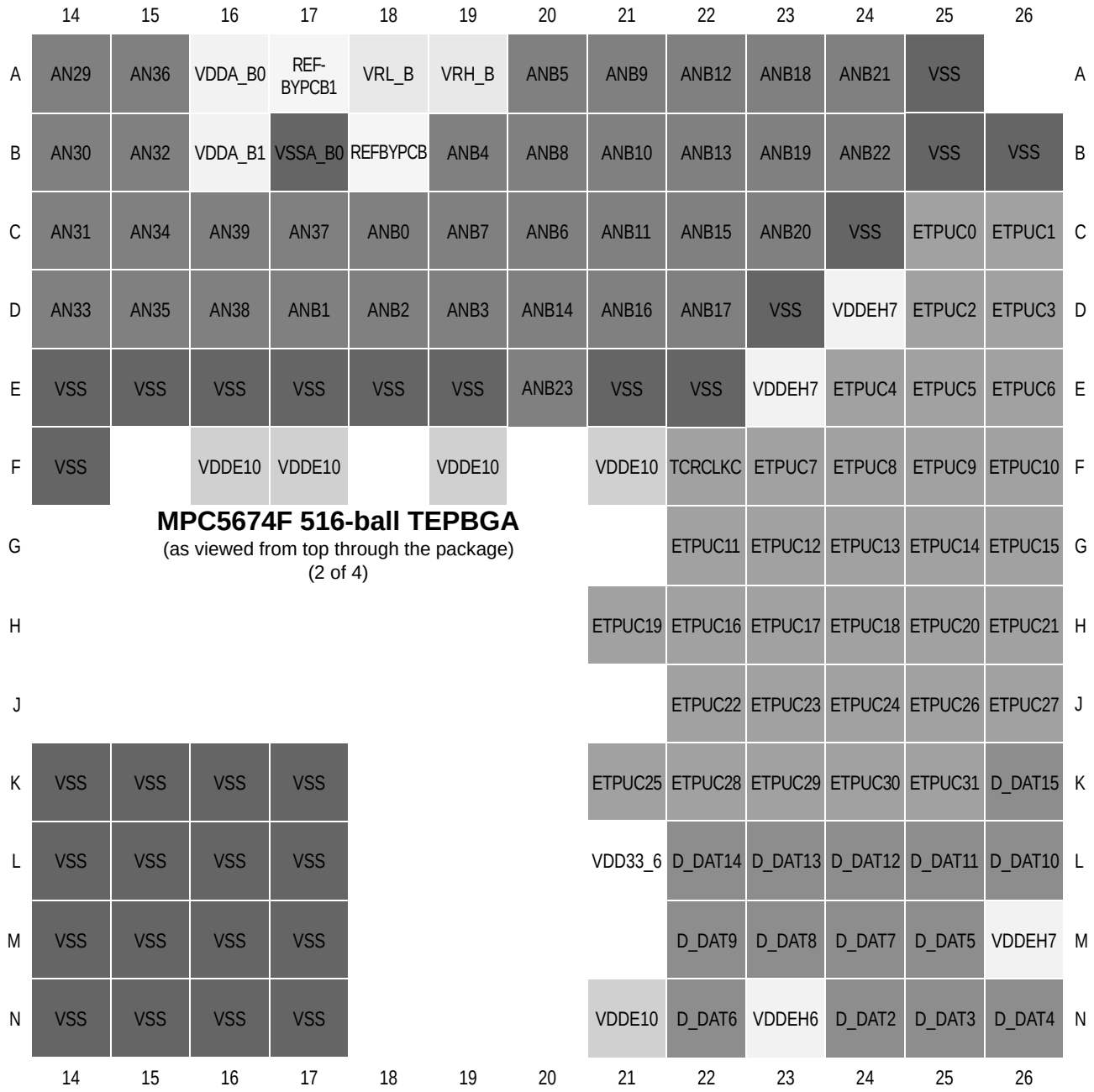


Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

Table 10. PMC Operating conditions

Name	Parameter	Condition	Min	Typ	Max	Unit	Note
V_{DDREG}	Supply voltage VDDREG 5V nominal	LDO5V / SMPS5V mode	4.5	5	5.5	V	1
V_{DDREG}	Supply voltage VDDREG 3V nominal	LDO3V mode	3.0	3.3	3.6	V	1
V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3V nominal	LDO3V mode	3.0	3.3	3.6	V	2
V_{DD}	Core supply voltage	—	1.14	1.2	1.32	V	3

1 Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

2 Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

3 Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, "untrimmed” means “at reset" and "trimmed” means “after reset".

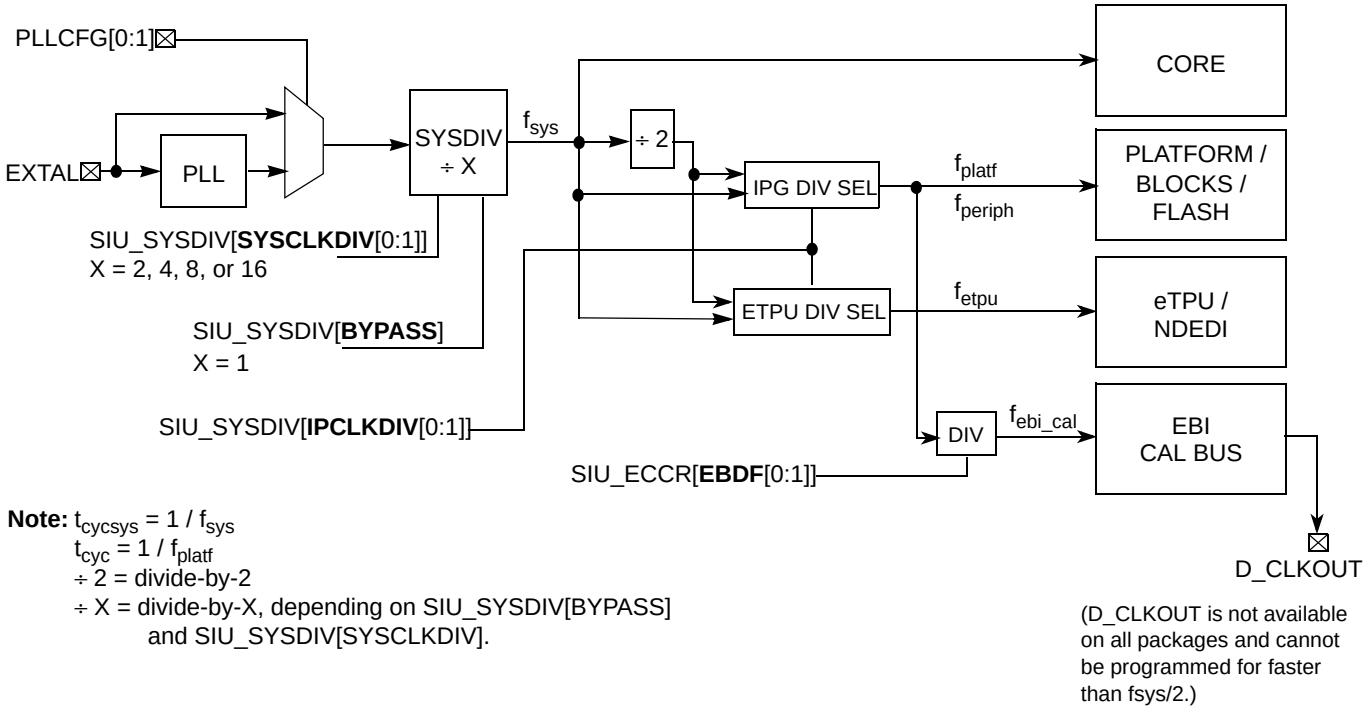
Table 11. PMC Electrical Specifications

ID	Name	Parameter	Min	Typ	Max	Unit
1	V_{BG}	Nominal bandgap reference voltage	0.608	0.620	0.632	V
1a	—	Untrimmed bandgap reference voltage	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
2	$V_{DD12OUT}$	Nominal VRC regulated 1.2V output VDD	—	1.27	—	V
2a	—	Untrimmed VRC 1.2V output variation before band gap trim (unloaded) **Note:** Voltage should be higher than maximum V_{LVD12} to avoid LVD event	$V_{DD12OUT}$ – 14%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	V
2b	—	Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max. 1A)[1]	$V_{DD12OUT}$ – 10%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 5%	V
2c	$V_{STEPV12}$	Trimming step $V_{DD12OUT}$	—	10	—	mV
3	V_{PORC}	POR rising VDD 1.2V	—	0.7	—	V
3a	—	POR VDD 1.2V variation	V_{PORC} – 30%	V_{PORC}	V_{PORC} + 30%	
3b	—	POR 1.2V hysteresis	—	75	—	mV
4	V_{LVD12}	Nominal rising LVD 1.2V **Note:** ~$V_{DD12OUT}$ × 0.87	—	1.100	—	V
4a	—	Untrimmed LVD 1.2V variation before band gap trim **Note:** Rising VDD	V_{LVD12} – 6%	V_{LVD12}	V_{LVD12} + 6%	V
4b	—	Trimmed LVD 1.2V variation after band gap trim Rising VDD	V_{LVD12} – 3%	V_{LVD12}	V_{LVD12} + 3%	V

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.



Note: $t_{cycsys} = 1 / f_{sys}$
$t_{cyc} = 1 / f_{platf}$
÷ 2 = divide-by-2
÷ X = divide-by-X, depending on SIU_SYSDIV[BYPASS] and SIU_SYSDIV[SYSCLKDIV].

(D_CLKOUT is not available on all packages and cannot be programmed for faster than fsys/2.)

Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

Table 32. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

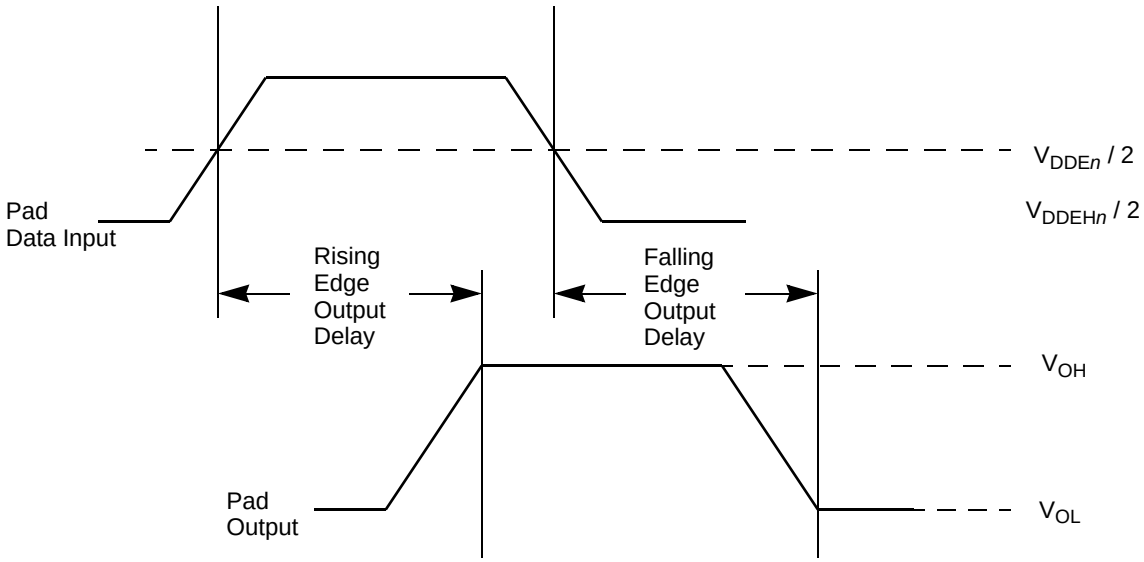


Figure 17. Pad Output Delay

4.12 AC Timing

4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 18 and Figure 19 apply to all I/O pins with pad types F and MH. See Appendix A, Signal Properties and Muxing, for the pad type for each pin.

4.12.4 Nexus Timing

Table 35. Nexus Debug Port Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2[2]	8	t_{CYC}[3]
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[4]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[4]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[4]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}[3]
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[5]	—	t_{CYC}[3]
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	$\overline{\text{RDY}}$ Valid to MCKO[6]	—	—	—	—

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

3 See Notes on t_{cyc} in Table 28 in Section 4.11.1 Clocking.

4 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

5 Lower frequency is required to be fully compliant to standard.

6 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

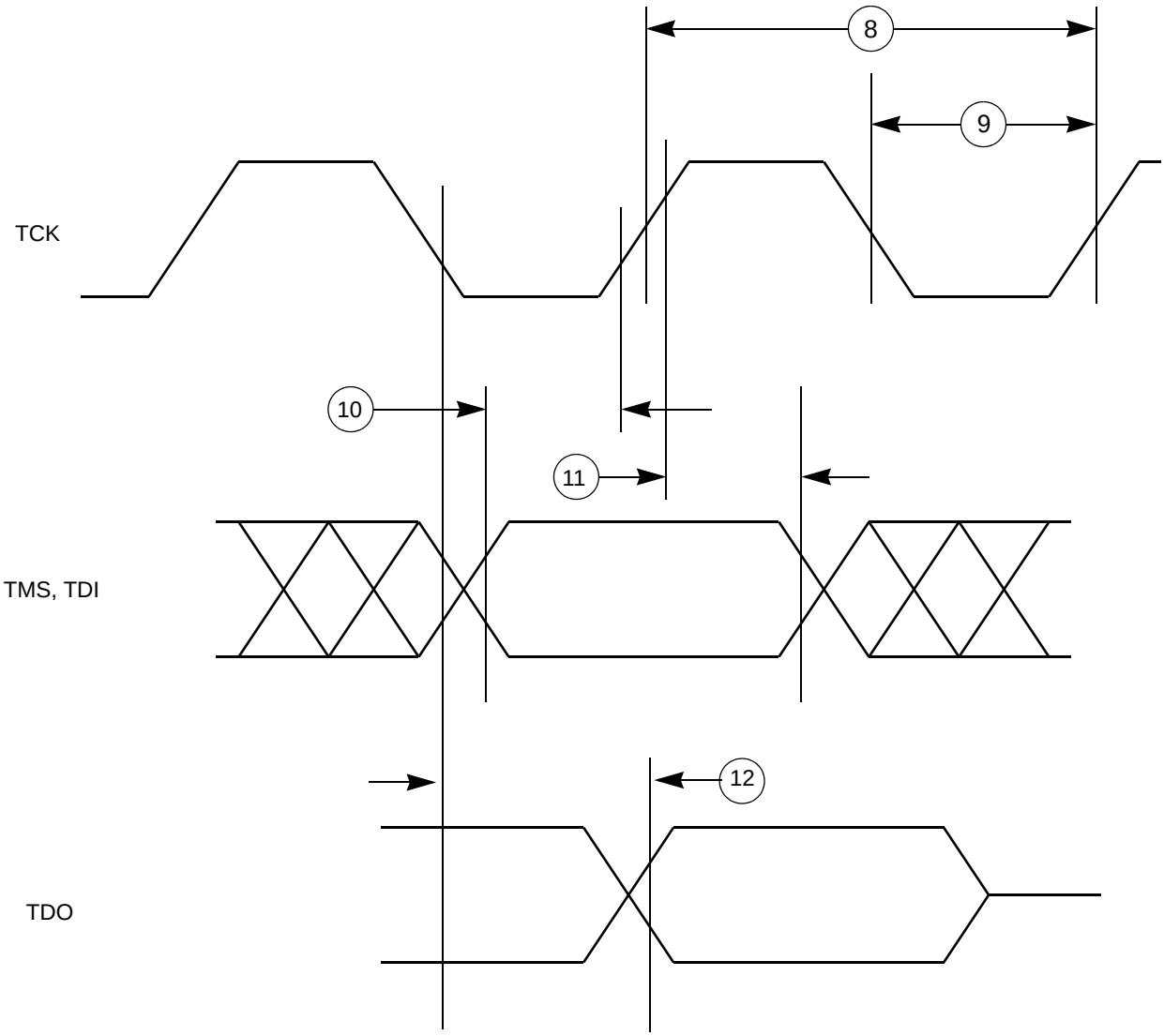


Figure 26. Nexus TCK, TDI, TMS, TDO Timing

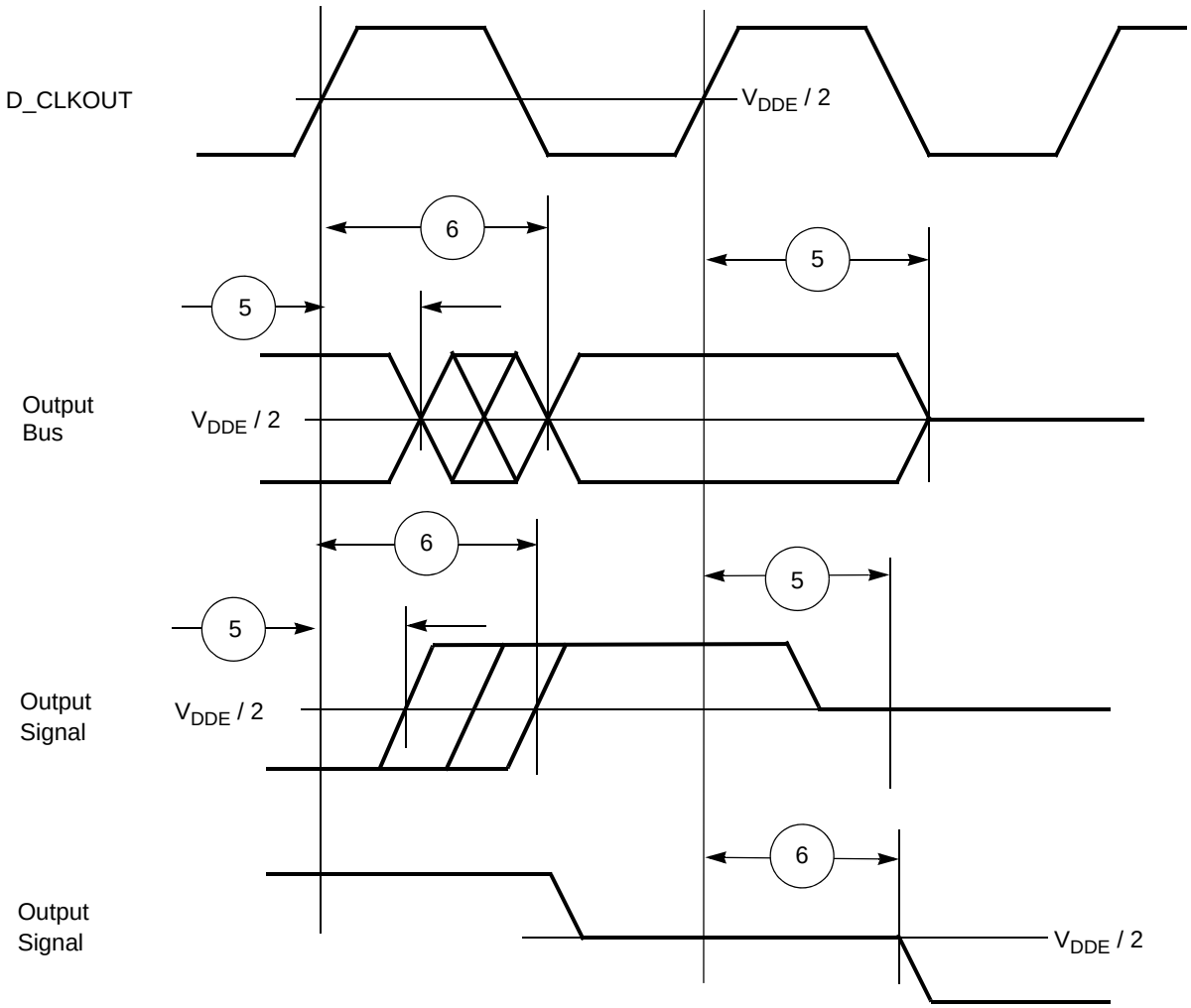


Figure 28. Synchronous Output Timing

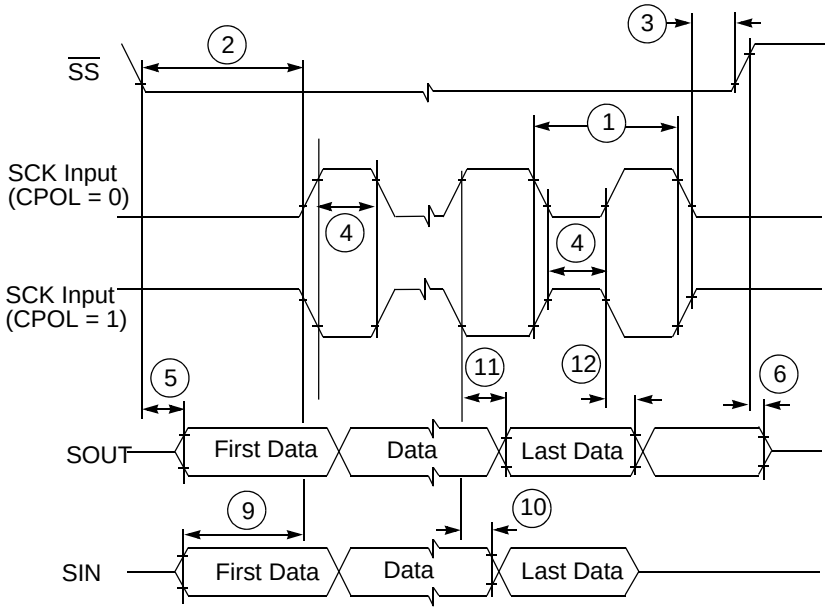


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

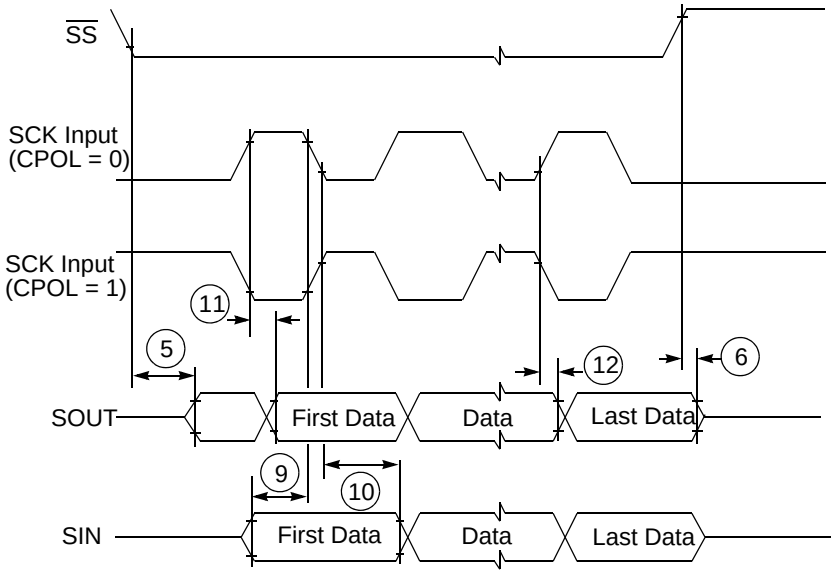


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

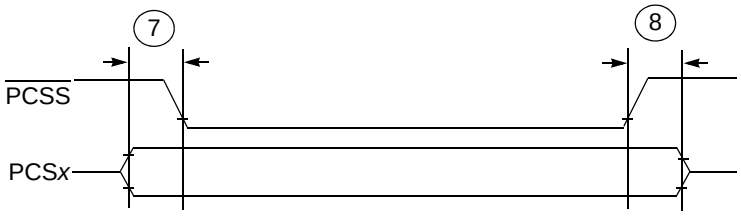


Figure 42. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

5 Package Information

The latest package outline drawings are available on the product summary pages on our website: http://www.freescale.com/powerarchitecture. The following table lists the package case number. Use these numbers in the webpage's keyword search engine to find the latest package outline drawings.

Table 42. Package Information

Package Type	Case Outline Number
324 TEPBGA	98ASS23840W
416 TEPBGA	98ARE10523D
516 TEPBGA	98ARS10503D

5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in Figure 43 and Figure 44.

Figure 43. 324 TEPBGA Package (1 of 2)

Table 43. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
eTPU_A												
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	K1	L1	K4
		A1	IRQ7	External interrupt request	I							
		A2	—	—	—							
		G	GPIO113	GPIO	I/O							
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO114	GPIO	I/O							
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO115	GPIO	I/O							
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO116	GPIO	I/O							
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO117	GPIO	I/O							
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO118	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO125	GPIO	I/O							
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO126	GPIO	I/O							
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO127	GPIO	I/O							
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO128	GPIO	I/O							
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO129	GPIO	I/O							
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO130	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
155	ETPUB8_ETPUB24_ GPIO155	P	ETPUB8	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N21	P24	T24
		A1	ETPUB24	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO155	GPIO	I/O							
156	ETPUB9_ETPUB25_ GPIO156	P	ETPUB9	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M22	P25	R22
		A1	ETPUB25	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO156	GPIO	I/O							
157	ETPUB10_ETPUB26_ GPIO157	P	ETPUB10	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M20	P26	T25
		A1	ETPUB26	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO157	GPIO	I/O							
158	ETPUB11_ETPUB27_ GPIO158	P	ETPUB11	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M21	N24	T26
		A1	ETPUB27	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO158	GPIO	I/O							
159	ETPUB12_ETPUB28_ GPIO159	P	ETPUB12	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L19	N25	R23
		A1	ETPUB28	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO159	GPIO	I/O							
160	ETPUB13_ETPUB29_ GPIO160	P	ETPUB13	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L20	N26	P22
		A1	ETPUB29	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO160	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA10	AE11	AE13
		A1	ETPUA3	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO182	GPIO	I/O							
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB10	AF11	AF13
		A1	ETPUA4	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO183	GPIO	I/O							
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y11	AD12	AF14
		A1	ETPUA5	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO184	GPIO	I/O							
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	—	AE12	AE14
		A1	ETPUA6	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO185	GPIO	I/O							
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB11	AF12	AD14
		A1	ETPUA7	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO186	GPIO	I/O							
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W10	AC13	AC14
		A1	ETPUA8	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO187	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27	AN27	—	B13	B13
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28	AN28	—	A13	A13
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29	AN29	—	B14	A14
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30	AN30	—	C14	B14
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31	AN31	—	D14	C14
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32	AN32	—	A14	B15
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33	AN33	—	B15	D14
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34	AN34	—	C15	C15
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35	AN35	—	D15	D15
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36	AN36	—	A15	A15
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37	AN37	—	C16	C17
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38	AN38	—	C17	D16
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39	AN39	—	D16	C16
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0	ANB0	B15	C18	C18
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1	ANB1	B16	D17	D17
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2	ANB2	A17	D18	D18
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3	ANB3	A18	D19	D19
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4	ANB4	B17	C19	B19
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5	ANB5	B18	C20	A20
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6	ANB6	A19	B19	C20
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7	ANB7	A20	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	ANB8	D13	B20	B20

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up	—/Up	—	N1	L5
		A1	PCSD5	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO92	GPIO	I/O							
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	—	AF23	AF23
		A1	ETRIG0	eQADC trigger input	I							
		A2	—	—	—							
		G	GPIO244	GPIO	I/O							
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up	—/Up	—	AD22	AD22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO245	GPIO	I/O							
DSPI												
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y7	AD8	AB8
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO93	GPIO	I/O							
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up	—/Up	AA7	AF7	AE7
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO94	GPIO	I/O							
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up	—/Up	AB7	AD7	AC7
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO95	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
238	PCSC0_SOUT_C_LVDSM_ GPIO238	P	PCSC0	DSPI C peripheral chip select	I/O	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AB19	AE21	AE21
		A1	SOUT_C_LVDSM	LVDS– downstream signal negative output data	O							
		A2	—	—	—							
		G	GPIO238	GPIO	I/O							
239	PCSC1_ GPIO239	P	PCSC1	DSPI C peripheral chip select	O	MH	V_{DDEH4}	—/Up	—/Up	—	AC22	AC22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO239	GPIO	I/O							
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AE23	AE23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO240	GPIO	I/O							
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AD23	AD23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO241	GPIO	I/O							
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AF24	AF24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO242	GPIO	I/O							
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AE24	AE24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO243	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO305	GPIO	I/O							
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO306	GPIO	I/O							
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO307	GPIO	I/O							
Reset and Clocks												
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	RESET/Up	M2	R2	N5
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	RSTOUT/ High	A3	A3	A3
211	BOOTCFG0_IRQ2_ GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	BOOTCFG/ Down	—	—	L4
		A1	IRQ2		I							
		A2	—	—	—							
		G	GPIO211	GPIO	I/O							
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	Input/Down	L1	N2	L3
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO212	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
231	MDO12_GPIO231	–[13]	MDO12[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V1	AA1	Y5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO231	GPIO	I/O							
232	MDO13_GPIO232	–[13]	MDO13[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W2	AA2	AA1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO232	GPIO	I/O							
233	MDO14_GPIO233	–[13]	MDO14[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V3	AA3	AA2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO233	GPIO	I/O							
234	MDO15_GPIO234	–[13]	MDO15[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U4	Y4	AA3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO234	GPIO	I/O							
224	$\overline{\text{MSEO0}}$	–[13]	MSEO0[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	P2	U2	U6
225	$\overline{\text{MSEO1}}$	–[13]	MSEO1[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	N3	T3	U5
226	RDY	–[13]	RDY	Nexus ready output	O	F	V_{DDE2}	O/Low	RDY/HI	M4	R4	U3
—	TCK	–[13]	TCK	JTAG test clock input	I	F	V_{DDE2}	TCK/Down	TCK/Down	Y1	AB2	AB2
—	TDI	–[13]	TDI	JTAG test data input	I	F	V_{DDE2}	TDI/Up	TDI/Up	Y2	AC2	AC2
228	TDO	–[13]	TDO	JTAG test data output	O	F	V_{DDE2}	TDO/Up	TDO/Up	W1	AB1	AB1
—	TMS	–[13]	TMS	JTAG test mode select input	I	F	V_{DDE2}	TMS/Up	TMS/Up	W3	AB3	AB3
—	JCOMP	–[13]	JCOMP	JTAG TAP controller enable	I	F	V_{DDE2}	JCOMP/Down	JCOMP/Down	M1	R1	U2
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down	TEST/Down	B4	B4	B4
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I	VDDE	V_{DDSYN}	VDDSYN	VDDSYN	Y22	AD26	AD26