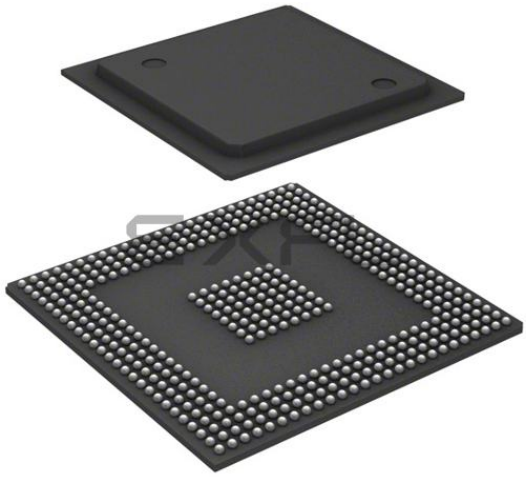

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674famvr3

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

1.2 MPC567xF Family Differences

Table 2 lists the differences between the MPC567xF devices. Refer to the *MPC5674F Reference Manual* for a full feature list and comparison.

Table 2. MPC567xF Family Differences

Feature	MPC5674F	MPC5674F	MPC5673F	MPC5673F
Package	416 BGA 516 BGA	324 BGA	416 BGA 516 BGA	324 BGA
Flash	4 MB	4 MB	3 MB	3 MB
SRAM	256 KB	256 KB	192 KB	192 KB
External bus	Yes (516 BGA only)	No	Yes (516 BGA only)	No
Serial	3	2	3	2
eSCI_A	Yes	Yes	Yes	Yes
eSCI_B	Yes	Yes	Yes	Yes
eSCI_C	Yes	No	Yes	No
SPI	4	3	4	3
DSPI_A	Yes	No	Yes	No
DSPI_B	Yes	Yes	Yes	Yes
DSPI_C	Yes	Yes	Yes	Yes
DSPI_D	Yes	Yes	Yes	Yes
eMIOS	32 channel	22 channel	32 channel	22 channel
eTPU2	64 channel	47 channel	64 channel	47 channel
eTPU_A	Yes (32 ch)	Yes (26 ch)	Yes	Yes (26 ch)
eTPU_B	Yes (32 ch)	Yes (21 ch, no TCRCLK)	Yes	Yes (21 ch, no TCRCLK)
ADC	64 channel	48 channel	64 channel	48 channel
eQADC_A	Yes (64 ch)[1]	Yes (24 ch)	Yes (64 ch)[1]	Yes (24 ch)
eQADC_B		Yes (24 ch)		Yes (24 ch)

1 There are are two pairs of 24 channels plus 16 shared channels. This gives 64 channels total: 40 per ADC (since 16 are shared).

Table 5. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	25	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	20	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
Junction to Board [5]	$R_{\theta JB}$	10	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. Thermal Characteristics, 324-pin Package[1]

MPC5674F Thermal Characteristic	Symbol	Value	Unit
Junction to ambient [2, 3], natural convection (one-layer board)	$R_{\theta JA}$	29	°C/W
Junction to ambient [1, 4], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	19	°C/W
Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	23	°C/W
Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	16	°C/W
Junction to board [5] (four-layer board 2s2p)	$R_{\theta JB}$	10	°C/W
Junction to case [6]	$R_{\theta JC}$	7	°C/W
Junction to package top [7], natural convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 12 and Table 13.

Table 12. Power Sequence Pin States for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 13. Power Sequence Pin States for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs Disabled
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs Disabled
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

1 The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

4.6.1 Power-Up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

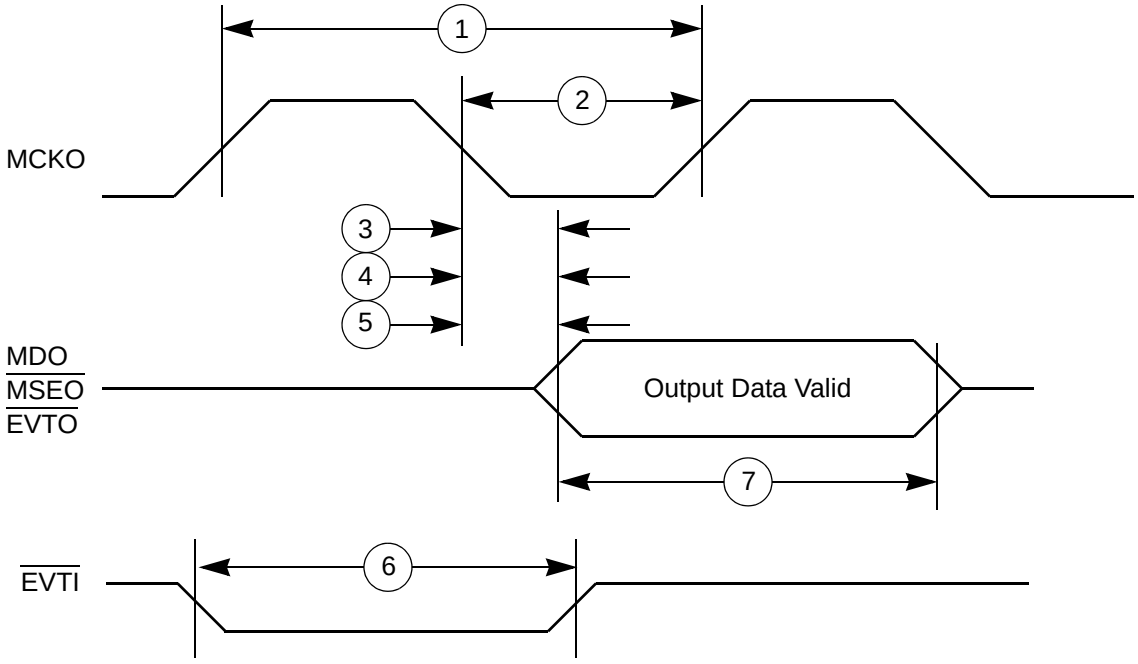

Figure 25. Nexus Timings

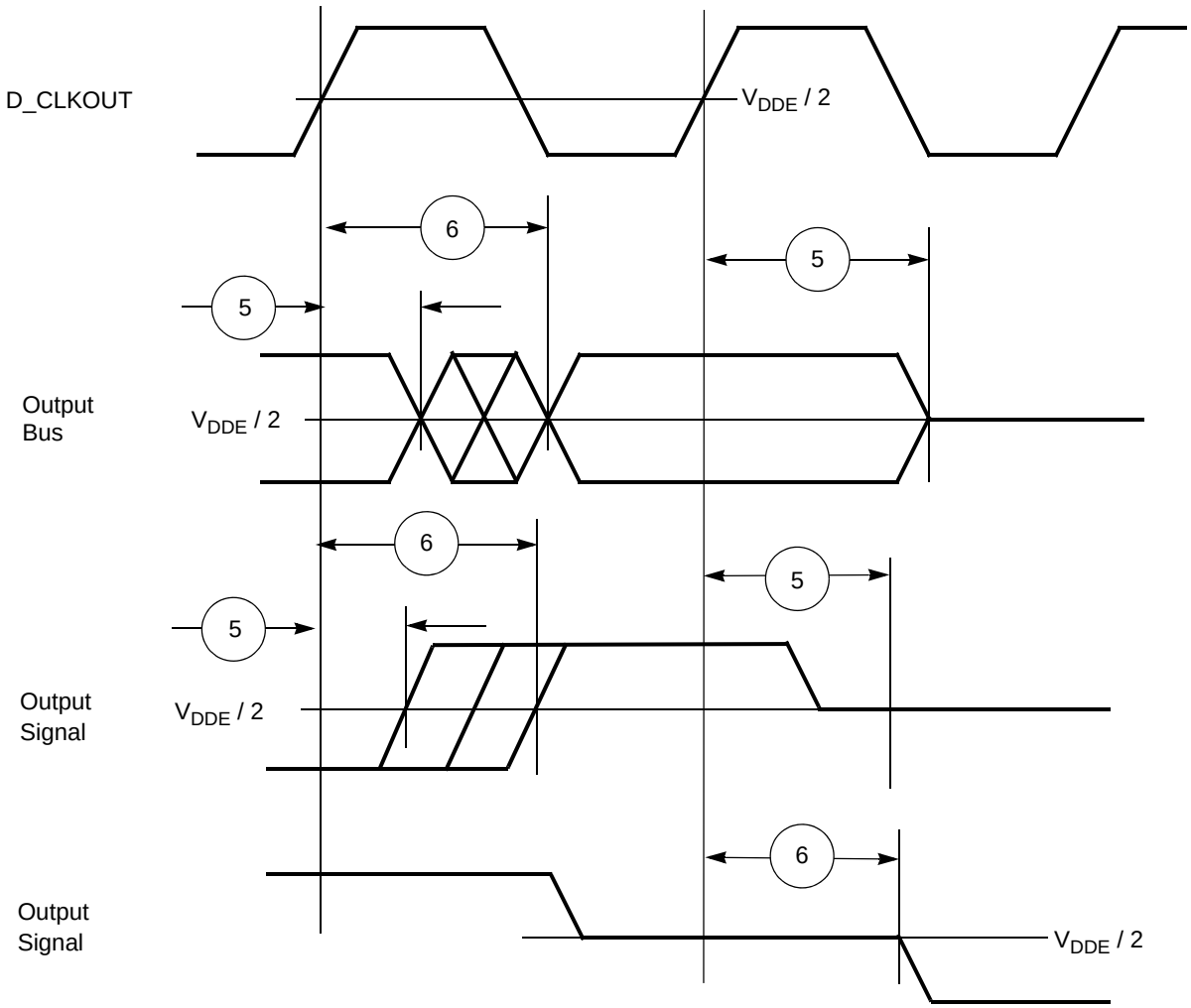

Figure 28. Synchronous Output Timing

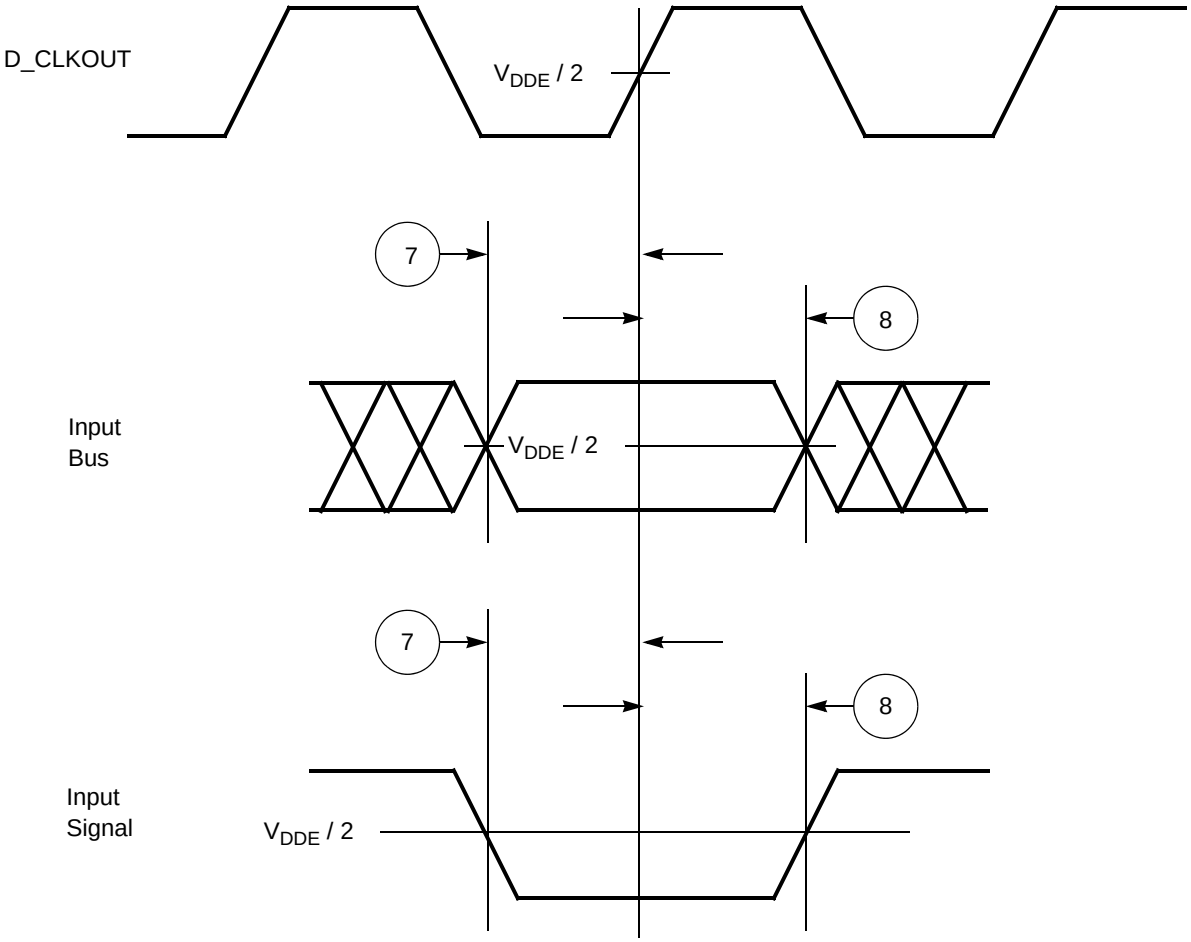

Figure 29. Synchronous Input Timing

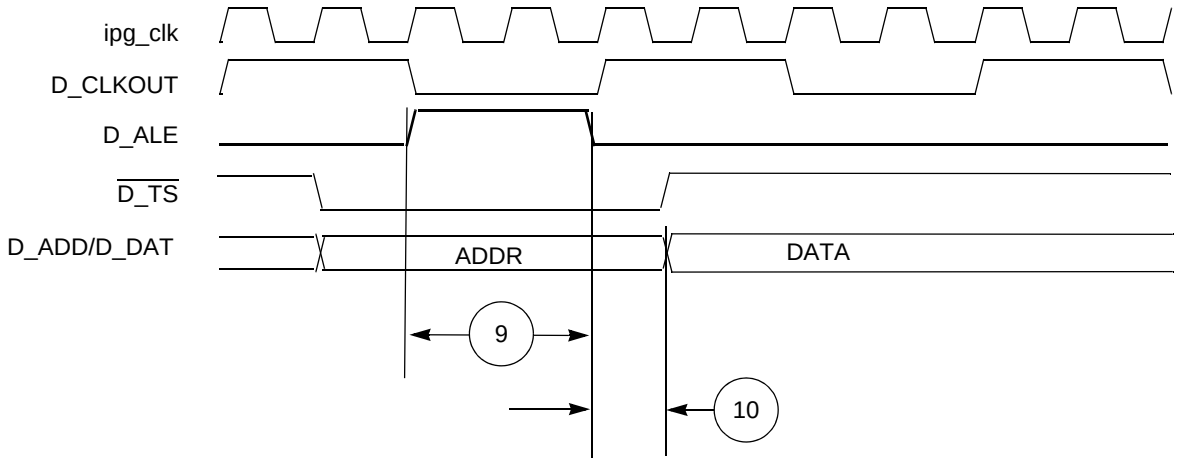

Figure 30. ALE Signal Timing

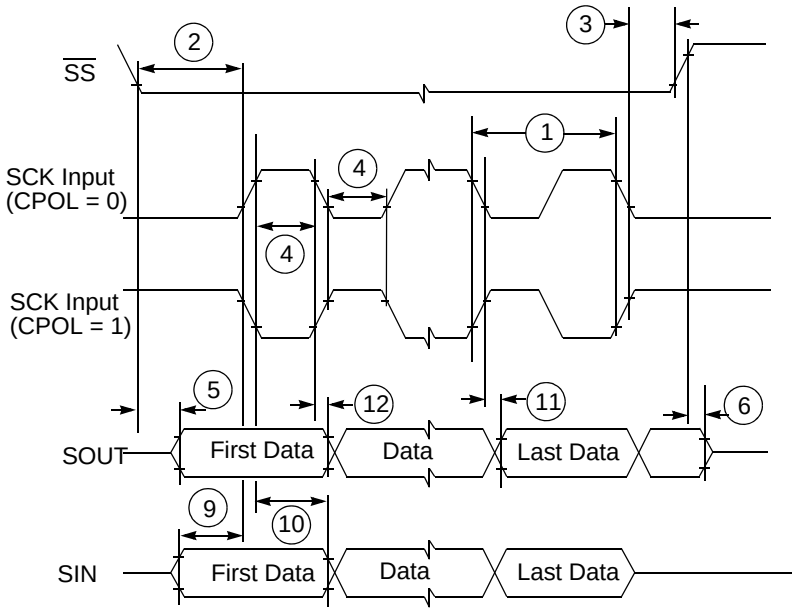

Figure 36. DSPI Classic SPI Timing — Slave, CPHA = 0

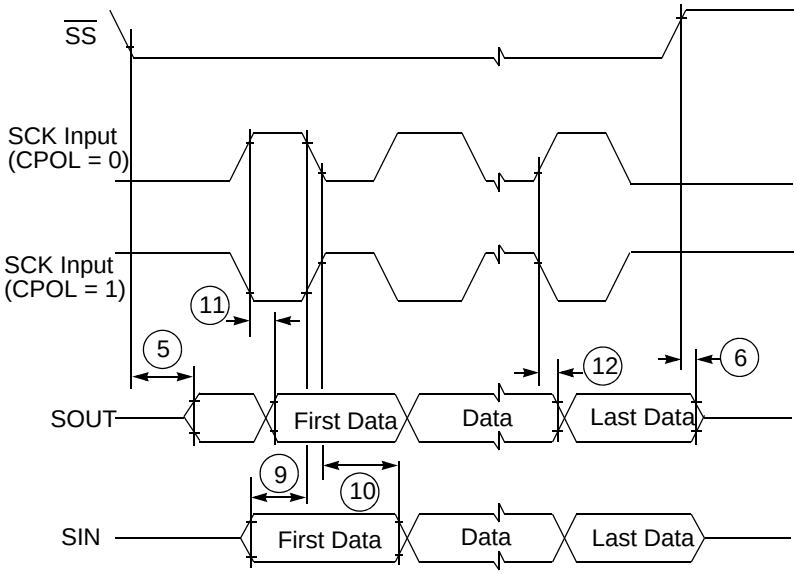

Figure 37. DSPI Classic SPI Timing — Slave, CPHA = 1

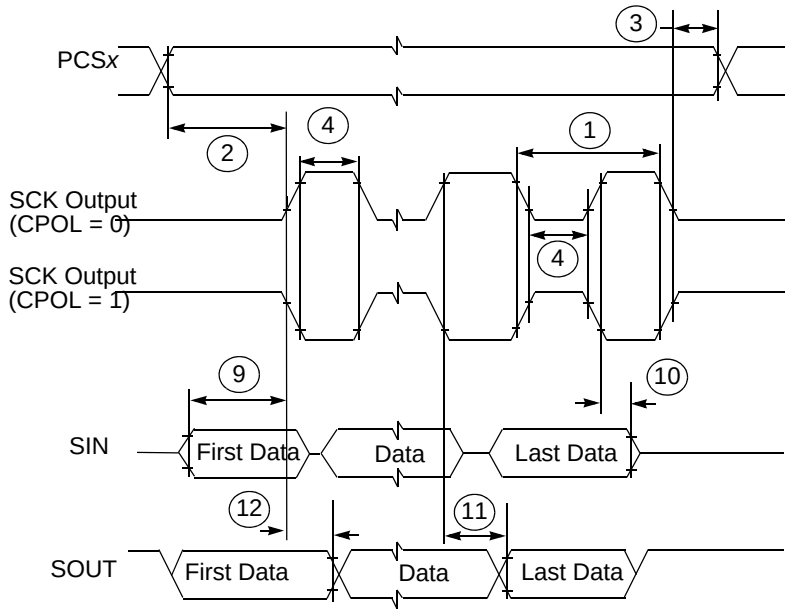

Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

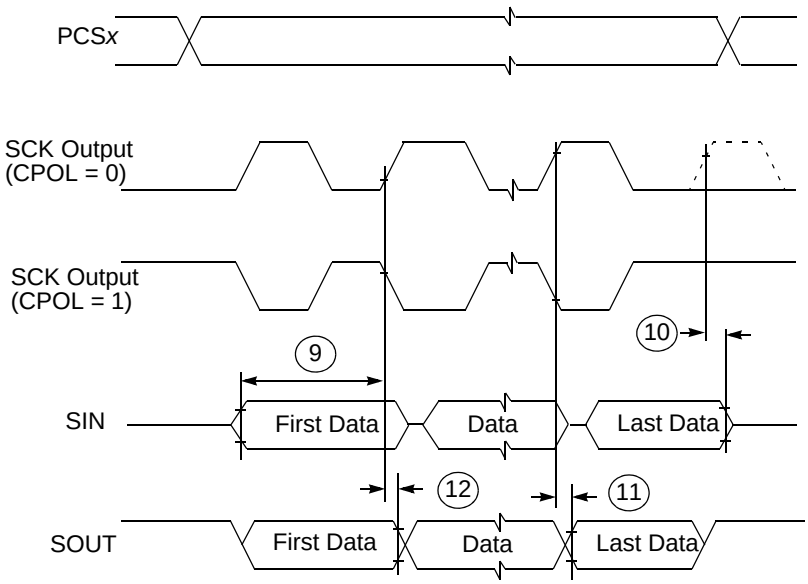

Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

5 Package Information

The latest package outline drawings are available on the product summary pages on our website: http://www.freescale.com/powerarchitecture. The following table lists the package case number. Use these numbers in the webpage's keyword search engine to find the latest package outline drawings.

Table 42. Package Information

Package Type	Case Outline Number
324 TEPBGA	98ASS23840W
416 TEPBGA	98ARE10523D
516 TEPBGA	98ARS10503D

Figure 46. 416 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
eTPU_A												
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	K1	L1	K4
		A1	IRQ7	External interrupt request	I							
		A2	—	—	—							
		G	GPIO113	GPIO	I/O							
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO114	GPIO	I/O							
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO115	GPIO	I/O							
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO116	GPIO	I/O							
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO117	GPIO	I/O							
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO118	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO125	GPIO	I/O							
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO126	GPIO	I/O							
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO127	GPIO	I/O							
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO128	GPIO	I/O							
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO129	GPIO	I/O							
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO130	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	E1	E1
		A1	IRQ11	External interrupt request	I							
		A2	—	—	—							
		G	GPIO137	GPIO	I/O							
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E2	E2
		A1	IRQ12	External interrupt request	I							
		A2	—	—	—							
		G	GPIO138	GPIO	I/O							
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	E3	E3
		A1	IRQ13	External interrupt request	I							
		A2	—	—	—							
		G	GPIO139	GPIO	I/O							
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	E4	E4
		A1	IRQ14	External interrupt request	I							
		A2	—	—	—							
		G	GPIO140	GPIO	I/O							
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	D1	D1
		A1	IRQ15	External interrupt request	I							
		A2	—	—	—							
		G	GPIO141	GPIO	I/O							
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO142	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
194	EMIOS15_IRQ1_ GPIO194	P	EMIOS15	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y13	AD14	AE16
		A1	IRQ1	External interrupt request	I							
		A2	CNRXD	FlexCAN D receive	I							
		G	GPIO194	GPIO	I/O							
195	EMIOS16_ETPUB0_ GPIO195	P	EMIOS16	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB14	AF15	AD16
		A1	ETPUB0	eTPU B channel	O							
		A2	FR_DBG[3]	FlexRay debug	O							
		G	GPIO195	GPIO	I/O							
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA13	AE15	AB15
		A1	ETPUB1	eTPU B channel	O							
		A2	FR_DBG[2]	FlexRay debug	O							
		G	GPIO196	GPIO	I/O							
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W12	AC15	AD17
		A1	ETPUB2	eTPU B channel	O							
		A2	FR_DBG[1]	FlexRay debug	O							
		G	GPIO197	GPIO	I/O							
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y14	AD15	AB16
		A1	ETPUB3	eTPU B channel	O							
		A2	FR_DBG[0]	FlexRay debug	O							
		G	GPIO198	GPIO	I/O							
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB15	AF16	AF16
		A1	ETPUB4	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO199	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
EBI												
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	—/Up	—	—	AD9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO256	GPIO	I/O							
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	—/Up	—	—	U1
		A1	D_ADD_DAT31	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO257	GPIO	I/O							
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	—/Up	—	—	T6
		A1	D_TEA	EBI transfer error acknowledge	I							
		A2	—	—	—							
		G	GPIO258	GPIO	I/O							
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO259	GPIO	I/O							
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO260	GPIO	I/O							
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO261	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
262	D_ADD15_ GPIO262	P	D_ADD15	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO262	GPIO	I/O							
263	D_ADD16_D_ADD_DAT16_ GPIO263	P	D_ADD16	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R5
		A1	D_ADD_DAT16	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO263	GPIO	I/O							
264	D_ADD17_D_ADD_DAT17_ GPIO264	P	D_ADD17	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T5
		A1	D_ADD_DAT17	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO264	GPIO	I/O							
265	D_ADD18_D_ADD_DAT18_ GPIO265	P	D_ADD18	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T2
		A1	D_ADD_DAT18	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO265	GPIO	I/O							
266	D_ADD19_D_ADD_DAT19_ GPIO266	P	D_ADD19	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T3
		A1	D_ADD_DAT19	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO266	GPIO	I/O							
267	D_ADD20_D_ADD_DAT20_ GPIO267	P	D_ADD20	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	T4
		A1	D_ADD_DAT20	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO267	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	VSSSYN	U22	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	VSTBY	K4	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	REGSEL	V20	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	REGCTL	T22	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	VSSFL	V21	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	VDDREG	U21	AA25	AA25

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO . This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

9 This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU_C.

10 During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

11 NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.

[12] Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FPM trace is enabled. MSEO and MCKO are also dependent on trace (RPM or FPM) being enabled.

[13] The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of these pins once enabled.

[14] MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).

[15] Do not connect pin directly to a power supply or ground.

Table 45 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 44. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13	J14	J9
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13	M14	N11
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3							

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