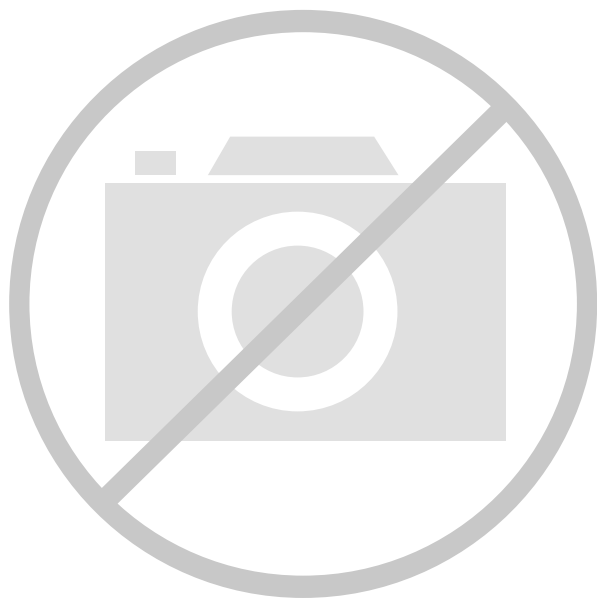




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Details

Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5674famvr3r

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3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VDD	RSTOUT	ANA0	ANA1	ANA4	ANA5	ANA15	VDDA_A0	VRH_A	VRL_A	REF-BYPCB1	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA2	ANA3	ANA6	ANA7	VDDA_A0	VSSA_A1	REF-BYPCA	REF-BYPCB	VDDA_B1	VSSA_B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ETPUA21	ETPUA26	VSS	VDD	ANA8	ANA10	ANA9	ANA13	ANA17	ANA19	ANA21	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ETPUA23	ETPUA25	ETPUA31	VSS	VDD	ANA11	ANA12	ANA14	ANA16	ANA18	ANA20	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
E	ETPUA20	ETPUA22	ETPUA24	ETPUA30															ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
F	ETPUA13	ETPUA14	ETPUA15	ETPUA27															ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
G	ETPUA10	ETPUA11	ETPUA12	ETPUA17															ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
H	ETPUA5	ETPUA6	ETPUA9	ETPUA16															VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA3	ETPUA4					VSS	VSS	VSS	VSS	VSS	VSS					ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	TCRCLKA	ETPUA0	VDD	VSTBY					VSS	VSS	VSS	VSS	VSS	VSS					ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	BOOT-CFG1	PLLCFG1	PLLCFG2	VDDEH1					VSS	VSS	VSS	VSS	VSS	VSS					ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	JCOMP	RESET	PLLCFG0	RDY					VDDE2	VSS	VSS	VSS	VSS	VSS					ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VDDE2	MCKO	MSE01	EVTI					VDDE2	VDDE2	VSS	VSS	VSS	VSS					ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	EVT0	MSE00	MDO0	MDO1					VDDE2	VDDE2	VSS	VSS	VSS	VSS					TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
R	MDO2	MDO3	MDO4	MDO5															ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
T	MDO6	MDO7	MDO8	VDDE2															ETPUB19	ETPUB18	VDDEH6	REGCTL	T
U	MDO9	MDO10	MDO11	MDO15															ETPUB31	ETPUB30	VDDREG	VSSSYN	U
V	MDO12	VDDE2	MDO14	VDD33_2															VDD	REGSEL	VSSFL	EXTAL	V
W	TDO	MDO13	TMS	VSS	VDD	VDDE2	PCSB2	VDDEH4	VDD	EMIOS8	EMIOS9	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	TCK	TDI	VSS	VDD	FR_A_TX	FR_B_TX	SCKA	SCKB	PCSB0	EMIOS2	EMIOS5	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	ENGCLK	VSS	VDD	FR_A_RX	FR_B_RX	PCSA5	SINA	SINB	EMIOS0	EMIOS3	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	VSS	VDD	FR_A_TX_EN	VDDE2	FR_B_TX_EN	PCSA0	SOUTA	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

Pin Assignments

	12	13	14	15	16	17	18	19	20	21	22	
A	REF-BYPCB1	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB2	ANB3	ANB6	ANB7	ANB22	VSS	A
B	REF-BYPCB	VDDA_B1	VSSA_B0	ANB0	ANB1	ANB4	ANB5	ANB19	ANB23	VSS	TCRCLKC	B
C	ANA23	ANB10	ANB9	ANB11	ANB12	ANB14	ANB16	ANB20	VSS	ETPUC0	VDDEH7	C
D	ANA22	ANB8	ANB13	ANB15	ANB17	ANB18	ANB21	VSS	ETPUC1	ETPUC3	ETPUC2	D
								ETPUC5	ETPUC10	ETPUC11	ETPUC4	E
								ETPUC12	ETPUC14	ETPUC13	ETPUC9	F
								ETPUC20	ETPUC18	ETPUC19	ETPUC17	G
								VDDEH7	ETPUC23	ETPUC22	ETPUC21	H
J	VSS	VSS	VSS					ETPUC27	ETPUC28	ETPUC26	ETPUC24	J
K	VSS	VSS	VSS					ETPUC31	ETPUC30	ETPUC29	ETPUC25	K
L	VSS	VSS	VSS					ETPUB12	ETPUB13	ETPUB14	VDDEH7	L
M	VSS	VSS	VSS					ETPUB7	ETPUB10	ETPUB11	ETPUB9	M
N	VSS	VSS	VSS					ETPUB0	VDDEH6	ETPUB8	ETPUB6	N
P	VSS	VSS	VSS					TCRCLKB	ETPUB16	ETPUB5	ETPUB4	P
								ETPUB1	ETPUB17	ETPUB3	ETPUB2	R
								ETPUB19	ETPUB18	VDDEH6	REGCTL	T
								ETPUB31	ETPUB30	VDDREG	VSSSYN	U
								VDD	REGSEL	VSSFL	EXTAL	V
W	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNTXC	CNRXC	CNRXB	VSS	VDD	VDD33_3	XTAL	W
Y	EMIOS14	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNRXD	VSS	VDD	VDDSYN	Y
AA	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS28	EMIOS29	CNRXA	SCKC	SINC	VSS	VDD	AA
AB	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	CNTXA	SOUTC	PCSC0	VDDEH4	CNTXD	VSS	AB
	12	13	14	15	16	17	18	19	20	21	22	

MPC5674F 324 TEPBGA
(as viewed from top through the package)

Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)

3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

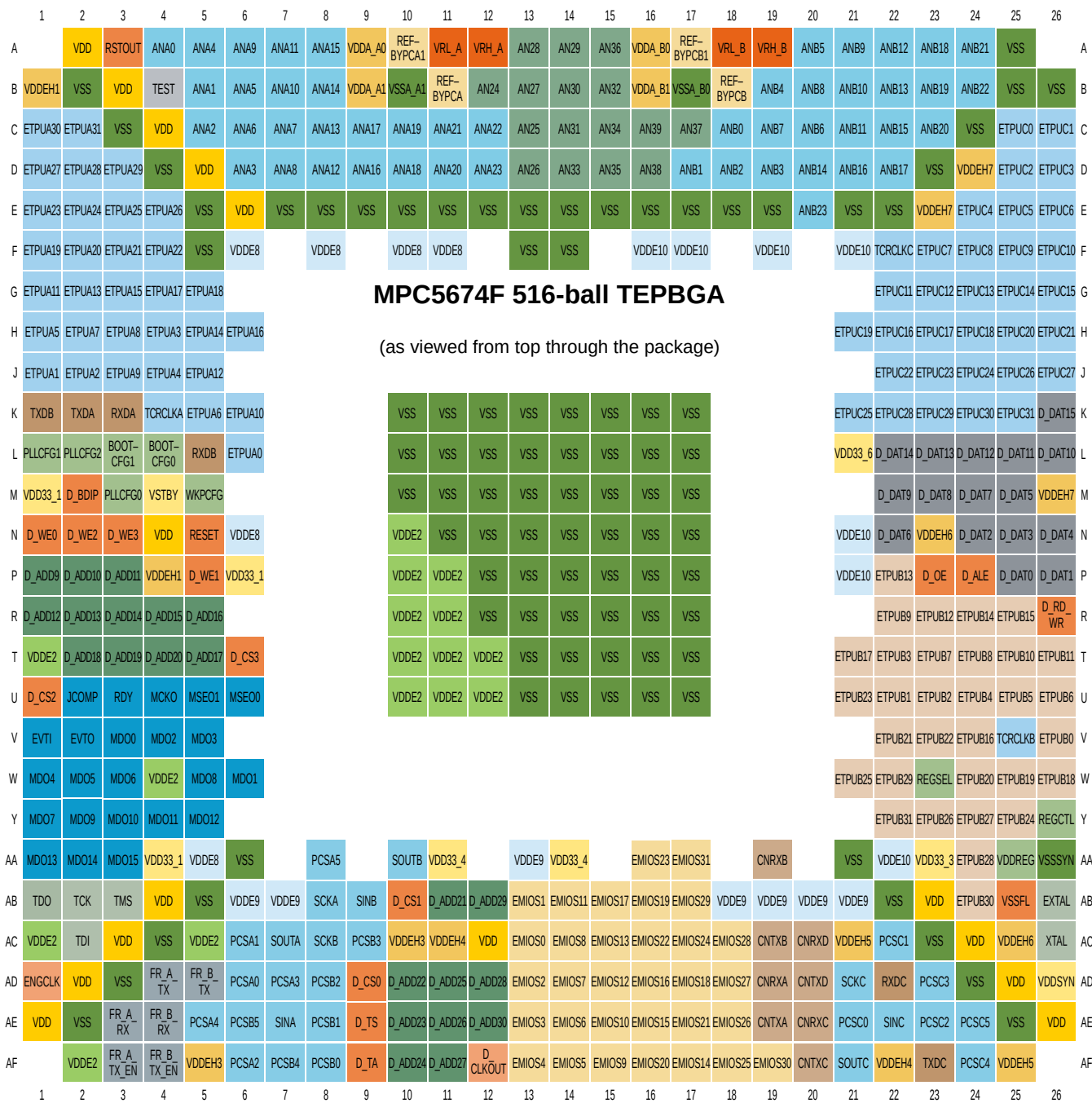


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A		VDD	RSTOUT	ANA0	ANA4	ANA9	ANA11	ANA15	VDDA_A0	REF-BYPCA1	VRL_A	VRH_A	AN28	A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REFBYPCA	AN24	AN27	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA7	ANA13	ANA17	ANA19	ANA21	ANA22	AN25	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA8	ANA12	ANA16	ANA18	ANA20	ANA23	AN26	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18									G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16								H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12									J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	L
M	VDD33_1	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

MPC5674F 516-ball TEPBGA
(as viewed from top through the package)
(1 of 4)

Figure 12. MPC5674F 516-ball TEPBGA (1 of 4)

Pin Assignments

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN29	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	AN30	AN32	VDDA_B1	VSSA_B0	REFBYPCB	ANB4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	AN31	AN34	AN39	AN37	ANB0	ANB7	ANB6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	AN33	AN35	AN38	ANB1	ANB2	ANB3	ANB14	ANB16	ANB17	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	MPC5674F 516-ball TEPBGA (as viewed from top through the package) (2 of 4)								ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H								ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J									ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K								ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	VSS	VSS	VSS	VSS				VDD33_6	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings¹

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	-0.3	2.0 ²	V
2	SRAM Standby Voltage	V_{STBY}	-0.3	6.4 ^{3,4}	V
3	Clock Synthesizer Voltage	V_{DDSYN}	-0.3	5.3 ^{4,5}	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	-0.3	5.3 ^{4,5}	V
5	Analog Supply Voltage (reference to V_{SSA} ⁶)	V_{DDA} ⁷	-0.3	6.4 ^{3,4}	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	-0.3	5.3 ^{4,5}	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	-0.3	6.4 ^{3,4}	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	-0.3	6.4 ^{3,4}	V
9	Analog Reference High Voltage (reference to V_{RL} ⁸)	V_{RH} ⁹	-0.3	6.4 ^{3,4}	V
10	V_{SS} to V_{SSA} ⁸ Differential Voltage	$V_{SS} - V_{SSA}$	-0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	-0.3	6.4 ^{3,4}	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	-0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} - V_{DDSYN}$	-0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	-0.1	0.1	V
15	Maximum Digital Input Current ¹⁰ (per pin, applies to all digital pins)	I_{MAXD}	-3 ¹¹	3 ¹¹	mA
16	Maximum Analog Input Current ¹² (per pin, applies to all analog pins)	I_{MAXA}	-3 ⁷	3 ^{7,11}	mA
17	Maximum Operating Temperature Range ¹³ – Die Junction Temperature	T_J	-40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	-55.0	150.0	°C
19	Maximum Solder Temperature ¹⁴ Pb-free package SnPb package	T_{sdr}	— —	260.0 245.0	°C
20	Moisture Sensitivity Level ¹⁵	MSL	—	3	—

- ⁶ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- ⁷ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \text{Eqn. 1}$$

where:

T_A = ambient temperature for the package ($^{\circ}\text{C}$)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} * P_D) \quad \text{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package ($^{\circ}\text{C}$)

Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
4c	—	LVD 1.2V Hysteresis	15	20	25	mV
4d	V _{LVDSTEP12}	Trimming step LVD 1.2V	—	10	—	mV
5	I _{REGCTL}	VRC DC current output on REGCTL	—	—	20	mA
6	—	Voltage regulator 1.2V current consumption VDDREG	—	3	—	mA
7	V _{DD33OUT}	Nominal V _{REG} 3.3V output	—	3.3	—	V
7a	—	Untrimmed V _{REG} 3.3V output variation before band gap trim (unloaded) Note: Rising VDDSYN	V _{DD33OUT} – 6%	V _{DD33OUT}	V _{DD33OUT} + 10%	V
7b	—	Trimmed V _{REG} 3.3V output variation after band gap trim (max. load 80mA)	V _{DD33OUT} – 5%	V _{DD33OUT}	V _{DD33OUT} + 10%	V
7c	V _{STEPV33}	Trimming step VDDSYN	—	30	—	mV
8	V _{LVD33}	Nominal rising LVD 3.3V Note: ~V _{DD33OUT} × 0.872	—	2.950	—	V
8a	—	Untrimmed LVD 3.3V variation before band gap trim Note: Rising VDDSYN	V _{LVD33} – 5%	V _{LVD33}	V _{LVD33} + 5%	V
8b	—	Trimmed LVD 3.3V variation after bad gap trim Note: Rising VDDSYN	V _{LVD33} – 3%	V _{LVD33}	V _{LVD33} + 3%	V
8c	—	LVD 3.3V Hysteresis	—	30	—	mV
8d	V _{LVDSTEP33}	Trimming step LVD 3.3V	—	30	—	mV
9	I _{DD33}	V _{REG} = 4.5 V, max DC output current V _{REG} = 4.25 V, max DC output current, crank condition Note: Max current supplied by VDDSYN that does not cause it to drop below V _{LVD33}	— —	— —	80 40	mA mA
10	—	Voltage regulator 3.3V current consumption VDDREG Note: Except I _{DD33}	—	2	—	mA
11	V _{PORREG}	POR rising on VDDREG	—	2.00	—	V
11a	—	POR VDDREG variation	V _{PORREG} – 30%	V _{PORREG}	V _{PORREG} + 30%	V
11b	—	POR VDDREG hysteresis	—	250	—	mV
12	V _{LVDREG}	Nominal rising LVD VDDREG (LDO3V / LDO5V mode)	—	2.950	—	V
12a	—	Untrimmed LVD VDDREG variation before band gap trim Note: Rising VDDREG	V _{LVDREG} – 5%	V _{LVDREG}	V _{LVDREG} + 5%	V
12b	—	Trimmed LVD VDDREG variation after band gap trim Note: Rising VDDREG	V _{LVDREG} – 3%	V _{LVDREG}	V _{LVDREG} + 3%	V

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ± 1.0 °C 100 °C to 150 °C ± 1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$ ¹	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	± 10.0	—	°C

¹ Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ ¹	Initial Max ²	Max ³	Unit
1	Double Word (64 bits) Program Time ⁴	$t_{dwprogram}$	—	38	—	500	μs
2	Page Program Time ^{4,5}	$t_{pprogram}$	—	45	160	500	μs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

¹ Typical program and erase times assume nominal supply values and operation at 25 °C.

² Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

³ The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

⁴ Program times are actual hardware programming times and do not include software overhead.

⁵ Page size is 128 bits (4 words).

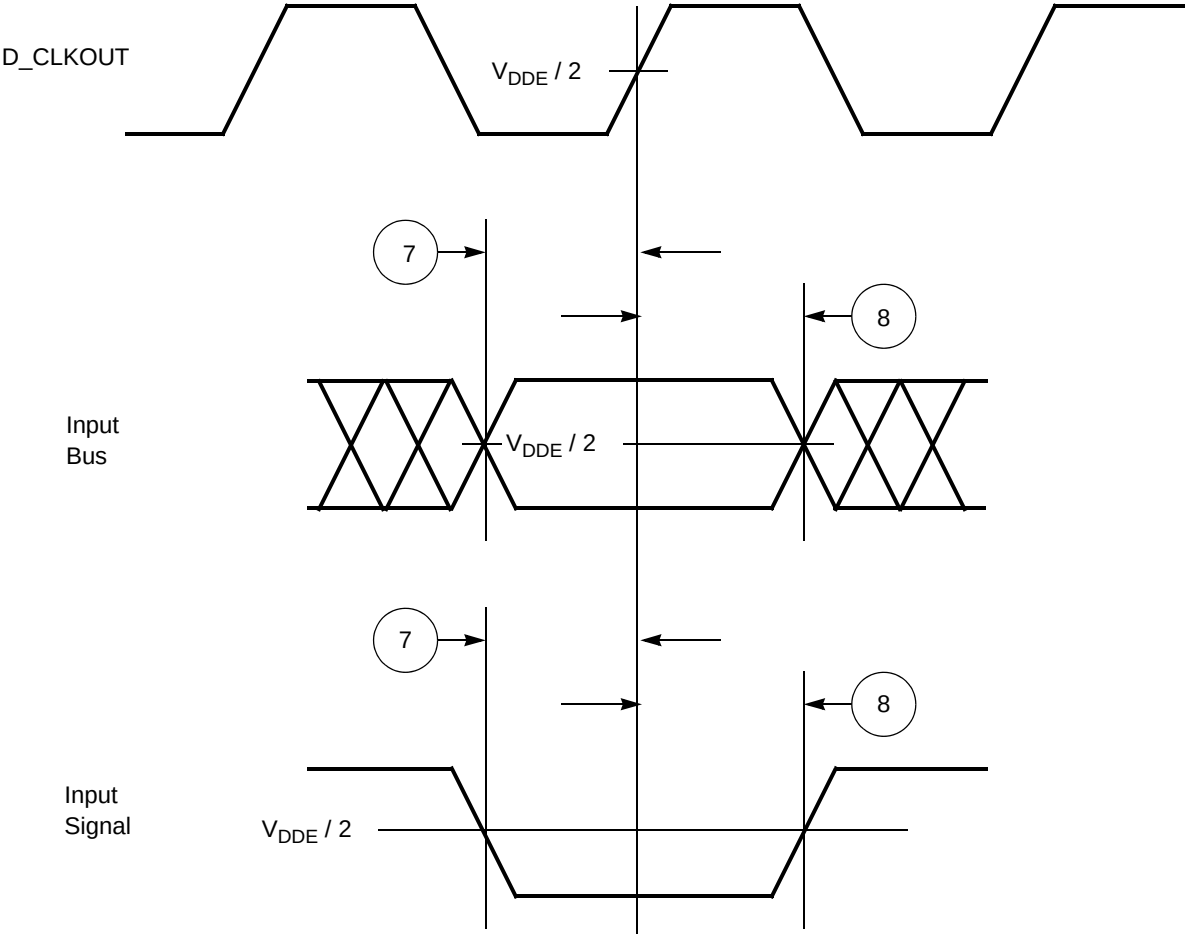


Figure 29. Synchronous Input Timing

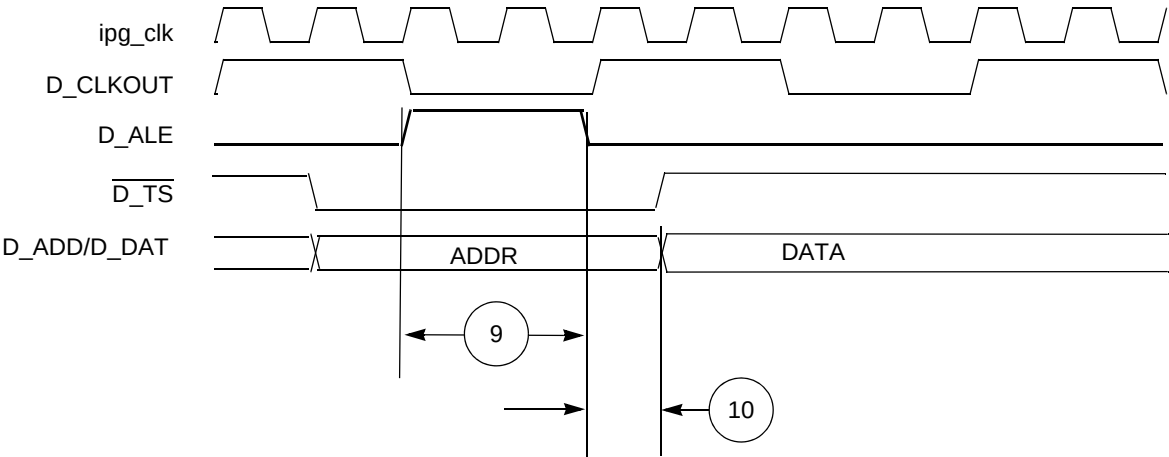


Figure 30. ALE Signal Timing

5 Package Information

The latest package outline drawings are available on the product summary pages on our website: <http://www.freescale.com/powerarchitecture>. The following table lists the package case number. Use these numbers in the webpage’s keyword search engine to find the latest package outline drawings.

Table 42. Package Information

Package Type	Case Outline Number
324 TEPBGA	98ASS23840W
416 TEPBGA	98ARE10523D
516 TEPBGA	98ARS10503D

5.2 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 45 and Figure 46.

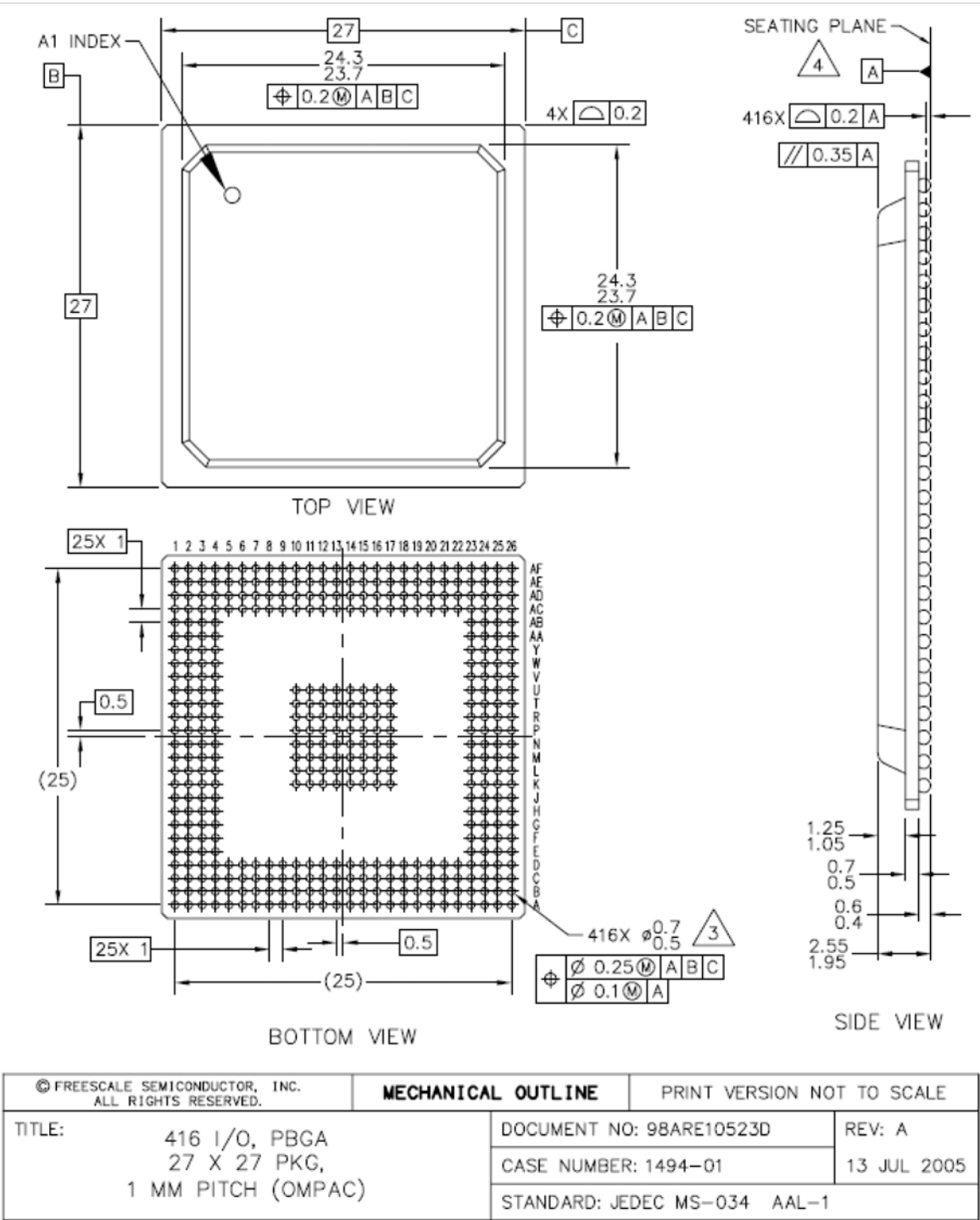


Figure 45. 416 TEPBGA Package (1 of 2)

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. PACKAGE CODES: 5193 & 5198.

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TITLE: 516 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARS10503D		REV: B
	CASE NUMBER: 1164A-01		09 AUG 2005
	STANDARD: JEDEC MS-034 AAL-1		

Figure 48. 516 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO131	GPIO	I/O							
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO132	GPIO	I/O							
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	—	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO133	GPIO	I/O							
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	E1	F2	F2
		A1	IRQ8	External interrupt request	I							
		A2	—	—	—							
		G	GPIO134	GPIO	I/O							
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	C1	F3	F3
		A1	IRQ9	External interrupt request	I							
		A2	—	—	—							
		G	GPIO135	GPIO	I/O							
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V _{DDEH1}	—/WKPCFG	—/WKPCFG	E2	F4	F4
		A1	IRQ10	External interrupt request	I							
		A2	—	—	—							
		G	GPIO136	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
188	EMIOS9_ETPUA9_GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	W11	AD13	AF15
		A1	ETPUA9	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO188	GPIO	I/O							
189	EMIOS10_SCKD_GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AA11	AE13	AE15
		A1	SCKD	DSPI D clock	O							
		A2	—	—	—							
		G	GPIO189	GPIO	I/O							
190	EMIOS11_SIND_GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AB12	AF13	AB14
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO190	GPIO	I/O							
191	EMIOS12_SOUTC_GPIO191	P	EMIOS12	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AB13	AF14	AD15
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO191	GPIO	I/O							
192	EMIOS13_SOUTD_GPIO192	P	EMIOS13	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	AA12	AE14	AC15
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO192	GPIO	I/O							
193	EMIOS14_IRQ0_GPIO193	P	EMIOS14	eMIOS channel	O	MH	V _{DDEH4}	—/WKPCFG	—/WKPCFG	Y12	AC14	AF17
		A1	IRQ0	External interrupt request	I							
		A2	CNTXD	FlexCAN D transmit	O							
		G	GPIO193	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V _{DDE2}	—/Up (—/— for Rev.1 of the device)	—/Up (—/— for Rev.1 of the device)	AB5	AF4	AF4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO253	GPIO	I/O							
FlexCAN												
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V _{DDEH4}	—/Up	—/Up	AB17	AF19	AE19
		A1	TXDA	eSCI A transmit	O							
		A2	—	—	—							
		G	GPIO83	GPIO	I/O							
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V _{DDEH4}	—/Up	—/Up	AA18	AE19	AD19
		A1	RXDA	eSCI A receive	I							
		A2	—	—	—							
		G	GPIO84	GPIO	I/O							
85	CNTXB_PCSC3_ GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V _{DDEH4}	—/Up	—/Up	Y18	AD19	AC19
		A1	PCSC3	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO85	GPIO	I/O							
86	CNRXB_PCSC4_ GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V _{DDEH4}	—/Up	—/Up	W18	AC19	AA19
		A1	PCSC4	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO86	GPIO	I/O							
87	CNTXC_PCSD3_ GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V _{DDEH4}	—/Up	—/Up	W16	AF20	AF20
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO87	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	M25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO283	GPIO	I/O							
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	N22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO284	GPIO	I/O							
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	M24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO285	GPIO	I/O							
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	M23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO286	GPIO	I/O							
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	M22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO287	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
77	MDO6_GPIO77 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO6 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	T1	W1	W3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO77	GPIO	I/O							
78	MDO7_GPIO78 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO7 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	T2	W2	Y1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO78	GPIO	I/O							
79	MDO8_GPIO79 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO8 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	T3	W3	W5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO79	GPIO	I/O							
80	MDO9_GPIO80 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO9 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	U1	Y1	Y2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO80	GPIO	I/O							
81	MDO10_GPIO81 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO10 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	U2	Y2	Y3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO81	GPIO	I/O							
82	MDO11_GPIO82 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO11 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	U3	Y3	Y4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO82	GPIO	I/O							

- ¹² Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FPM trace is enabled. MSEO and MCKO are also dependent on trace (RPM or FPM) being enabled.
- ¹³ The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of these pins once enabled.
- ¹⁴ MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).
- ¹⁵ Do not connect pin directly to a power supply or ground.