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Details

Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674famvy3r

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings¹

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	-0.3	2.0 ²	V
2	SRAM Standby Voltage	V_{STBY}	-0.3	6.4 ^{3,4}	V
3	Clock Synthesizer Voltage	V_{DDSYN}	-0.3	5.3 ^{4,5}	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	-0.3	5.3 ^{4,5}	V
5	Analog Supply Voltage (reference to V_{SSA} ⁶)	V_{DDA} ⁷	-0.3	6.4 ^{3,4}	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	-0.3	5.3 ^{4,5}	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	-0.3	6.4 ^{3,4}	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	-0.3	6.4 ^{3,4}	V
9	Analog Reference High Voltage (reference to V_{RL} ⁸)	V_{RH} ⁹	-0.3	6.4 ^{3,4}	V
10	V_{SS} to V_{SSA} ⁸ Differential Voltage	$V_{SS} - V_{SSA}$	-0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	-0.3	6.4 ^{3,4}	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	-0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} - V_{DDSYN}$	-0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	-0.1	0.1	V
15	Maximum Digital Input Current ¹⁰ (per pin, applies to all digital pins)	I_{MAXD}	-3 ¹¹	3 ¹¹	mA
16	Maximum Analog Input Current ¹² (per pin, applies to all analog pins)	I_{MAXA}	-3 ⁷	3 ^{7,11}	mA
17	Maximum Operating Temperature Range ¹³ – Die Junction Temperature	T_J	-40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	-55.0	150.0	°C
19	Maximum Solder Temperature ¹⁴ Pb-free package SnPb package	T_{sdr}	— —	260.0 245.0	°C
20	Moisture Sensitivity Level ¹⁵	MSL	—	3	—

⁴ “FM on” = FM depth of $\pm 2\%$

⁵ K = 30 dB μ V

Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA

Symbol	Description	Conditions	f_{osc} f_{sys}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	$V_{DD} = 1.2\text{ V}$ $V_{DDE} = 3.3\text{ V}$ $V_{DDEH} = 5\text{ V}$ $T_A = 25\text{ }^\circ\text{C}$ 516 BGA EBI on CLK on FM off	40 MHz crystal 264 MHz ($f_{EBI_CAL} = 66\text{ MHz}$)	0.15–50	40	dB μ V	¹
				50–150	48		
				150–500	48		
				500–1000	47		
				IEC and SAE level	G ²	—	^{1, 3}
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	$V_{DD} = 1.2\text{ V}$ $V_{DDE} = 3.3\text{ V}$ $V_{DDEH} = 5\text{ V}$ $T_A = 25\text{ }^\circ\text{C}$ 516 BGA EBI on CLK on FM on ⁴	40 MHz crystal 264 MHz ($f_{EBI_CAL} = 66\text{ MHz}$)	0.15–50	40	dB μ V	¹
				50–150	44		
				150–500	41		
				500–1000	36		
				IEC and SAE level	G ²	—	^{1, 3}

¹ Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

² G = 48 dB μ V

³ Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

⁴ “FM on” = FM depth of $\pm 2\%$

4.4 ESD Characteristics

Table 9. ESD Ratings^{1,2}

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Note: For ADC internal resource measurements, see Table 21 in Section 4.9.1, “ADC Internal Resource Measurements.”

Table 20. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Offset Error without Calibration	OFFNC	0 ⁴	100 ⁴	LSB
10	Offset Error with Calibration	OFFWC	-4 ⁴	4 ⁴	LSB
11	Full Scale Gain Error without Calibration	GAINNC	-120 ⁴	0 ⁴	LSB
12	Full Scale Gain Error with Calibration	GAINWC	-4 ^{4,6}	4 ^{4,6}	LSB
13	Non-Disruptive Input Injection Current ^{7, 8, 9, 10}	I _{INJ}	-3	3	mA
14	Incremental Error due to injection current ^{11, 12}	E _{INJ}	-4 ⁴	4 ⁴	Counts
15	TUE value at 8 MHz ^{13, 14} (with calibration)	TUE8	-4 ^{4,6}	4 ^{4,6}	Counts
16	TUE value at 16 MHz ^{13, 14} (with calibration)	TUE16	-8	8	Counts
17	Maximum differential voltage ¹⁵ (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	DIFF _{max} DIFF _{max2} DIFF _{max4}	— — —	(V _{RH} - V _{RL})/2 (V _{RH} - V _{RL})/4 (V _{RH} - V _{RL})/8	V V V
18	Differential input Common mode voltage ¹⁵ (DANx- + DANx+)/2	DIFF _{cmv}	(V _{RH} - V _{RL})/2 - 5%	(V _{RH} - V _{RL})/2 + 5%	V

¹ Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

² At V_{RH} - V_{RL} = 5.12 V, one count = 1.25 mV without using pregain.

³ INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} - 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

⁴ New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

⁵ At V_{RH} - V_{RL} = 5.12 V, one LSB = 1.25 mV.

⁶ The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

⁷ Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than V_{RH} and \$000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

⁸ Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

⁹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using V_{POSCLAMP} = V_{DDA} + 0.5 V and V_{NEGCLAMP} = -0.3 V, then use the larger of the calculated values.

¹⁰ Condition applies to two adjacent pins at injection limits.

¹¹ Performance expected with production silicon.

¹² All channels have same 10 kΩ < R_s < 100 kΩ Channel under test has R_s = 10 kΩ, I_{INJ} = I_{INJMAX} · I_{INJMIN}.

¹³ The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

¹⁴ TUE does not apply to differential conversions.

¹⁵ Voltages between V_{RL} and V_{RH} will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.

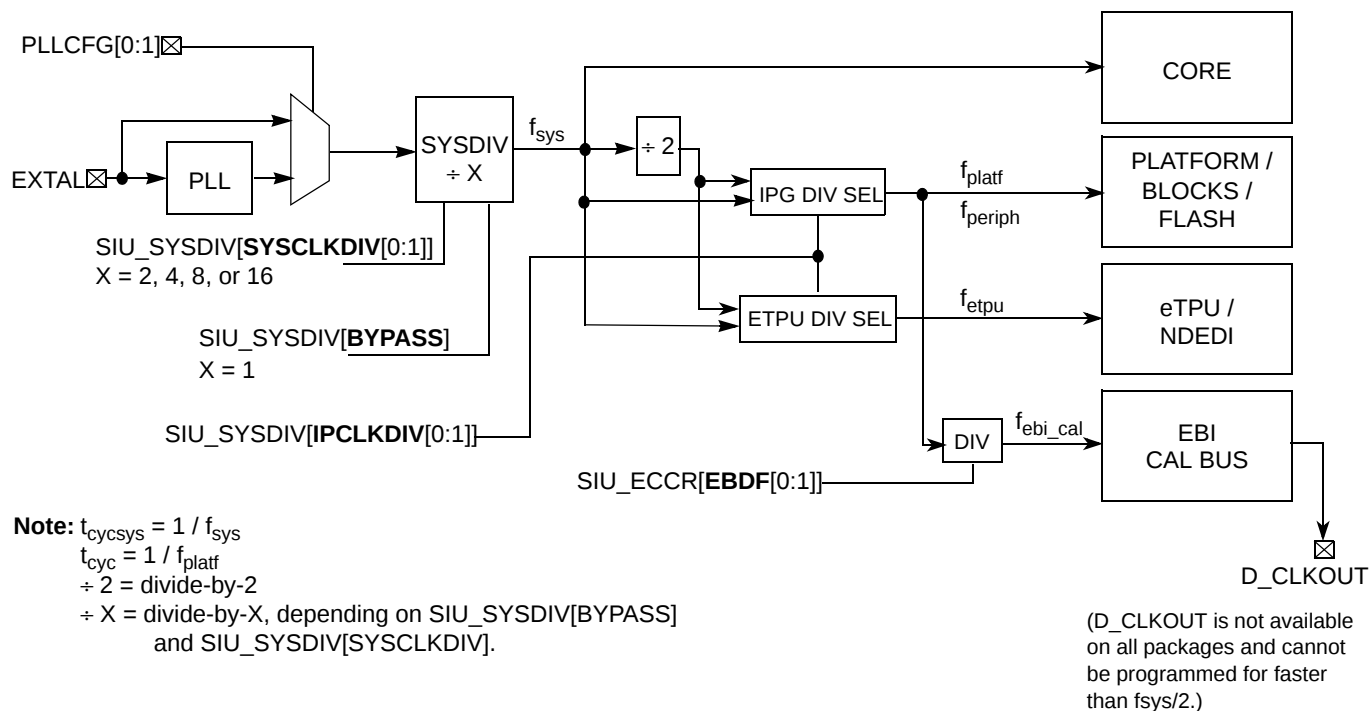


Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies^{1, 2}

Mode	SIU_ECCR [EBDF[0:1]] ³	f_{sys} (core)	f_{platt} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal} ^{4,5}	Unit
Enhanced	01	264	132	132	66	MHz
	11	264	132	132	33	
Full	01	200	100	200	50	MHz
	11	200	100	200	25	
Legacy	01	132	132	132	66	MHz
	11	132	132	132	33	

¹ The values in the table are specified at:
 $V_{DD} = 1.02 \text{ V to } 1.32 \text{ V}$
 $V_{DDE} = 3.0 \text{ V to } 3.6 \text{ V}$
 $V_{DDEH} = 4.5 \text{ V to } 5.5 \text{ V}$
 V_{DD33} and $V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}$
 $T_A = T_L \text{ to } T_H$.

Table 36. Bus Operation Timing ¹ (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq) ^{2 3}		Unit	Notes
			Min	Max		
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIS}	5.0/4.5	—	ns	Input setup time selectable via SIU_ECCR[EBTS] bit: EBTS = 0; 5.0ns EBTS = 1; 4.5ns
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIH}	1.0	—	ns	
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 ⁵	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

¹ EBI timing specified at $V_{DD} = 1.08 \text{ V}$ to 1.32 V , $V_{DDE} = 3.0 \text{ V}$ to 3.6 V , V_{DD33} and $V_{DDSYN} = 3.0 \text{ V}$ to 3.6 V , $T_A = T_L$ to T_H , and $C_L = 30 \text{ pF}$ with DSC = 0b10.

² Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

³ Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

⁴ Refer to Fast pad timing in Table 31 and Table 32.

⁵ ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0 °C. 2.0 ns spec applies to temperatures > 0 °C. This spec has no dependency on SIU_ECCR[EBTS] bit.

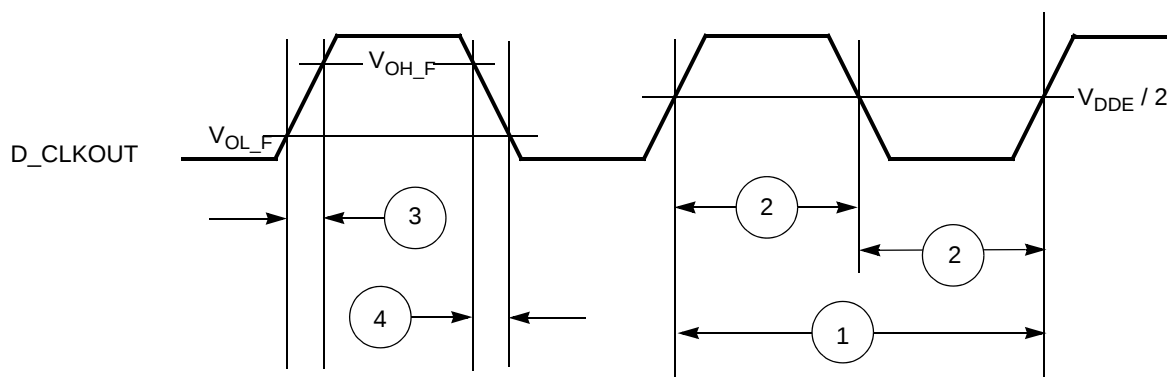


Figure 27. D_CLKOUT Timing

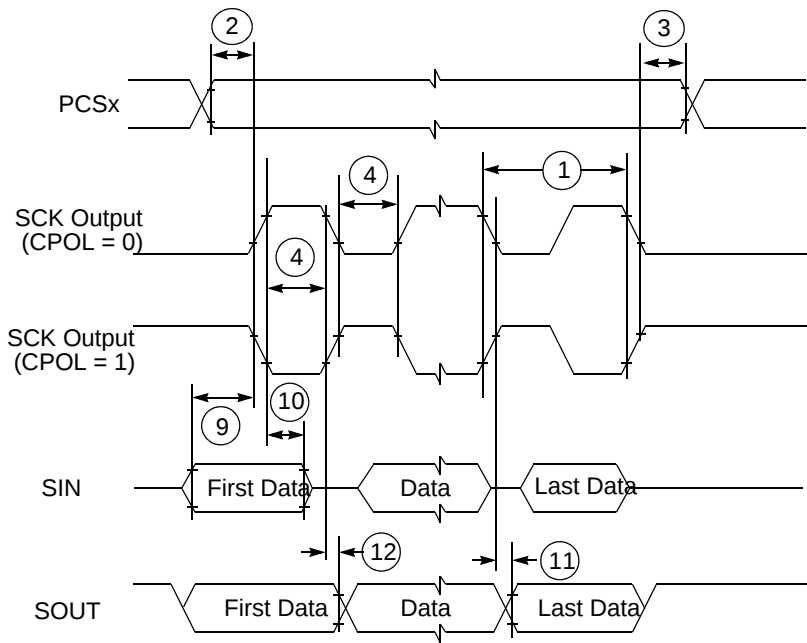


Figure 34. DSPI Classic SPI Timing — Master, CPHA = 0

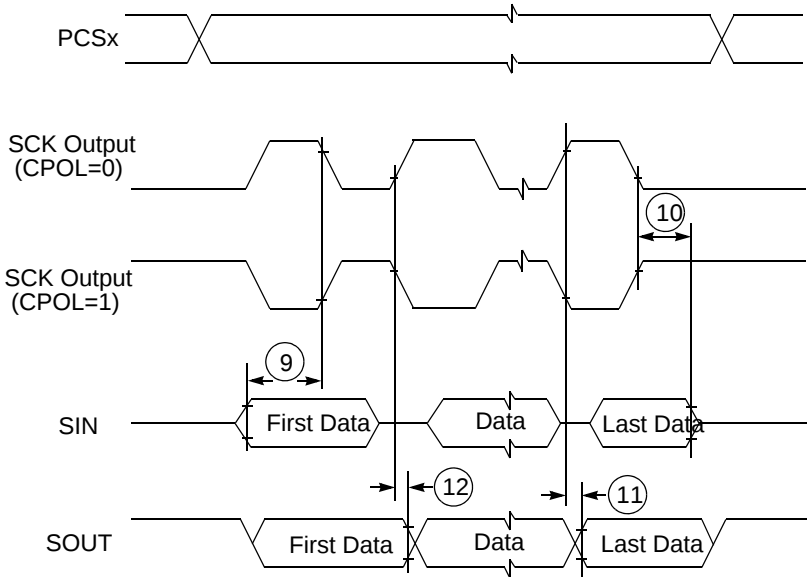


Figure 35. DSPI Classic SPI Timing — Master, CPHA = 1

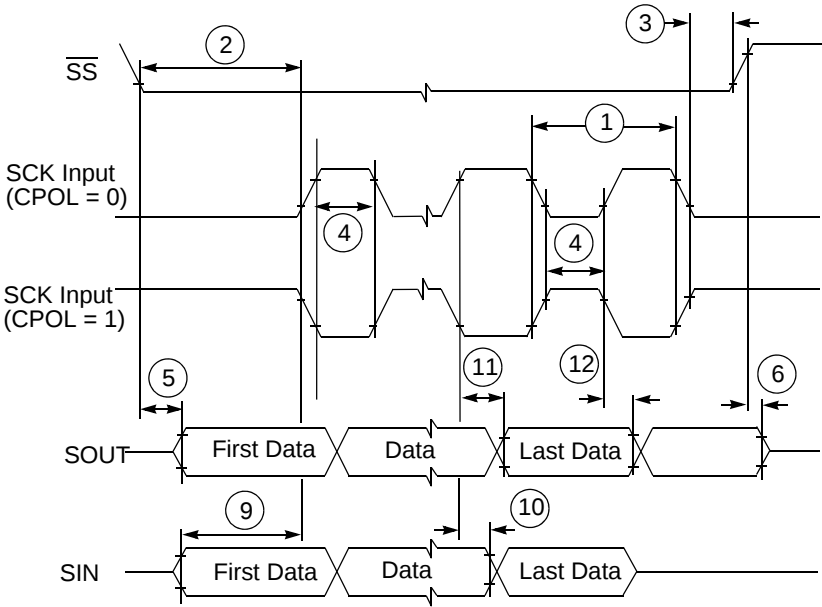


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

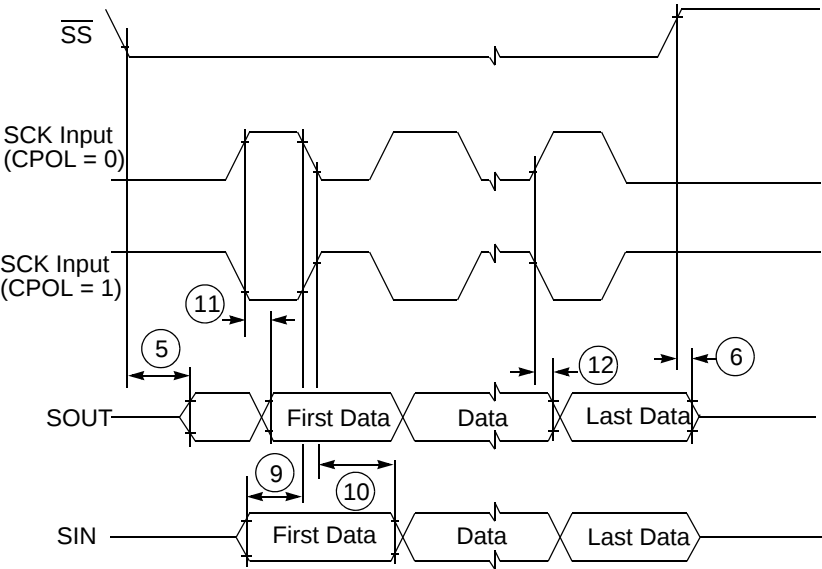


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

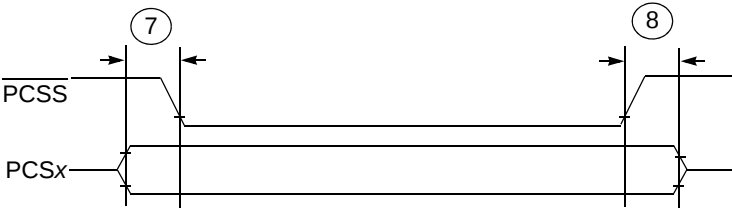


Figure 42. DSPI PCS Strobe (PCSS) Timing

5 Package Information

The latest package outline drawings are available on the product summary pages on our website: <http://www.freescale.com/powerarchitecture>. The following table lists the package case number. Use these numbers in the webpage’s keyword search engine to find the latest package outline drawings.

Table 42. Package Information

Package Type	Case Outline Number
324 TEPBGA	98ASS23840W
416 TEPBGA	98ARE10523D
516 TEPBGA	98ARS10503D

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
GPIO, IRQ, FlexRay												
440	TCRCLKC_ GPIO440 ⁹	P	—	—	—	MH	V _{DDEH7}	—/Up	—/Up	B22	B26	F22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO440	GPIO	I/O							
441	ETPUC0_ GPIO441 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	C21	C25	C25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO441	GPIO	I/O							
442	ETPUC1_ GPIO442 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	D20	C26	C26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO442	GPIO	I/O							
443	ETPUC2_ GPIO443 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	D22	D25	D25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO443	GPIO	I/O							
444	ETPUC3_ GPIO444 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	D21	D26	D26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO444	GPIO	I/O							
445	ETPUC4_ GPIO445 ⁹	P	—	—	—	MH	V _{DDEH7}	—/WKPCFG	—/WKPCFG	E22	E24	E24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO445	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V _{DDA_A0}	AN27	AN27	—	B13	B13
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V _{DDA_A0}	AN28	AN28	—	A13	A13
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V _{DDA_A0}	AN29	AN29	—	B14	A14
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V _{DDA_B1}	AN30	AN30	—	C14	B14
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V _{DDA_B1}	AN31	AN31	—	D14	C14
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V _{DDA_B1}	AN32	AN32	—	A14	B15
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN33	AN33	—	B15	D14
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN34	AN34	—	C15	C15
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN35	AN35	—	D15	D15
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V _{DDA_B1}	AN36	AN36	—	A15	A15
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN37	AN37	—	C16	C17
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN38	AN38	—	C17	D16
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V _{DDA_B0}	AN39	AN39	—	D16	C16
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB0	ANB0	B15	C18	C18
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB1	ANB1	B16	D17	D17
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB2	ANB2	A17	D18	D18
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB3	ANB3	A18	D19	D19
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB4	ANB4	B17	C19	B19
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB5	ANB5	B18	C20	A20
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB6	ANB6	A19	B19	C20
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V _{DDA_B0}	ANB7	ANB7	A20	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V _{DDA_B0}	ANB8	ANB8	D13	B20	B20

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
88	CNRXC_PCSD4_GPIO88	P	CNRXC	FlexCAN C receive	I	MH	V _{DDEH4}	—/Up	—/Up	W17	AE20	AE20
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO88	GPIO	I/O							
246	CNTXD_GPIO246	P	CNTXD	FlexCAN D transmit	O	MH	V _{DDEH4}	—/Up	—/Up	AB21	AD20	AD20
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO246	GPIO	I/O							
247	CNRXD_GPIO247	P	CNRXD	FlexCAN D receive	I	MH	V _{DDEH4}	—/Up	—/Up	Y19	AC20	AC20
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO247	GPIO	I/O							
eSCI												
89	TXDA_GPIO89	P	TXDA	eSCI A transmit	O	MH	V _{DDEH1}	—/Up	—/Up	—	M2	K2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO89	GPIO	I/O							
90	RXDA_GPIO90	P	RXDA	eSCI A receive	I	MH	V _{DDEH1}	—/Up	—/Up	—	M3	K3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO90	GPIO	I							
91	TXDB_PCSD1_GPIO91	P	TXDB	eSCI B transmit	O	MH	V _{DDEH1}	—/Up	—/Up	—	P1	K1
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO91	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
262	D_ADD15_ GPIO262	P	D_ADD15	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	R4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO262	GPIO	I/O							
263	D_ADD16_D_ADD_DAT16_ GPIO263	P	D_ADD16	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	R5
		A1	D_ADD_DAT16	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO263	GPIO	I/O							
264	D_ADD17_D_ADD_DAT17_ GPIO264	P	D_ADD17	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	T5
		A1	D_ADD_DAT17	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO264	GPIO	I/O							
265	D_ADD18_D_ADD_DAT18_ GPIO265	P	D_ADD18	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	T2
		A1	D_ADD_DAT18	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO265	GPIO	I/O							
266	D_ADD19_D_ADD_DAT19_ GPIO266	P	D_ADD19	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	T3
		A1	D_ADD_DAT19	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO266	GPIO	I/O							
267	D_ADD20_D_ADD_DAT20_ GPIO267	P	D_ADD20	EBI address bus	I/O	F	V _{DDE8}	—/Up	—/Up	—	—	T4
		A1	D_ADD_DAT20	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO267	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	P25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO278	GPIO	I/O							
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	P26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO279	GPIO	I/O							
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	N24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO280	GPIO	I/O							
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	N25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO281	GPIO	I/O							
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V _{DDE10}	—/Up	—/Up	—	—	N26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO282	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V _{DDE10}	—/Up	—/Up	—	—	P24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO299	GPIO	I/O							
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V _{DDE9}	—/Up	—/Up	—	—	AF9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO300	GPIO	I/O							
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V _{DDE9}	—/Up	—/Up	—	—	AB10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO301	GPIO	I/O							
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V _{DDE8}	—/Up	—/Up	—	—	M2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO302	GPIO	I/O							
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V _{DDE8}	—/Up	—/Up	—	—	N2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO303	GPIO	I/O							
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V _{DDE8}	—/Up	—/Up	—	—	N3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO304	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
213	WKPCFG_NMI_ GPIO213	P	WKPCFG	Weak pull configuration input	I	MH	V _{DDEH1}	WKPCFG/Up	Input/Up	—	N3	M5
		A1	NMI	Critical interrupt to core ¹¹	I							
		A2	—	—	—							
		G	GPIO213	GPIO	I							
208	PLLCFG0_IRQ4_ GPIO208	P	PLLCFG0	FMPLL mode configuration input	I	MH	V _{DDEH1}	PLLCFG/Up	Input/Up	M3	R3	M3
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO208	GPIO	I/O							
209	PLLCFG1_IRQ5_ GPIO209	P	PLLCFG1	FMPLL mode configuration input	I	MH	V _{DDEH1}	PLLCFG/Up	Input/Up (for Rev2 of the device: —/Up)	L2	P2	L1
		A1	IRQ5	External interrupt request	I							
		A2	SOUTD	DSPI D data output	O							
		G	GPIO209	GPIO	I/O							
—	PLLCFG2	P	PLLCFG2	FMPLL mode configuration input	I	MH	V _{DDEH1}	PLLCFG/ Down	PLLCFG/ Down	L3	P3	L2
—	XTAL	P	XTAL	Crystal oscillator output	O	AE	V _{DD33}	XTAL	XTAL	W22	AC26	AC26
—	EXTAL	P	EXTAL	Crystal oscillator input	I	AE	V _{DD33}	EXTAL	EXTAL	V22	AB26	AB26
229	D_CLKOUT	P	D_CLKOUT	EBI system clock output	O	F	V _{DDE9}	CLKOUT/ Enabled	CLKOUT/ Enabled	—	—	AF12
214	ENGCLK	P	ENGCLK	EBI engineering clock output Note: EXTCLK (External clock input) selected through SIU register)	O	F	V _{DDE2}	ENGCLK/ Enabled	ENGCLK/ Enabled	AA1	AD1	AD1
JTAG and Nexus (see footnote ¹² about resets)												
—	EVTI	₁₃	EVTI	Nexus event in	I	F	V _{DDE2}	—/Up	EVTI/Up	N4	T4	V1
227	EVTO (the BAM uses this pin to select if auto baud rate is on or off)	₁₃	EVTO	Nexus event out	O	F	V _{DDE2}	ABS/Up	EVTO/HI	P1	U1	V2
219	MCKO	₁₃	MCKO	Nexus message clock out	O	F	V _{DDE2}	O/Low	Disabled ¹⁴	N2	T2	U4

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
220	MDO0_GPIO220 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO0 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	MDO0/Low	P3	U3	V3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO220	GPIO	I/O							
221	MDO1_GPIO221 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO1 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	P4	U4	W6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO221	GPIO	I/O							
222	MDO2_GPIO222 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO2 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	R1	V1	V4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO222	GPIO	I/O							
223	MDO3_GPIO223 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO3 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	R2	V2	V5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO223	GPIO	I/O							
75	MDO4_GPIO75 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO4 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	R3	V3	W1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO75	GPIO	I/O							
76	MDO5_GPIO76 (GPIO function on this pin is only available on Rev.2 of the device)	_13	MDO5 ¹⁵	Nexus message data out	O	F	V _{DDE2}	O/Low	—/Down	R4	V4	W2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO76	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR ¹	Signal Name ²	P/A/G ³	Function ⁴	Function Summary	Direction	Pad Type ⁵	Voltage ⁶	State during RESET ⁷	State after RESET ⁸	Package Location		
										324	416	516
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V _{DDSYN}	VSSSYN	VSSSYN	U22	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V _{DDEH1}	VSTBY	VSTBY	K4	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V _{DDREG}	REGSEL	REGSEL	V20	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V _{DDREG}	REGCTL	REGCTL	T22	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V _{SS}	I	VSS	V _{DDREG}	VSSFL	VSSFL	V21	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V _{DDREG}	VDDREG	VDDREG	U21	AA25	AA25

¹ The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

² The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

³ P/A/G stands for Primary/Alternate/GPIO. This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

⁴ Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

⁵ MH = High voltage, medium speed

F = Fast speed

FS = Fast speed with slew

AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)

VHV = Very high voltage

⁶ VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

⁷ The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

⁸ The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

⁹ This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU_C.

¹⁰ During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

¹¹ NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.

Table 45 lists the pin locations of the power and ground signals on the 416 TEPBGA package.

Table 45. 416-pin Power Supply Locations

VDD

A2	B3	C4	D5	N4	AB4	AB23	AC3	AC12	AC24	AD2	AD25	AE1	AE26
----	----	----	----	----	-----	------	-----	------	------	-----	------	-----	------

VDD33

M1	AA4	AA23
----	-----	------

VDDE2

N10	P10	P11	R10	R11	T1	T10	T11	T12	U10	U11	U12	W4	AC1	AC5	AF2
-----	-----	-----	-----	-----	----	-----	-----	-----	-----	-----	-----	----	-----	-----	-----

VDDEH1

B1	P4
----	----

VDDEH3

AC10	AF5
------	-----

VDDEH4

AC11	AF22
------	------

VDDEH5

AC21	AF25
------	------

VDDEH6

N23	AC25
-----	------

VDDEH7

D24	E23	M26
-----	-----	-----

VSS

A1	A26	B2	B25	C3	C24	D4	D23	K10	K11	K12	K13	K14	K15	K16	K17	L10	L11
L12	L13	L14	L15	L16	L17	M10	M11	M12	M13	M14	M15	M16	M17	N11	N12	N13	N14
N15	N16	N17	P12	P13	P14	P15	P16	P17	R12	R13	R14	R15	R16	R17	T13	T14	T15
T16	T17	U13	U14	U15	U16	U17	AC4	AC23	AD3	AD24	AE2	AE25	AF1	AF26			

Table 47. Revision History (continued)

Revision (Date)	Description of changes
8 (Jun-2011)	Removed spec 3 from Table 27 "PFCPR1 Settings vs Frequency of Operation" Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 "PMC Electrical Specifications" to a max value of $V_{DD12OUT} + 17\%$. Updated item 26 (Operating Current VDDA Supply) in table 14 "Electrical Specifications" from 30 mA to 40 mA. Updated Note 11 for Table 14 (Electrical Specifications) to read $IOH_F = \{16,32,47,77\}$ mA and $IOL_F = \{24,48,71,115\}$ mA for $\{00,01,10,11\}$ drive mode with $VDDE = 3.0$ V. Updated ID 9 in Table 11 (PMC Electrical Specifications) to $V_{REG} = 4.5$ V, max DC output current with a max of 80 mA $V_{REG} = 4.25$ V, max DC output current, crank condition with a max of 40 mA Updated Table 17 (DSPI LVDS Pad Specification) with the following: - Spec 1 typical value updated from 40 MHz to 50 MHz - Spec 2 added SRC conditions and associated values: - SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV - SRC=0b01 Min 90 mV Max 320 mV - SRC=0b10 Min 160 mV Max 480 mV - Spec 3 - Min value from 1.075 V to 1.06 V - Max value from 1.325 V to 1.39 V - Added Spec 5, 6 and 7 Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to < 400 us as the Max vaule. Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications" Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications". Updated ID 16 in Table 11, "PMC Electrical Specifications", SMPS regulator clock frequency (after reset) 2.4MHz Max Updated Table 16 "Flash EEPROM Module Life", spec 3, 'Blocks with 10,001–100,000 P/E cycles' to 5 Years. Added Typ column to Table 25, "Flash Program and Erase Specifications" Updated Table 3, "Absolute Maximum Ratings" with the following: - Spec 1, '1.2 V Core Supply Voltage', to a Max of 2.0 V - Spec 3, 'Clock Synthesizer Voltage', to a Max of 5.3 V - Spec 4, 'I/O Supply Voltage' to a Max of 5.3 V - Spec 5, 'Analog Supply Voltage' to a Max of 5.3 V - Note 2 to read, "2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining." - Note 3, "... 5.0 V + 10% ..." to "... 5.25 V + 10 % ..." - Note 5, "... 3.3 V + 10% ..." to "... 3.60 V + 10 % ..." Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, "ESD Ratings", to 500 V Updated Table 27, "PFCPR1 Settings vs. Frequency of Operation", Spec 3, APC = RWSC column to 0b100. Updated Spec 26, "Operating Current 5.0 V Supplies @ $f_{sys} = 264$ MHz" for I_{DDA} to 50 mA, in Table 14, "DC electrical specifications".

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