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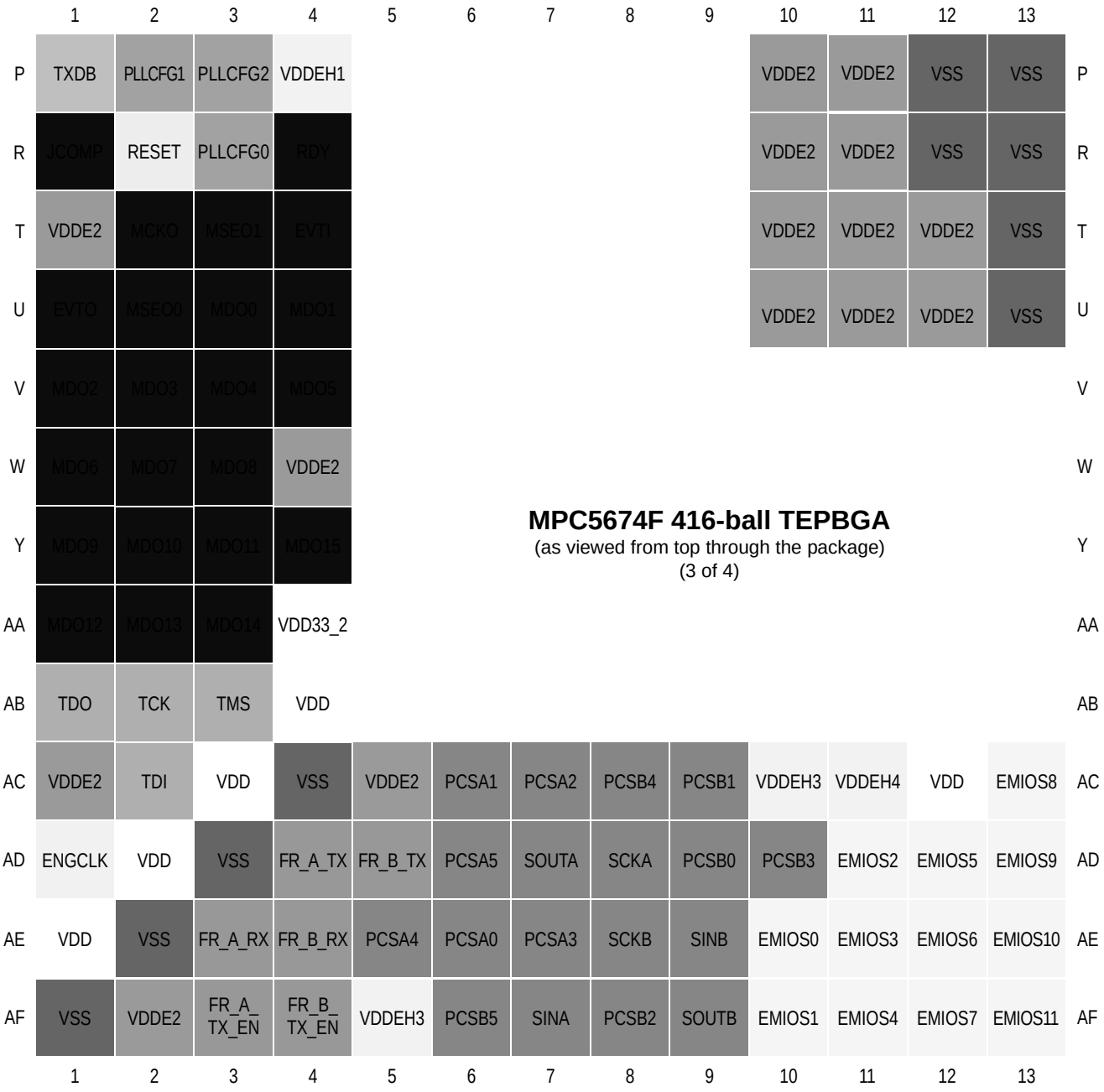
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674ff3mvv3r



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

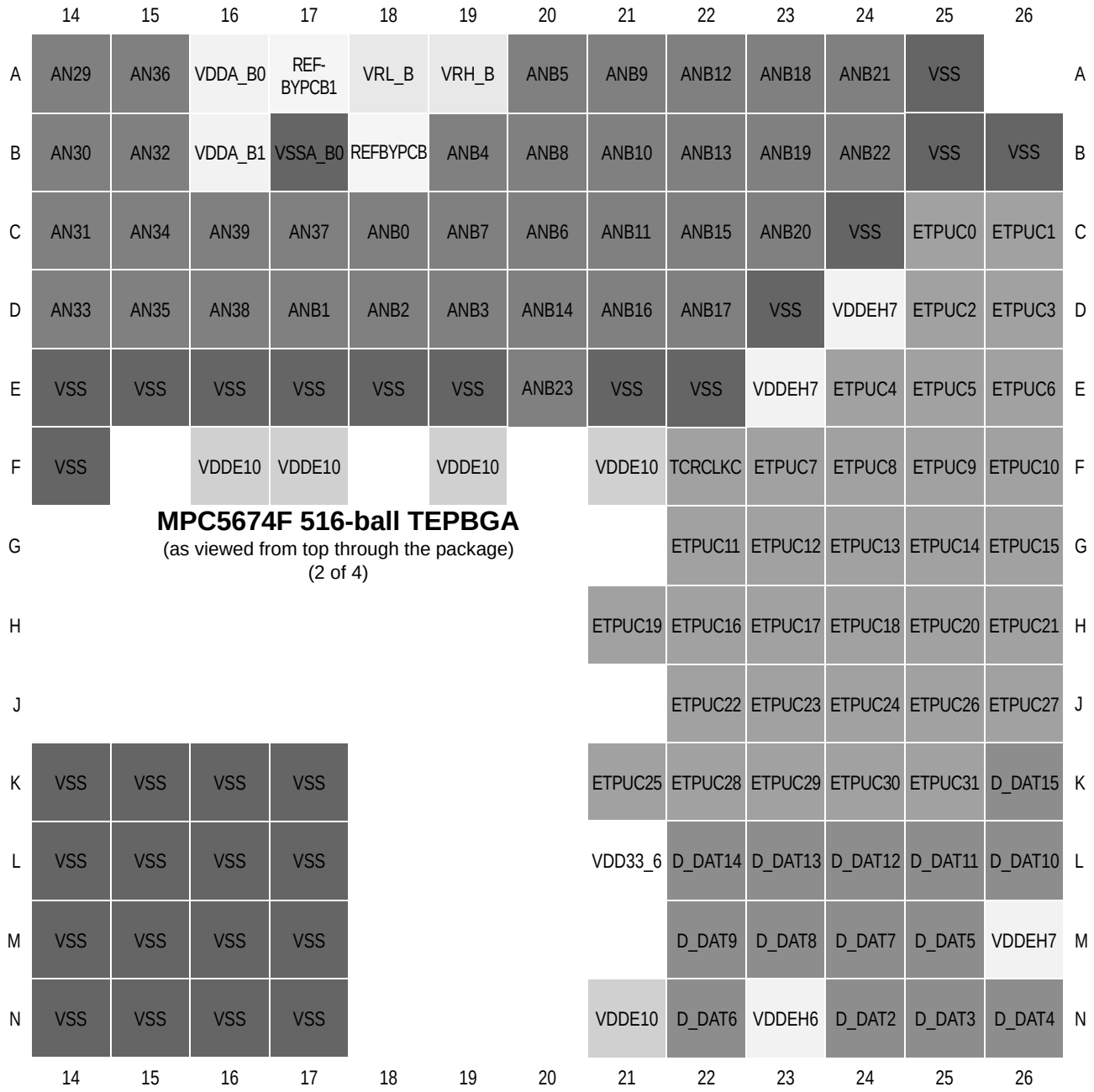


Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.freescale.com and perform a keyword search for “radiated emissions.” The following tables list the values of the device's radiated emissions operating behaviors.

Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	26	dBµV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	24	dBµV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 850 0.10 0.15	 mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[14] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[14] 7[15]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[16] 1.0 22	 mA mA mA

4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

Table 17. DSPI LVDS pad specification

#	Characteristic	Symbol	Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate							
1	Data Frequency	$f_{LVDSCLK}$	—	—	50	—	MHz
Driver Specs							
2	Differential output voltage	V_{OD}	SRC=0b00 or 0b11	150	—	400	mV
			SRC=0b01	90	—	320	
			SRC=0b10	160	—	480	
3	Common mode voltage (LVDS), VOS	V_{OS}	—	1.06	1.2	1.39	V
4	Rise/Fall time	T_R/T_F	—	—	2	—	ns
5	Propagation delay (Low to High)	T_{PLH}	—	—	4	—	ns
6	Propagation delay (High to Low)	T_{PHL}	—	—	4	—	ns
7	Delay (H/L), sync Mode	t_{PDSYNC}	—	—	4	—	ns
8	Delay, Z to Normal (High/Low)	T_{DZ}	—	—	500	—	ns
9	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	—	—	—	0.5	ns
Termination							
10	Trans. Line (differential Zo)	—	—	95	100	105	ohms
11	Temperature	—	—	–40	—	150	°C

4.8 Oscillator and FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference (PLLCFG2 = 0b1)	 $f_{ref\_crystal}$ $f_{ref\_crystal}$ f_{ref_ext} f_{ref_ext}	 8 16 8 16	 20 40[3] 20 40	MHz
2	Loss of Reference Frequency[4]	f_{LOR}	100	1000	kHz
3	Self Clocked Mode Frequency[5]	f_{SCM}	4	16	MHz
4	PLL Lock Time[6]	t_{LPLL}	—	< 400	µs

2 Up to the maximum frequency rating of the device (refer to Table 1). The f_{sys} speed is the nominal maximum frequency. 270 Mhz parts allow for 264 Mhz system clock + 2% FM.

3 See the *MPC5674F Reference Manual* for full description as not all bit combinations are valid.

4 EBI/Calibration bus is not available in all packages.

5 The EBI/Calibration Bus operating frequency, f_{ebi_cal} , depends on clock divider settings of block's max allowed frequency of operation. Normally $f_{ebi\_cal} = f_{platf}$ /2, but can be limited to < f_{platf} /2 in Full Mode.

Table 29. IPCLKDIV Settings

SIU_SYSDIV [IPCLKDIV[0:1]]	Mode	Description
00	Enhanced	CPU frequency is doubled (Max 264Mhz). Platform, peripheral, and eTPU clocks are 1/2 of CPU frequency
01	Full	CPU and eTPU frequency is doubled (Max 200Mhz). Platform and peripheral clocks are 1/2 of CPU frequency.
10	—	Reserved
11	Legacy	CPU, eTPU, platform, and peripheral's clocks all run at same speed (Max 132Mhz).

Table 30. SYSCLKDIV Settings

SIU_SYSDIV [SYSCLKDIV[0:1]]	Description
00	Divide by 2.
01	Divide by 4.
10	Divide by 8.
11	Divide by 16.

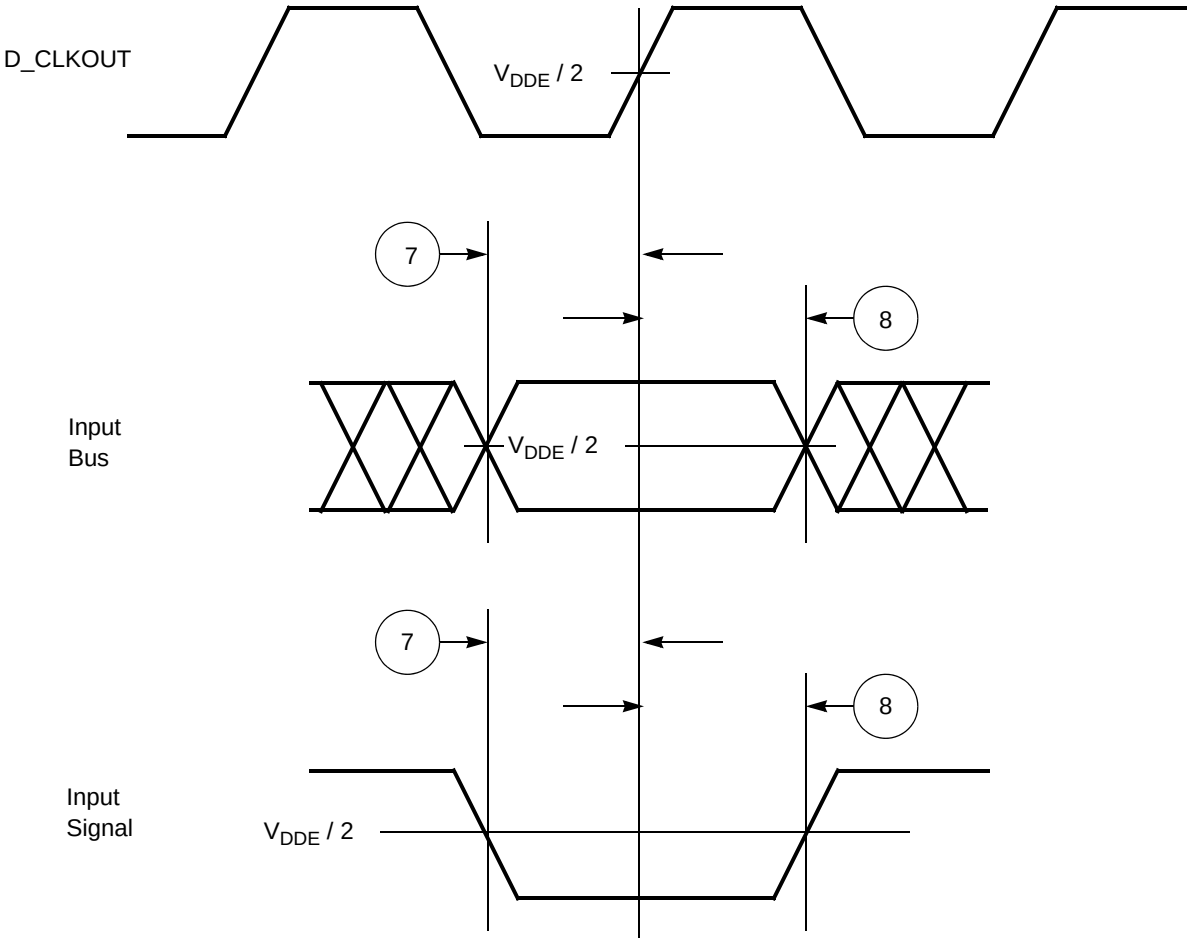


Figure 29. Synchronous Input Timing

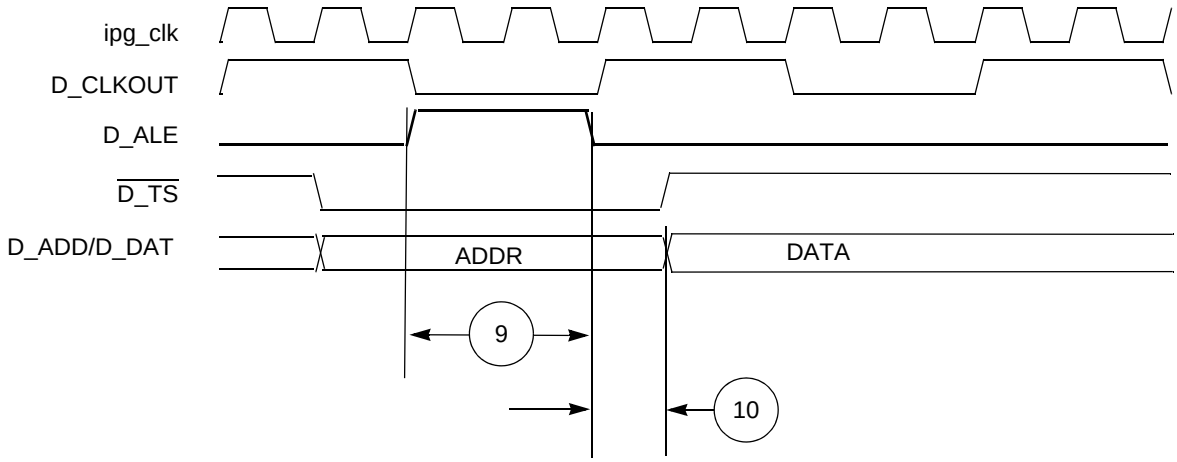


Figure 30. ALE Signal Timing

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO131	GPIO	I/O							
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO132	GPIO	I/O							
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO133	GPIO	I/O							
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E1	F2	F2
		A1	IRQ8	External interrupt request	I							
		A2	—	—	—							
		G	GPIO134	GPIO	I/O							
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C1	F3	F3
		A1	IRQ9	External interrupt request	I							
		A2	—	—	—							
		G	GPIO135	GPIO	I/O							
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E2	F4	F4
		A1	IRQ10	External interrupt request	I							
		A2	—	—	—							
		G	GPIO136	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D3	D3
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO143	GPIO	I/O							
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E4	C1	C1
		A1	PCSC3	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO144	GPIO	I/O							
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D3	C2	C2
		A1	PCSC4	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO145	GPIO	I/O							
eTPU_B												
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up	—/Up	P19	T23	V25
		A1	IRQ6	External interrupt request	I							
		A2	—	—	—							
		G	GPIO146	GPIO	I/O							
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N19	T24	V26
		A1	ETPUB16	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO147	GPIO	I/O							
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R19	T25	U22
		A1	ETPUB17	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO148	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
149	ETPUB2_ETPUB18_ GPIO149	P	ETPUB2	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R22	T26	U23
		A1	ETPUB18	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO149	GPIO	I/O							
150	ETPUB3_ETPUB19_ GPIO150	P	ETPUB3	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R21	R23	T22
		A1	ETPUB19	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO150	GPIO	I/O							
151	ETPUB4_ETPUB20_ GPIO151	P	ETPUB4	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P22	R24	U24
		A1	ETPUB20	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO151	GPIO	I/O							
152	ETPUB5_ETPUB21_ GPIO152	P	ETPUB5	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P21	R25	U25
		A1	ETPUB21	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO152	GPIO	I/O							
153	ETPUB6_ETPUB22_ GPIO153	P	ETPUB6	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N22	R26	U26
		A1	ETPUB22	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO153	GPIO	I/O							
154	ETPUB7_ETPUB23_ GPIO154	P	ETPUB7	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M19	P23	T23
		A1	ETPUB23	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO154	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA10	AE11	AE13
		A1	ETPUA3	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO182	GPIO	I/O							
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB10	AF11	AF13
		A1	ETPUA4	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO183	GPIO	I/O							
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y11	AD12	AF14
		A1	ETPUA5	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO184	GPIO	I/O							
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	—	AE12	AE14
		A1	ETPUA6	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO185	GPIO	I/O							
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB11	AF12	AD14
		A1	ETPUA7	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO186	GPIO	I/O							
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W10	AC13	AC14
		A1	ETPUA8	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO187	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27	AN27	—	B13	B13
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28	AN28	—	A13	A13
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29	AN29	—	B14	A14
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30	AN30	—	C14	B14
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31	AN31	—	D14	C14
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32	AN32	—	A14	B15
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33	AN33	—	B15	D14
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34	AN34	—	C15	C15
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35	AN35	—	D15	D15
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36	AN36	—	A15	A15
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37	AN37	—	C16	C17
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38	AN38	—	C17	D16
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39	AN39	—	D16	C16
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0	ANB0	B15	C18	C18
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1	ANB1	B16	D17	D17
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2	ANB2	A17	D18	D18
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3	ANB3	A18	D19	D19
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4	ANB4	B17	C19	B19
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5	ANB5	B18	C20	A20
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6	ANB6	A19	B19	C20
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7	ANB7	A20	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	ANB8	D13	B20	B20

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
88	CNRXC_PCSD4_ GPIO88	P	CNRXC	FlexCAN C receive	I	MH	V_{DDEH4}	—/Up	—/Up	W17	AE20	AE20
		A1	PCSD4	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO88	GPIO	I/O							
246	CNTXD_ GPIO246	P	CNTXD	FlexCAN D transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AB21	AD20	AD20
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO246	GPIO	I/O							
247	CNRXD_ GPIO247	P	CNRXD	FlexCAN D receive	I	MH	V_{DDEH4}	—/Up	—/Up	Y19	AC20	AC20
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO247	GPIO	I/O							
eSCI												
89	TXDA_ GPIO89	P	TXDA	eSCI A transmit	O	MH	V_{DDEH1}	—/Up	—/Up	—	M2	K2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO89	GPIO	I/O							
90	RXDA _ GPIO90	P	RXDA	eSCI A receive	I	MH	V_{DDEH1}	—/Up	—/Up	—	M3	K3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO90	GPIO	I							
91	TXDB_PCSD1_ GPIO91	P	TXDB	eSCI B transmit	O	MH	V_{DDEH1}	—/Up	—/Up	—	P1	K1
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO91	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
102	SCKB_ GPIO102	P	SCKB	DSPI B clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y8	AE8	AC8
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO102	GPIO	I/O							
103	SINB_ GPIO103	P	SINB	DSPI B data input	I	MH	V_{DDEH3}	—/Up	—/Up	AA8	AE9	AB9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO103	GPIO	I/O							
104	SOUTB_ GPIO104	P	SOUTB	DSPI B data output	O	MH	V_{DDEH3}	—/Up	—/Up	AB8	AF9	AA10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO104	GPIO	I/O							
105	PCSB0_PCSD2_ GPIO105	P	PCSB0	DSPI B peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	Y9	AD9	AF8
		A1	PCSD2	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO105	GPIO	I/O							
106	PCSB1_PCSD0_ GPIO106	P	PCSB1	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	—	AC9	AE8
		A1	PCSD0	DSPI D peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO106	GPIO	I/O							
107	PCSB2_SOUTC_ GPIO107	P	PCSB2	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	W7	AF8	AD8
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO107	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
EBI												
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	—/Up	—	—	AD9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO256	GPIO	I/O							
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	—/Up	—	—	U1
		A1	D_ADD_DAT31	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO257	GPIO	I/O							
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	—/Up	—	—	T6
		A1	D_TEA	EBI transfer error acknowledge	I							
		A2	—	—	—							
		G	GPIO258	GPIO	I/O							
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO259	GPIO	I/O							
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO260	GPIO	I/O							
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO261	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V_{DDE10}	—/Up	—/Up	—	—	P24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO299	GPIO	I/O							
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO300	GPIO	I/O							
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V_{DDE9}	—/Up	—/Up	—	—	AB10
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO301	GPIO	I/O							
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V_{DDE8}	—/Up	—/Up	—	—	M2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO302	GPIO	I/O							
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO303	GPIO	I/O							
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO304	GPIO	I/O							

Table 45 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 44. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13	J14	J9
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13	M14	N11
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3							

Table 47. Revision History (continued)

Revision (Date)	Description of changes
8 (Jun-2011)	Removed spec 3 from Table 27 “PFCPR1 Settings vs Frequency of Operation” Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 “PMC Electrical Specifications“ to a max value of VDD12OUT + 17%. Updated item 26 (Operating Current VDDA Supply) in table 14 “Electrical Specifications” from 30 mA to 40 mA. Updated Note 11 for Table 14 (Electrical Specifications) to read IOH_F = {16,32,47,77} mA and IOL_F = {24,48,71,115} mA for {00,01,10,11} drive mode with VDDE = 3.0 V. Updated ID 9 in Table 11 (PMC Electrical Specifications) to V_{REG} = 4.5 V, max DC output current with a max of 80 mA V_{REG} = 4.25 V, max DC output current, crank condition with a max of 40 mA Updated Table 17 (DSPI LVDS Pad Specification) with the following: • Spec 1 typical value updated from 40 MHz to 50 MHz • Spec 2 added SRC conditions and associated values: – SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV – SRC=0b01 Min 90 mV Max 320 mV – SRC=0b10 Min 160 mV Max 480 mV • Spec 3 - Min value from 1.075 V to 1.06 V - Max value from 1.325 V to 1.39 V • Added Spec 5, 6 and 7
	Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to < 400 us as the Max vaule. Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications" Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications". Updated ID 16 in Table 11, “PMC Electrical Specifications”, SMPS regulator clock frequency (after reset) 2.4MHz Max
	Updated Table 16 “Flash EEPROM Module Life”, spec 3, ‘Blocks with 10,001–100,000 P/E cycles’ to 5 Years. Added Typ column to Table 25, “Flash Program and Erase Specifications”
	Updated Table 3, “Absolute Maximum Ratings” with the following: - Spec 1, ‘1.2 V Core Supply Voltage’, to a Max of 2.0 V - Spec 3, ‘Clock Synthesizer Voltage’, to a Max of 5.3 V - Spec 4, ‘I/O Supply Voltage’ to a Max of 5.3 V - Spec 5, ‘Analog Supply Voltage’ to a Max of 5.3 V - Note 2 to read, “2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining.“ - Note 3, “... 5.0 V + 10% ...” to “... 5.25 V + 10 % ...” - Note 5, “... 3.3 V + 10% ...” to “... 3.60 V + 10 % ...” Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, “ESD Ratings”, to 500 V Updated Table 27, “PFCPR1 Settings vs. Frequency of Operation“, Spec 3, APC = RWSC column to 0b100. Updated Spec 26, “Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz“ for I_{DDA} to 50 mA, in Table 14, “DC electrical specifications”.