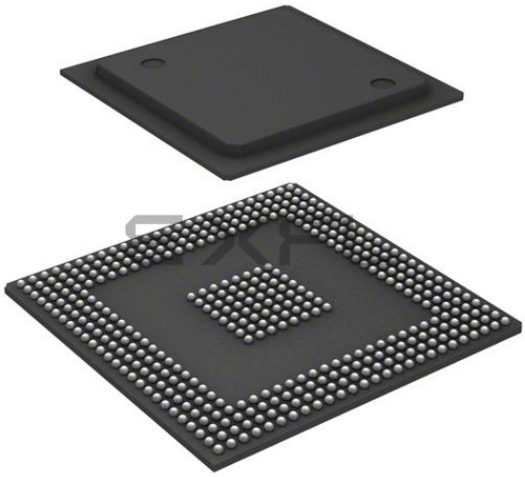

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674fk0mvr3

Table of Contents

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pulup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 usec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 uA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 12 and Table 13.

Table 12. Power Sequence Pin States for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 13. Power Sequence Pin States for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs Disabled
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs Disabled
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

1 The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

4.6.1 Power-Up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

Table 17. DSPI LVDS pad specification

#	Characteristic	Symbol	Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate							
1	Data Frequency	$f_{LVDSCLK}$	—	—	50	—	MHz
Driver Specs							
2	Differential output voltage	V_{OD}	SRC=0b00 or 0b11	150	—	400	mV
			SRC=0b01	90	—	320	
			SRC=0b10	160	—	480	
3	Common mode voltage (LVDS), VOS	V_{OS}	—	1.06	1.2	1.39	V
4	Rise/Fall time	T_R/T_F	—	—	2	—	ns
5	Propagation delay (Low to High)	T_{PLH}	—	—	4	—	ns
6	Propagation delay (High to Low)	T_{PHL}	—	—	4	—	ns
7	Delay (H/L), sync Mode	t_{PDSYNC}	—	—	4	—	ns
8	Delay, Z to Normal (High/Low)	T_{DZ}	—	—	500	—	ns
9	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	—	—	—	0.5	ns
Termination							
10	Trans. Line (differential Zo)	—	—	95	100	105	ohms
11	Temperature	—	—	–40	—	150	°C

4.8 Oscillator and FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference (PLLCFG2 = 0b1)	 $f_{ref\_crystal}$ $f_{ref\_crystal}$ f_{ref_ext} f_{ref_ext}	 8 16 8 16	 20 40[3] 20 40	MHz
2	Loss of Reference Frequency[4]	f_{LOR}	100	1000	kHz
3	Self Clocked Mode Frequency[5]	f_{SCM}	4	16	MHz
4	PLL Lock Time[6]	t_{LPLL}	—	< 400	µs

4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 22. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1, “Clocking.”

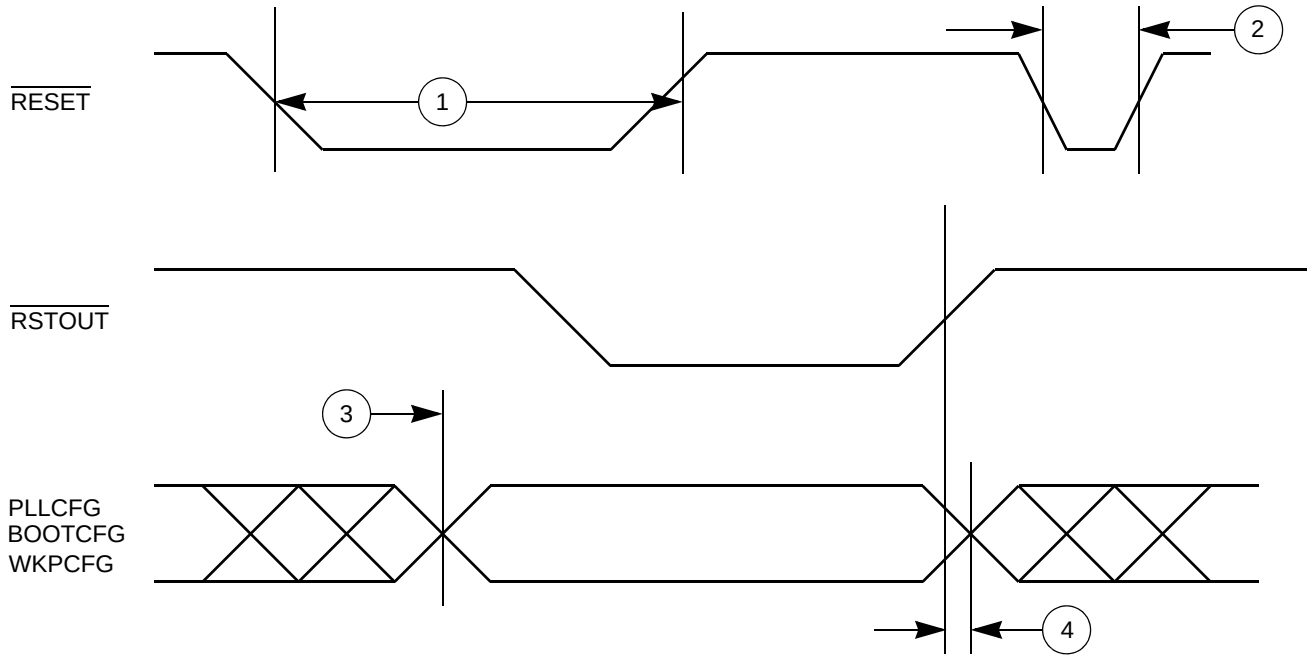

Figure 20. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 34. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

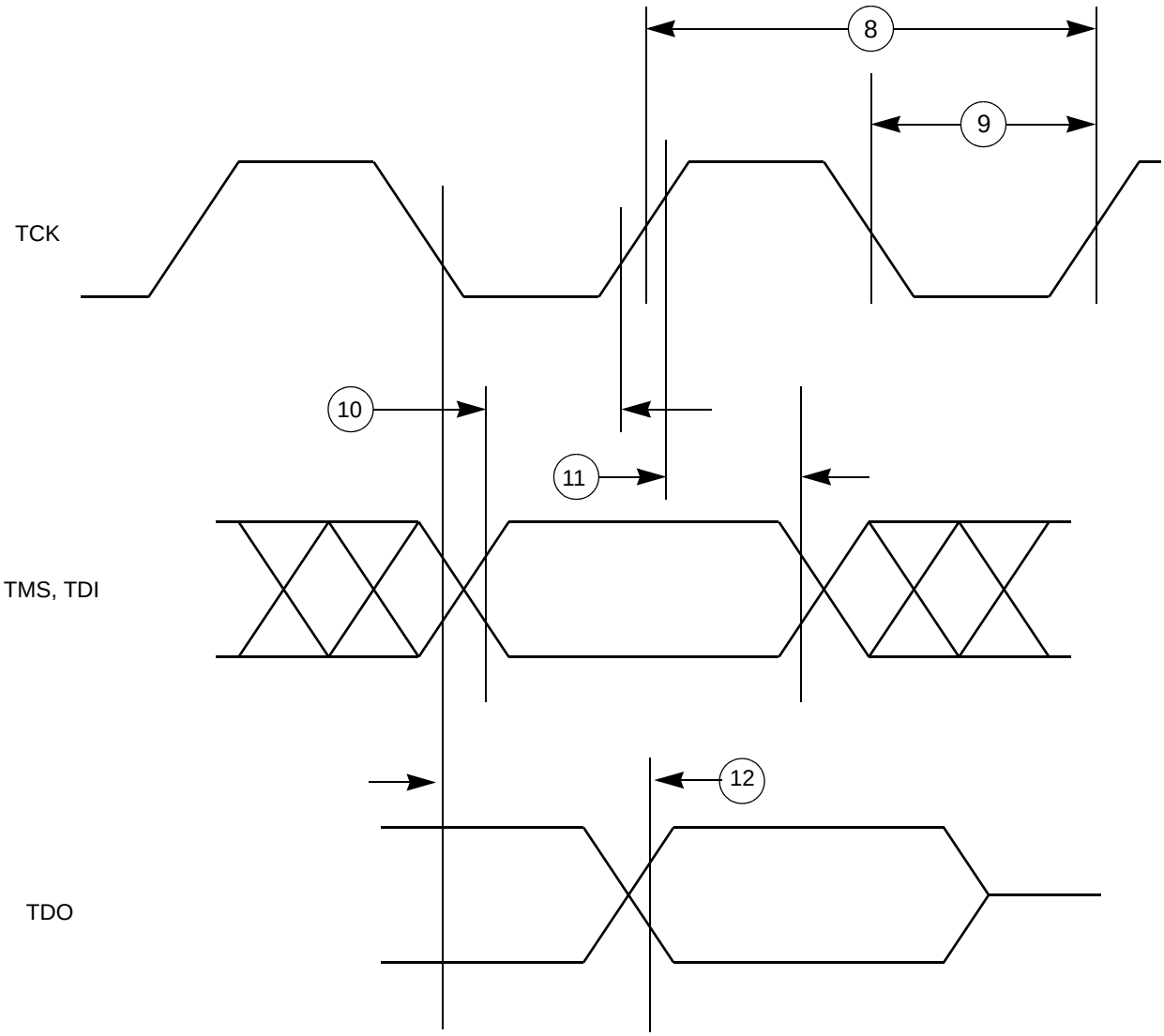

Figure 26. Nexus TCK, TDI, TMS, TDO Timing

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES: 5193 & 5198.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 516 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARS10503D	REV: B
	CASE NUMBER: 1164A–01	09 AUG 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 48. 516 TEPBGA Package (2 of 2)

6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5674F Microprocessor Reference Manual* (document number MPC5674FRM).

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0	VSSA_B0	B14	B17	B17
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1	REFBYPCB1	A14	A17	A17
FlexRay												
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y5	AD4	AD4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO248	GPIO	I/O							
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA4	AE3	AE3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO249	GPIO	I/O							
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AB3	AF3	AF3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO250	GPIO	I/O							
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y6	AD5	AD5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO251	GPIO	I/O							
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA5	AE4	AE4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO252	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
238	PCSC0_SOUT_C_LVDSM_ GPIO238	P	PCSC0	DSPI C peripheral chip select	I/O	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AB19	AE21	AE21
		A1	SOUT_C_LVDSM	LVDS– downstream signal negative output data	O							
		A2	—	—	—							
		G	GPIO238	GPIO	I/O							
239	PCSC1_ GPIO239	P	PCSC1	DSPI C peripheral chip select	O	MH	V_{DDEH4}	—/Up	—/Up	—	AC22	AC22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO239	GPIO	I/O							
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AE23	AE23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO240	GPIO	I/O							
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AD23	AD23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO241	GPIO	I/O							
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AF24	AF24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO242	GPIO	I/O							
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	—	AE24	AE24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO243	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB11
		A1	D_ADD_DAT21	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO268	GPIO	I/O							
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD10
		A1	D_ADD_DAT22	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO269	GPIO	I/O							
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE10
		A1	D_ADD_DAT23	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO270	GPIO	I/O							
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF10
		A1	D_ADD_DAT24	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO271	GPIO	I/O							
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD11
		A1	D_ADD_DAT25	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO272	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO278	GPIO	I/O							
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO279	GPIO	I/O							
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO280	GPIO	I/O							
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO281	GPIO	I/O							
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO282	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO288	GPIO	I/O							
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO289	GPIO	I/O							
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO290	GPIO	I/O							
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO291	GPIO	I/O							
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO292	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
293	D_ADD_DAT15_GPIO293	P	D_ADD_DAT15	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	K26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO293	GPIO	I/O							
294	D_RD_WR_GPIO294	P	D_RD_WR	EBI read/write	O	F	V_{DDE10}	—/Up	—/Up	—	—	R26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO294	GPIO	I/O							
295	D_WE0_GPIO295	P	D_WE0	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO295	GPIO	I/O							
296	D_WE1_GPIO296	P	D_WE1	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	P5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO296	GPIO	I/O							
297	D_OE_GPIO297	P	D_OE	EBI output enable	O	F	V_{DDE10}	—/Up	—/Up	—	—	P23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO297	GPIO	I/O							
298	D_TS_GPIO298	P	D_TS	EBI transfer start	O	F	V_{DDE9}	—/Up	—/Up	—	—	AE9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO298	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
77	MDO6_GPIO77 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO6[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	T1	W1	W3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO77	GPIO	I/O							
78	MDO7_GPIO78 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO7[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	T2	W2	Y1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO78	GPIO	I/O							
79	MDO8_GPIO79 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO8[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	T3	W3	W5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO79	GPIO	I/O							
80	MDO9_GPIO80 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO9[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U1	Y1	Y2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO80	GPIO	I/O							
81	MDO10_GPIO81 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO10[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U2	Y2	Y3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO81	GPIO	I/O							
82	MDO11_GPIO82 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO11[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U3	Y3	Y4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO82	GPIO	I/O							

Table 47. Revision History (continued)

Revision (Date)	Description of changes
8 (Jun-2011)	Removed spec 3 from Table 27 “PFCPR1 Settings vs Frequency of Operation” Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 “PMC Electrical Specifications“ to a max value of VDD12OUT + 17%. Updated item 26 (Operating Current VDDA Supply) in table 14 “Electrical Specifications” from 30 mA to 40 mA. Updated Note 11 for Table 14 (Electrical Specifications) to read IOH_F = {16,32,47,77} mA and IOL_F = {24,48,71,115} mA for {00,01,10,11} drive mode with VDDE = 3.0 V. Updated ID 9 in Table 11 (PMC Electrical Specifications) to V_{REG} = 4.5 V, max DC output current with a max of 80 mA V_{REG} = 4.25 V, max DC output current, crank condition with a max of 40 mA Updated Table 17 (DSPI LVDS Pad Specification) with the following: • Spec 1 typical value updated from 40 MHz to 50 MHz • Spec 2 added SRC conditions and associated values: – SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV – SRC=0b01 Min 90 mV Max 320 mV – SRC=0b10 Min 160 mV Max 480 mV • Spec 3 - Min value from 1.075 V to 1.06 V - Max value from 1.325 V to 1.39 V • Added Spec 5, 6 and 7
	Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to < 400 us as the Max vaule. Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications" Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications". Updated ID 16 in Table 11, “PMC Electrical Specifications”, SMPS regulator clock frequency (after reset) 2.4MHz Max
	Updated Table 16 “Flash EEPROM Module Life”, spec 3, ‘Blocks with 10,001–100,000 P/E cycles’ to 5 Years. Added Typ column to Table 25, “Flash Program and Erase Specifications”
	Updated Table 3, “Absolute Maximum Ratings” with the following: - Spec 1, ‘1.2 V Core Supply Voltage’, to a Max of 2.0 V - Spec 3, ‘Clock Synthesizer Voltage’, to a Max of 5.3 V - Spec 4, ‘I/O Supply Voltage’ to a Max of 5.3 V - Spec 5, ‘Analog Supply Voltage’ to a Max of 5.3 V - Note 2 to read, “2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining.“ - Note 3, “... 5.0 V + 10% ...” to “... 5.25 V + 10 % ...” - Note 5, “... 3.3 V + 10% ...” to “... 3.60 V + 10 % ...” Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, “ESD Ratings”, to 500 V Updated Table 27, “PFCPR1 Settings vs. Frequency of Operation“, Spec 3, APC = RWSC column to 0b100. Updated Spec 26, “Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz“ for I_{DDA} to 50 mA, in Table 14, “DC electrical specifications”.