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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674fk0mvy3

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

1.2 MPC567xF Family Differences

Table 2 lists the differences between the MPC567xF devices. Refer to the *MPC5674F Reference Manual* for a full feature list and comparison.

Table 2. MPC567xF Family Differences

Feature	MPC5674F	MPC5674F	MPC5673F	MPC5673F
Package	416 BGA 516 BGA	324 BGA	416 BGA 516 BGA	324 BGA
Flash	4 MB	4 MB	3 MB	3 MB
SRAM	256 KB	256 KB	192 KB	192 KB
External bus	Yes (516 BGA only)	No	Yes (516 BGA only)	No
Serial	3	2	3	2
eSCI_A	Yes	Yes	Yes	Yes
eSCI_B	Yes	Yes	Yes	Yes
eSCI_C	Yes	No	Yes	No
SPI	4	3	4	3
DSPI_A	Yes	No	Yes	No
DSPI_B	Yes	Yes	Yes	Yes
DSPI_C	Yes	Yes	Yes	Yes
DSPI_D	Yes	Yes	Yes	Yes
eMIOS	32 channel	22 channel	32 channel	22 channel
eTPU2	64 channel	47 channel	64 channel	47 channel
eTPU_A	Yes (32 ch)	Yes (26 ch)	Yes	Yes (26 ch)
eTPU_B	Yes (32 ch)	Yes (21 ch, no TCRCLK)	Yes	Yes (21 ch, no TCRCLK)
ADC	64 channel	48 channel	64 channel	48 channel
eQADC_A	Yes (64 ch)[1]	Yes (24 ch)	Yes (64 ch)[1]	Yes (24 ch)
eQADC_B		Yes (24 ch)		Yes (24 ch)

1 There are are two pairs of 24 channels plus 16 shared channels. This gives 64 channels total: 40 per ADC (since 16 are shared).

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

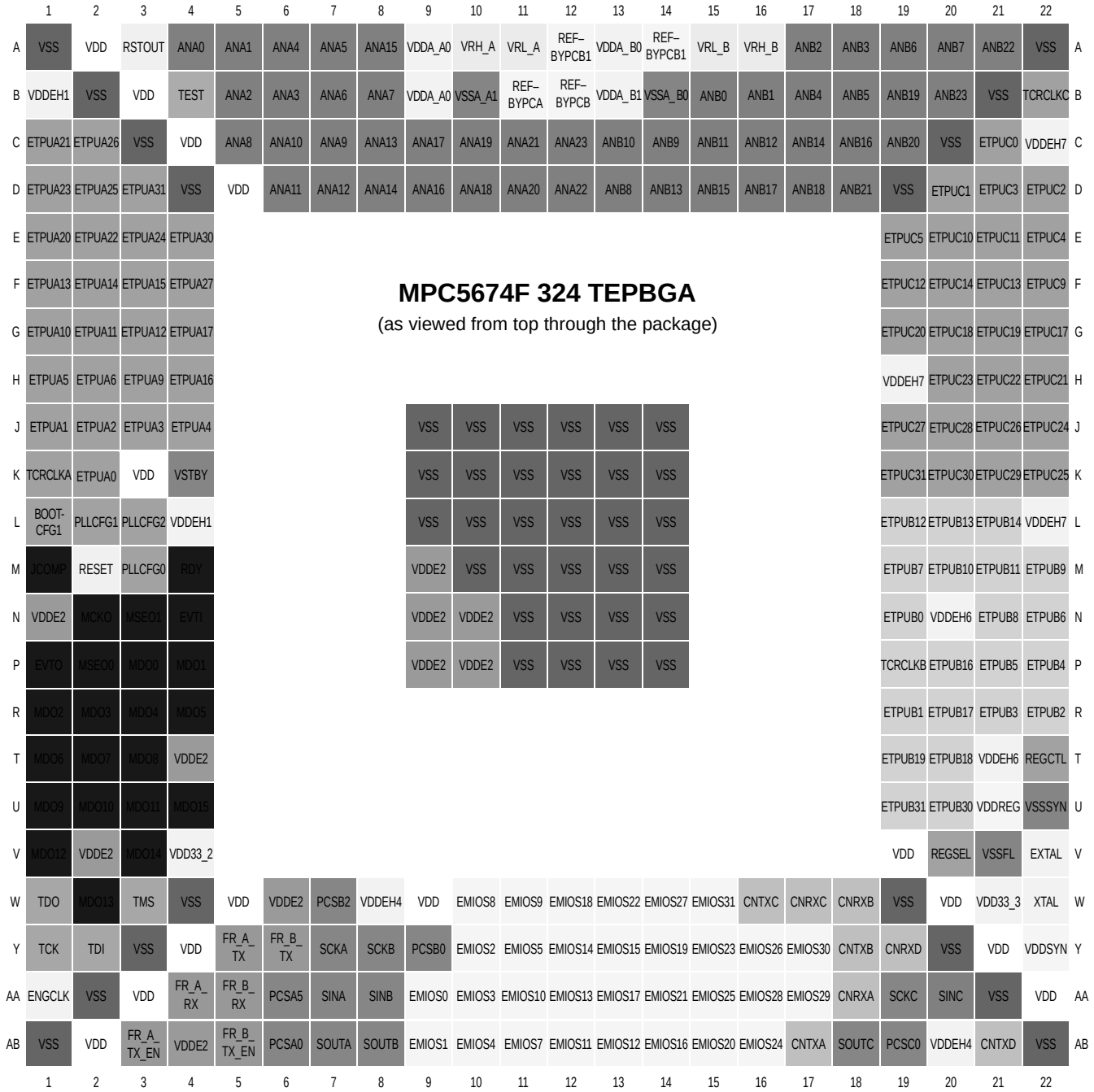


Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

3.4 Signal Properties and Muxing

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	–0.3	2.0 [2]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	6.4 [3,4]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	5.3 [4,5]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	5.3 [4,5]	V
5	Analog Supply Voltage (reference to V_{SSA}[6])	V_{DDA}[7]	–0.3	6.4 [3,4]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	5.3 [4,5]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	6.4 [3,4]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	6.4 [3,4]	V
9	Analog Reference High Voltage (reference to V_{RL}[8])	V_{RH}[9]	–0.3	6.4 [3,4]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	6.4 [3,4]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [10] (per pin, applies to all digital pins)	I_{MAXD}	–3 [11]	3 [11]	mA
16	Maximum Analog Input Current [12] (per pin, applies to all analog pins)	I_{MAXA}	– 3 [7]	3 [7,11]	mA
17	Maximum Operating Temperature Range [13] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [14] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [15]	MSL	—	3	—

[10] I_{OH_F} = {16,32,47,77} mA and I_{OL_F} = {24,48,71,115} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V. This spec is for characterization only.

[11] I_{OH_S} = {11.6} mA and IOL_S = {17.7} mA for {medium} I/O with V_{DDE} = 4.5 V;
I_{OH_S} = {5.4} mA and IOL_S = {8.1} mA for {medium} I/O with V_{DDE} = 3.0 V. These specs are for characterization only.

[12] Applies to D_CLKOUT, external bus pins, and Nexus pins.

[13] V_{STBY} current specified at 1.0 V at a junction temperature of 85 °C. V_{STBY} current is 700 µA maximum at a junction temperature of 150 °C.

[14] Power requirements for the V_{DD33} supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Section 4.7.2, “I/O Pad V_{DD33} Current Specifications,” for information on both fast (F, FS) and medium (MH) pads. Also refer to Table 16 for values to calculate power dissipation for specific operation.

[15] This value is a target that is subject to change.

[16] This value allows a 5 V reference to supply ADC + REF.

[17] Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Section 4.7.1, “I/O Pad Current Specifications,” for information on I/O pad power. Also refer to Table 15 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[18] Absolute value of current, measured at V_{IL} and V_{IH}.

[19] Absolute value of current, measured at V_{IL} and V_{IH}.

[20] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types F and MH.

[21] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types AE and AE/up-down. See Appendix A, Signal Properties and Muxing.

[22] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics

[23] Pull-up and pull-down resistances are both enabled and settings are equal.

4.7.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 15 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 15.

The AC timing of these pads are described in the Section 4.11.2, “Pad AC Specifications.”

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{DRV_MH}	50	50	5.25	11	16.0
2			20	50	5.25	01	6.3
3			3.0	50	5.25	00	1.1
4			2.0	200	5.25	00	2.4
5	Fast	I_{DRV_FC}	66	10	3.6	00	7.4
6			66	20	3.6	01	10.5
7			66	30	3.6	10	12.3
8			66	50	3.6	11	35.2

Table 18. FMPLL Electrical Specifications[1] (continued)

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
5	Duty Cycle of Reference [7]	t_{DC}	40	60	%
6	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
7	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
8	D_CLKOUT Period Jitter[8, 9] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
9	Peak-to-Peak Frequency Modulation Range Limit [10,11] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
10	FM Depth Tolerance[12]	C_{mod_err}	–0.25	0.25	%f_{sys}
11	VCO Frequency	f_{VCO}	192	600	MHz
12	Modulation Rate Limits[13]	f_{mod}	0.400	1	MHz
13	Predivider output frequency range[14]	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

6 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

7 For Flexray operation, duty cycle requirements are higher.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. D_CLKOUT divider set to divide-by-2.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

10 Modulation depth selected must not result in f_{pll} value greater than the f_{pll} maximum specified value.

11 Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 2%, 3%, and 4% peak-to-peak.

12 Depth tolerance is the programmed modulation depth ±0.25% of F_{sys}. Violating the VCO min/max range may prevent the system from exiting reset.

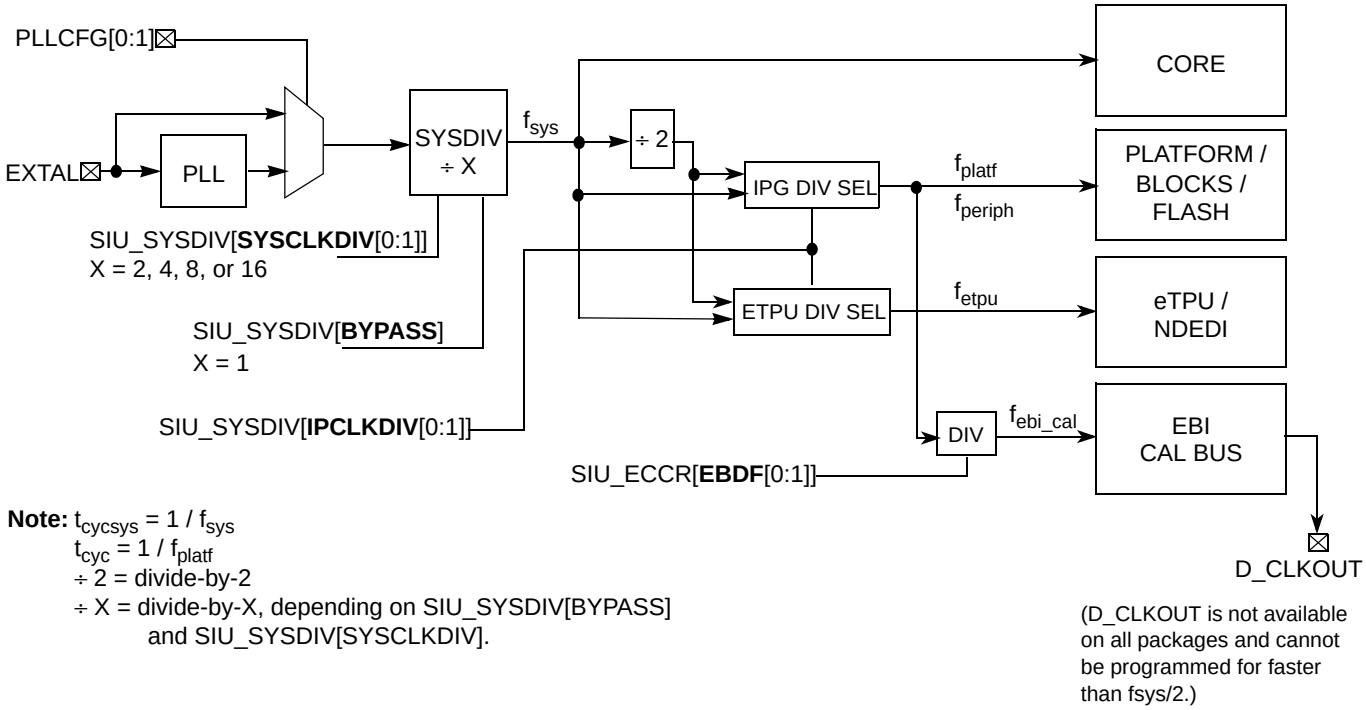
13 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

14 Violating this range will cause the VCO max/min range to be violated with the default MFD settings out of reset.

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.



Note: $t_{cycsys} = 1 / f_{sys}$
$t_{cyc} = 1 / f_{platf}$
÷ 2 = divide-by-2
÷ X = divide-by-X, depending on SIU_SYSDIV[BYPASS] and SIU_SYSDIV[SYSCLKDIV].

(D_CLKOUT is not available on all packages and cannot be programmed for faster than fsys/2.)

Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

4.11.2 Pad AC Specifications

Table 31. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	2.6
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

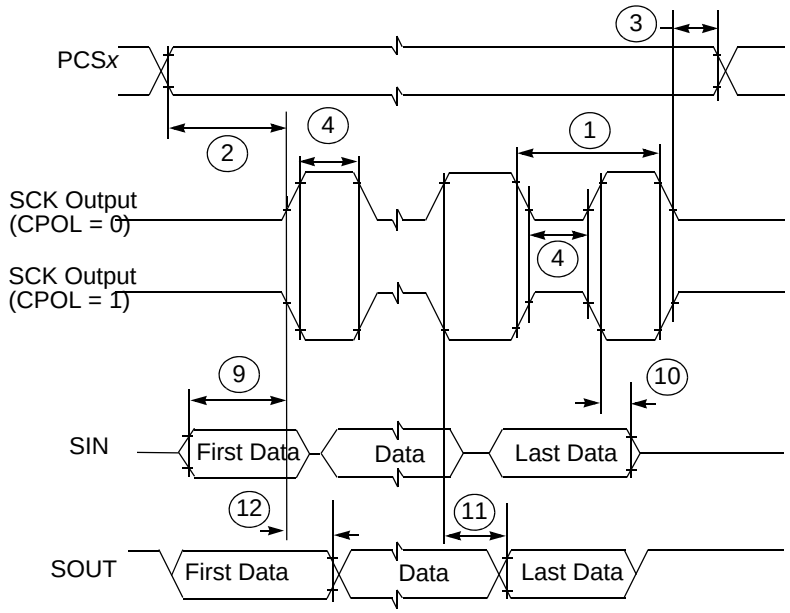


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

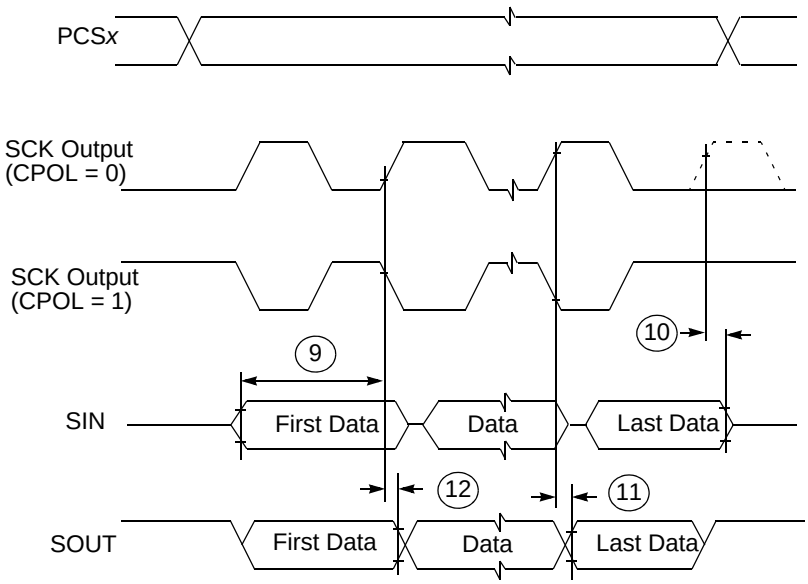


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

Figure 48. 516 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO125	GPIO	I/O							
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO126	GPIO	I/O							
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO127	GPIO	I/O							
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO128	GPIO	I/O							
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO129	GPIO	I/O							
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO130	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V26	W24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO167	GPIO	I/O							
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V25	V22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO168	GPIO	I/O							
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V24	V23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO169	GPIO	I/O							
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W26	U21
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO170	GPIO	I/O							
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W25	Y25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO171	GPIO	I/O							
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W24	W21
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO172	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
GPIO, IRQ, FlexRay												
440	TCRCLKC_ GPIO440[9]	P	—	—	—	MH	V_{DDEH7}	—/Up	—/Up	B22	B26	F22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO440	GPIO	I/O							
441	ETPUC0_ GPIO441[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	C21	C25	C25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO441	GPIO	I/O							
442	ETPUC1_ GPIO442[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	D20	C26	C26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO442	GPIO	I/O							
443	ETPUC2_ GPIO443[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	D22	D25	D25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO443	GPIO	I/O							
444	ETPUC3_ GPIO444[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	D21	D26	D26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO444	GPIO	I/O							
445	ETPUC4_ GPIO445[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E22	E24	E24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO445	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W11	AD13	AF15
		A1	ETPUA9	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO188	GPIO	I/O							
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA11	AE13	AE15
		A1	SCKD	DSPI D clock	O							
		A2	—	—	—							
		G	GPIO189	GPIO	I/O							
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB12	AF13	AB14
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO190	GPIO	I/O							
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB13	AF14	AD15
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO191	GPIO	I/O							
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA12	AE14	AC15
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO192	GPIO	I/O							
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y12	AC14	AF17
		A1	IRQ0	External interrupt request	I							
		A2	CNTXD	FlexCAN D transmit	O							
		G	GPIO193	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	ANB9	C14	D20	A21
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	ANB10	C13	B21	B21
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	ANB11	C15	A21	C21
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	ANB12	C16	C21	A22
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	ANB13	D14	D21	B22
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	ANB14	C17	A22	D20
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	ANB15	D15	B22	C22
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	ANB16	C18	C22	D21
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	ANB17	D16	A23	D22
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	ANB18	D17	B23	A23
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	ANB19	B19	C23	B23
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	ANB20	C19	D22	C23
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	ANB21	D18	A24	A24
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	ANB22	A21	B24	B24
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	ANB23	B20	A25	E20
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	VRH_A	A10	A12	A12
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	VRL_A	A11	A11	A11
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	VRH_B	A16	A19	A19
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	VRL_B	A15	A18	A18
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	REFBYPCB	B12	B18	B18
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	REFBYPCA	B11	B11	B11
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	VDDA_A0	A9	A9	A9
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	VDDA_A1	B9	B9	B9
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	REFBYPCA1	A12	A10	A10
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	VSSA_A1	B10	B10	B10
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	VDDA_B0	A13	A16	A16
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	VDDA_B1	B13	B16	B16

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO278	GPIO	I/O							
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	P26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO279	GPIO	I/O							
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO280	GPIO	I/O							
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO281	GPIO	I/O							
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO282	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO283	GPIO	I/O							
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO284	GPIO	I/O							
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO285	GPIO	I/O							
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO286	GPIO	I/O							
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO287	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO305	GPIO	I/O							
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO306	GPIO	I/O							
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	P3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO307	GPIO	I/O							
Reset and Clocks												
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	RESET/Up	M2	R2	N5
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	RSTOUT/ High	A3	A3	A3
211	BOOTCFG0_IRQ2_ GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	BOOTCFG/ Down	—	—	L4
		A1	IRQ2		I							
		A2	—	—	—							
		G	GPIO211	GPIO	I/O							
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	Input/Down	L1	N2	L3
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO212	GPIO	I/O							

Table 47. Revision History (continued)

Revision (Date)	Description of changes
9	Updated Table 1.,"Orderable Part Numbers" with actual available parts. Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200 MHz nom and max.—Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”. Updated footnotes of Table 3.,"Absolute Maximum Ratings" to: • 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining. • 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining. • 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining. Updated Table 6.,"Thermal Characteristics, 324-pin Package" to show MPC5674F thermal characteristics. In Table 10.,"PMC Operating conditions", updated the parameter “Supply voltage VDD 1.2V nominal" to “Core supply voltage". In Table 11.,"PMC Electrical Specifications", updated the following rows: • Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V. • The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%”, respectively. • The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%”, respectively. In Table 12.,"Power Sequence Pin States for MH and AE pads", updated the row (VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”. In Table 13.,"Power Sequence Pin States for F and FS pads", updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high), parameter “F and FS pad” to “Outputs Disabled”. In Table 14.,"DC Electrical Specifications", updated the spec 'Operating Current 1.2 V Supplies @ f_{SYS} = 264 MHz' with 'V_{DD} @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary. Updated current (mA) values in Table 15.,"V_{DDE}/V_{DDEH} I/O Pad Average DC Current" from Spec 5 to 13: • Spec 5 Current (mA) from 6.5 to 7.4 • Spec 6 Current (mA) from 9.4 to 10.5 • Spec 7 Current (mA) from 10.8 to 12.3 • Spec 8 Current (mA) from 33.3 to 35.2 • Spec 9 Current (mA) from 12.0 to 12.7 • Spec 10 Current (mA) from 6.2 to 6.7 • Spec 11 Current (mA) from 4.0 to 4.2 • Spec 12 Current (mA) from 2.4 to 2.6 • Spec 13 Current (mA) from8.9 to 9. In Table 35.,"Nexus Debug Port Timing", updated the footnote of parameter “tCYC” to “See Notes on tcyc in Table27”. Removed references to “Section I/O Pad VDD33 Current Specifications” .
10	Updated Figure 1.,"MPC5674F Orderable Part Number Description" with changes in “Revision of Silicon” and “Fab Revision ID”. Updated Table 1.,"Orderable Part Numbers" with changes in Part numbers and Package Description.
10.1	In Figure 1.,"MPC5674F Orderable Part Number Description", replaced “Revision of Silicon for TSMC is 0 for now. In future, it will be revision 1” with “0 = Rev 0 (TSMC14)”.