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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674fk0mvy3r

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3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

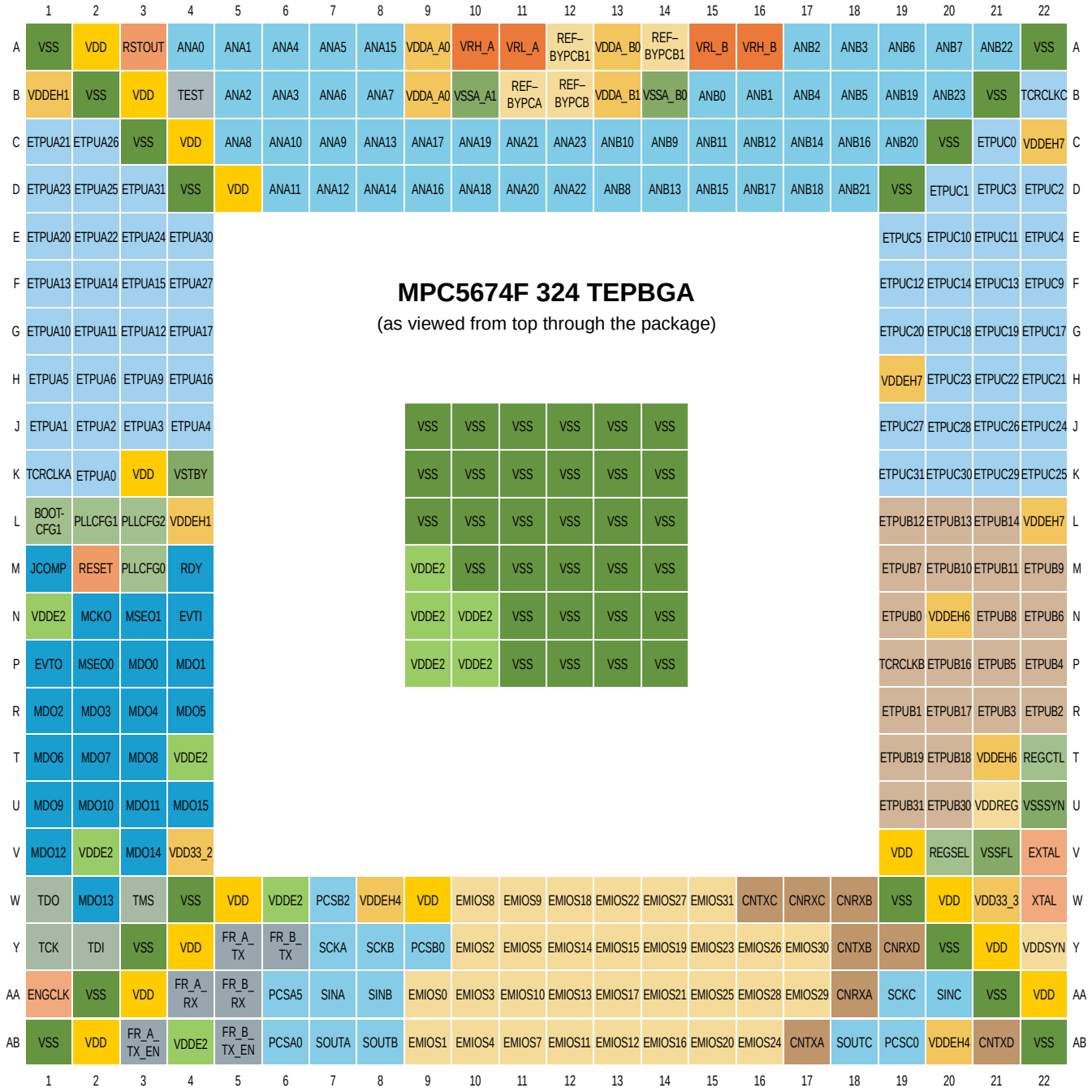
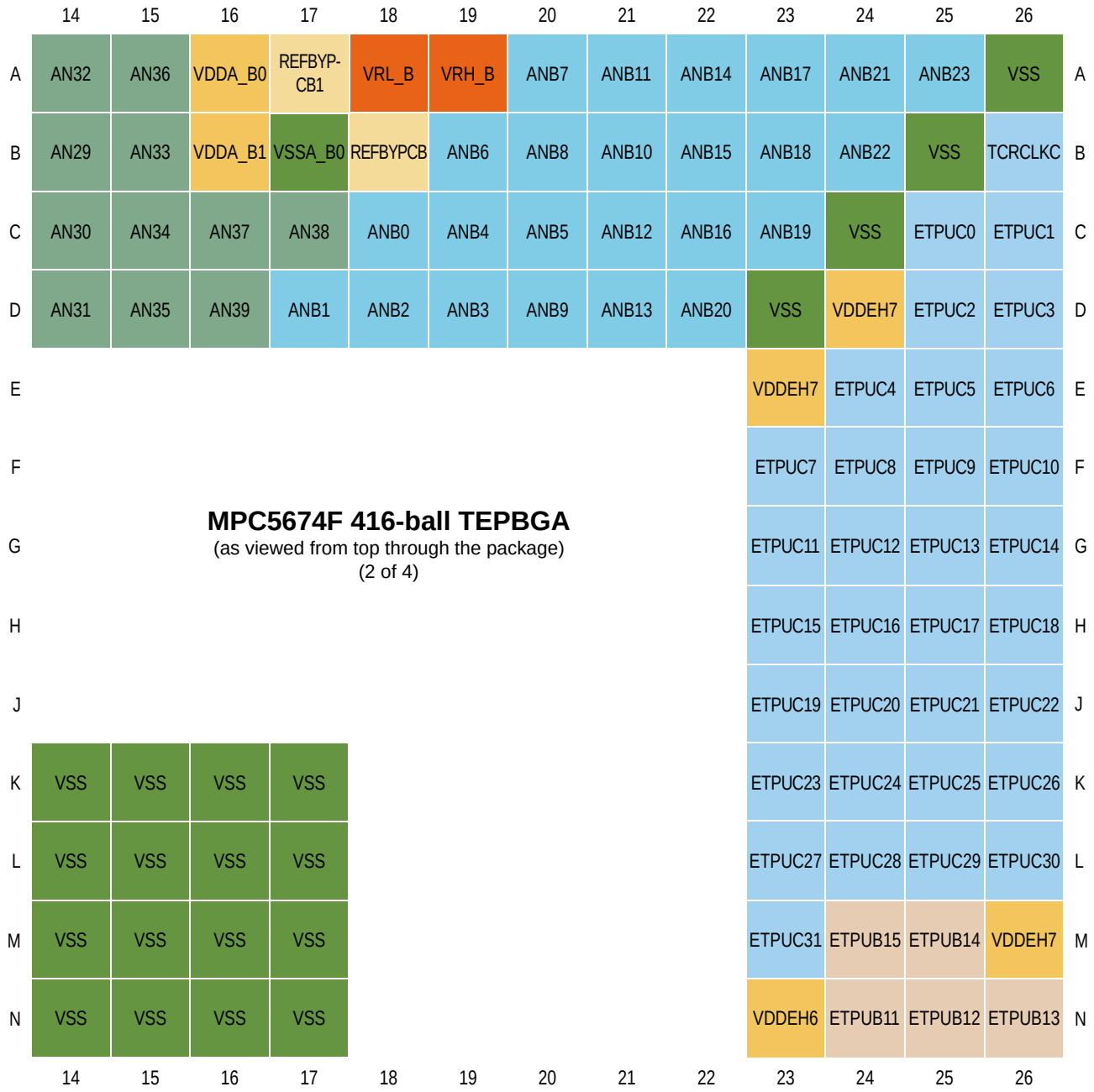


Figure 3. MPC5674F 324-ball TEPBGA (full diagram)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN32	AN36	VDDA_B0	REFBYP-CB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	AN29	AN33	VDDA_B1	VSSA_B0	REFBYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E										VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F										ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G										ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H										ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J										ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pulup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 usec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 uA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

4.11.2 Pad AC Specifications

Table 31. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	2.6
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 32. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

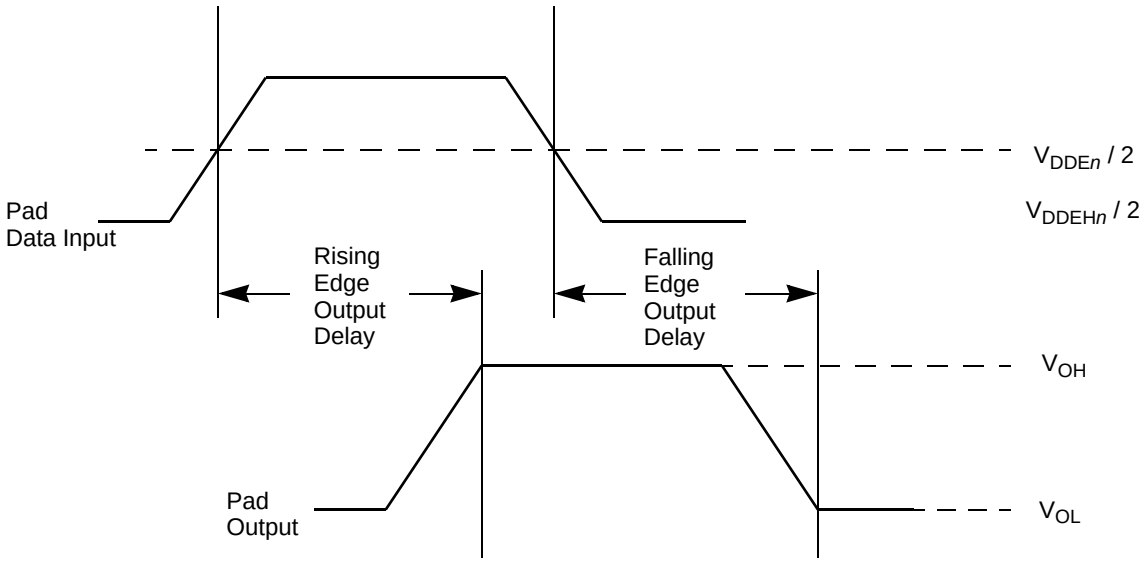


Figure 17. Pad Output Delay

4.12 AC Timing

4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 18 and Figure 19 apply to all I/O pins with pad types F and MH. See Appendix A, Signal Properties and Muxing, for the pad type for each pin.

4.12.5 External Bus Interface (EBI) Timing

Table 36. Bus Operation Timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	7.0/7.5	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 7.0 ns EBTS = 1: 7.5 ns

4.12.6 External Interrupt Timing (IRQ Pin)

Table 37. External Interrupt Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

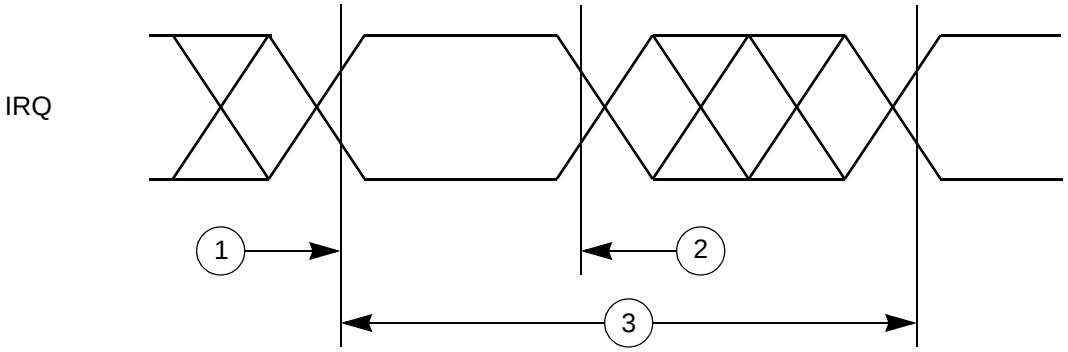


Figure 31. External Interrupt Timing

4.12.7 eTPU Timing

Table 38. eTPU Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

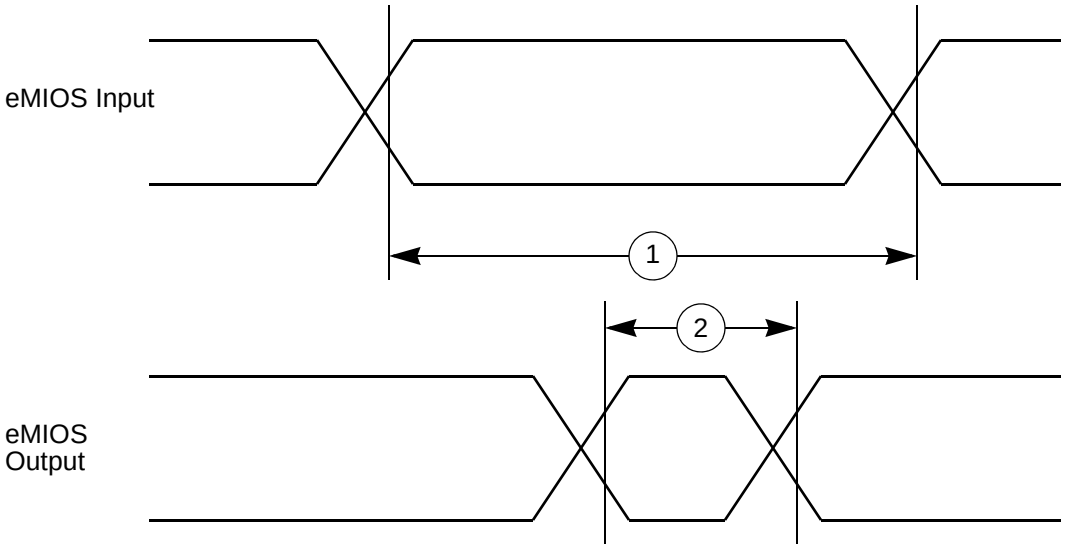


Figure 33. eMIOS Timing

4.12.9 DSPI Timing

Table 40. DSPI Timing[1 2]

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
1	DSPI Cycle Time[3, 4] Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	t_{SYS} * 2	t_{SYS}*32768*7	ns
2	PCS to SCK Delay[5]	t_{CSC}	12	—	ns
3	After SCK Delay[6] Master mode Slave mode	t_{ASC}	t_{SYS} * 2 t_{SYS} *3 – constraints [7]	—	ns
4	SCK Duty Cycle	t_{SDC}	0.33 * t_{SCK}	0.66 * t_{SCK}	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	t_{SYS} * 2	t_{SYS} * 7	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	t_{SYS} * 2	t_{SYS} * 7	ns

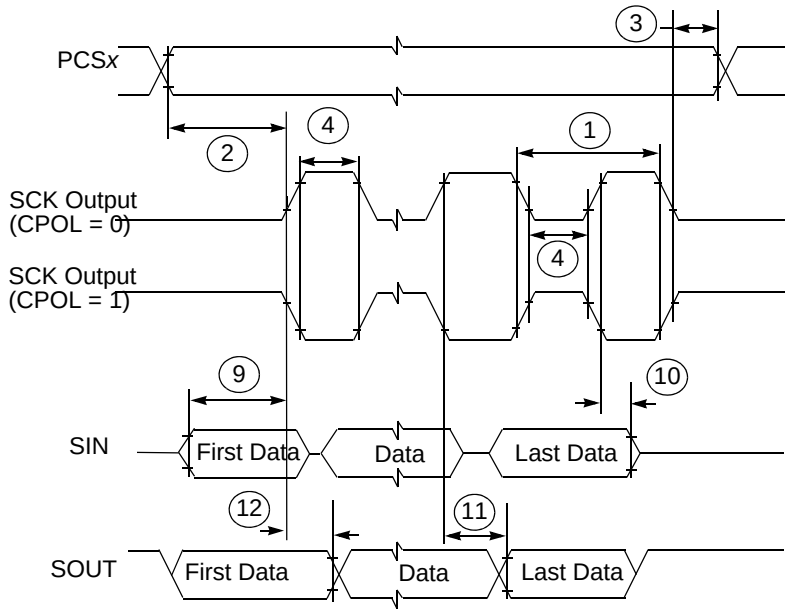


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

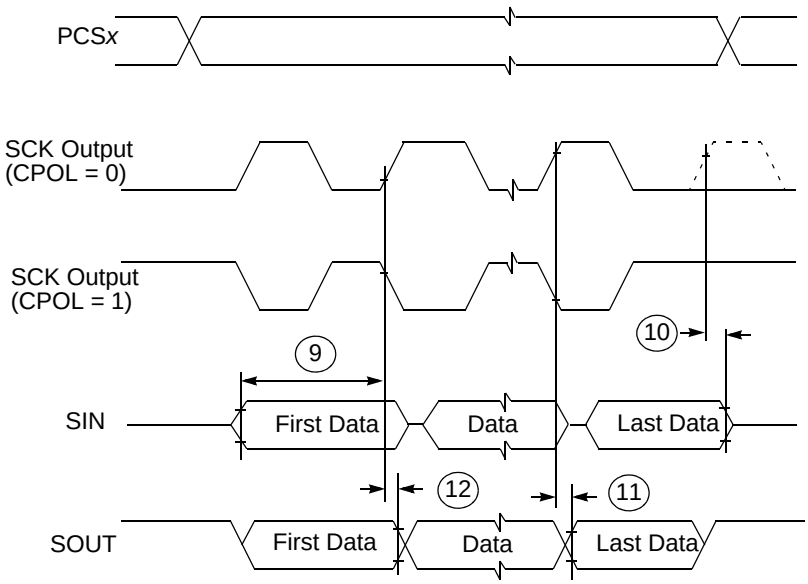


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASS23840W	REV: D
PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1158–03	26 APR 2006
	STANDARD: JEDEC MS–034 AAJ–1	

Figure 44. 324 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
eTPU_A												
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	K1	L1	K4
		A1	IRQ7	External interrupt request	I							
		A2	—	—	—							
		G	GPIO113	GPIO	I/O							
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO114	GPIO	I/O							
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO115	GPIO	I/O							
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO116	GPIO	I/O							
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO117	GPIO	I/O							
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO118	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H1	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO119	GPIO	I/O							
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H2	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO120	GPIO	I/O							
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	J1	H2
		A1	ETPUA19	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO121	GPIO	I/O							
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	J2	H3
		A1	ETPUA20	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO122	GPIO	I/O							
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H3	J3	J3
		A1	ETPUA21	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO123	GPIO	I/O							
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G1	J4	K6
		A1	ETPUA22	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO124	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA10	AE11	AE13
		A1	ETPUA3	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO182	GPIO	I/O							
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB10	AF11	AF13
		A1	ETPUA4	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO183	GPIO	I/O							
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y11	AD12	AF14
		A1	ETPUA5	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO184	GPIO	I/O							
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	—	AE12	AE14
		A1	ETPUA6	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO185	GPIO	I/O							
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB11	AF12	AD14
		A1	ETPUA7	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO186	GPIO	I/O							
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W10	AC13	AC14
		A1	ETPUA8	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO187	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA14	AE16	AE17
		A1	ETPUB5	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO200	GPIO	I/O							
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W13	AC16	AC16
		A1	ETPUB6	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO201	GPIO	I/O							
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y15	AD16	AA16
		A1	ETPUB7	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO202	GPIO	I/O							
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB16	AF17	AC17
		A1	PCSB0	DSPI B peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO203	GPIO	I/O							
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA15	AE17	AF18
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO204	GPIO	I/O							
432	EMIOS26_PCSB2_ GPIO432	P	EMIOS26	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y16	AD17	AE18
		A1	PCSB2	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO432	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB11
		A1	D_ADD_DAT21	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO268	GPIO	I/O							
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD10
		A1	D_ADD_DAT22	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO269	GPIO	I/O							
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE10
		A1	D_ADD_DAT23	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO270	GPIO	I/O							
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF10
		A1	D_ADD_DAT24	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO271	GPIO	I/O							
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD11
		A1	D_ADD_DAT25	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO272	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO288	GPIO	I/O							
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO289	GPIO	I/O							
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO290	GPIO	I/O							
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO291	GPIO	I/O							
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO292	GPIO	I/O							