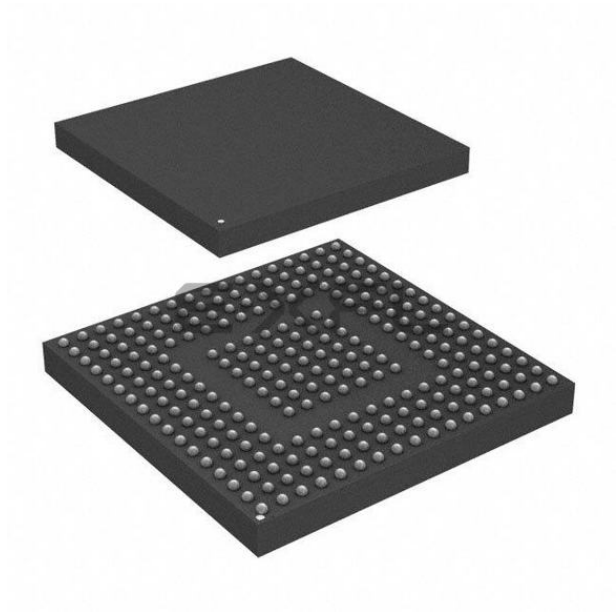

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Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kavmm2

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

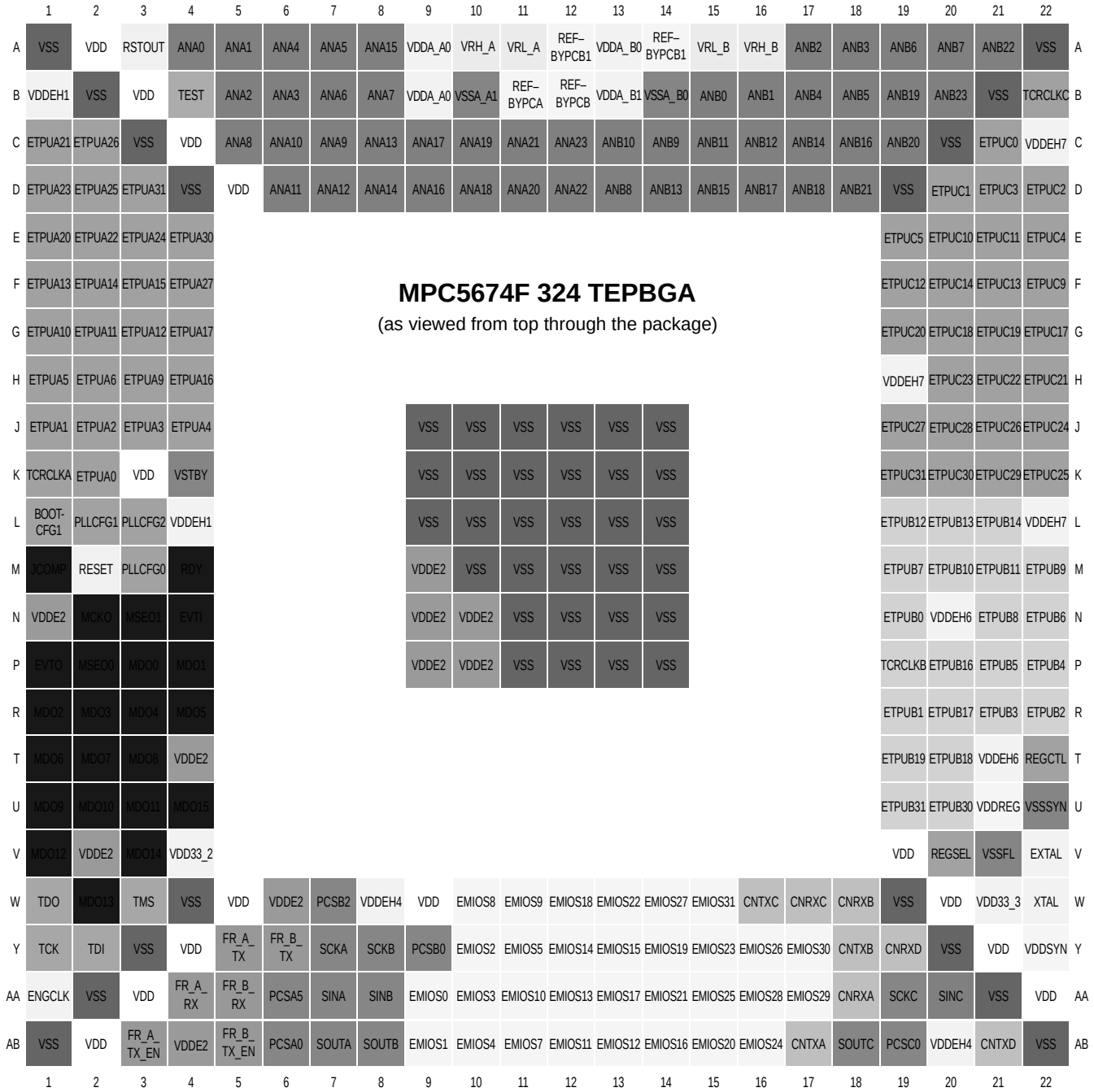


Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

MPC5674F 516-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V									ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W								ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y									ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	VDD33_4		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDD33_3	ETPUB28	VDDREG	VSSSYN	AA
AB	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSSFL	EXTAL	AB
AC	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 15. MPC5674F 516-ball TEPBGA (4 of 4)

3.4 Signal Properties and Muxing

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.freescale.com and perform a keyword search for “radiated emissions.” The following tables list the values of the device's radiated emissions operating behaviors.

Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	26	dBµV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	24	dBµV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 12 and Table 13.

Table 12. Power Sequence Pin States for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 13. Power Sequence Pin States for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs Disabled
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs Disabled
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

1 The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

4.6.1 Power-Up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

Table 20. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

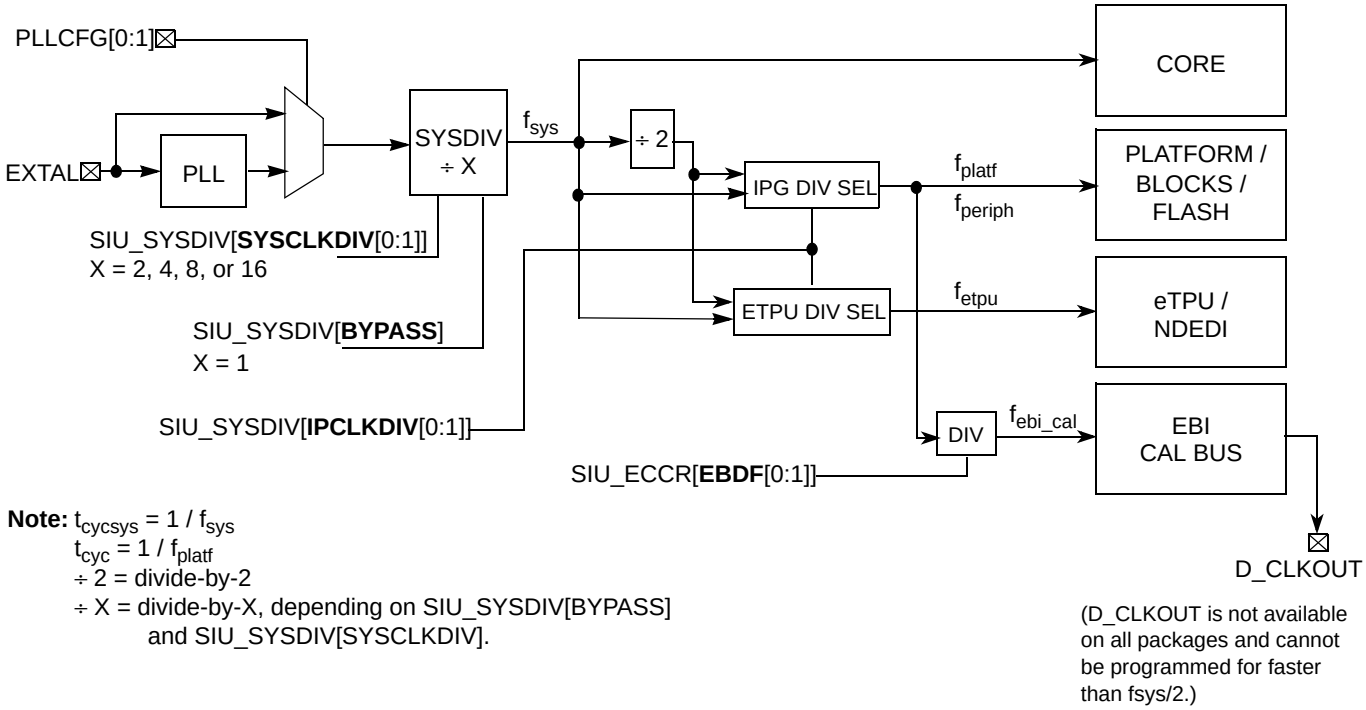
4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.



Note: $t_{cycsys} = 1 / f_{sys}$
$t_{cyc} = 1 / f_{platf}$
÷ 2 = divide-by-2
÷ X = divide-by-X, depending on SIU_SYSDIV[BYPASS] and SIU_SYSDIV[SYSCLKDIV].

(D_CLKOUT is not available on all packages and cannot be programmed for faster than fsys/2.)

Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

4.12.5 External Bus Interface (EBI) Timing

Table 36. Bus Operation Timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	7.0/7.5	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 7.0 ns EBTS = 1: 7.5 ns

4.12.6 External Interrupt Timing (IRQ Pin)

Table 37. External Interrupt Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

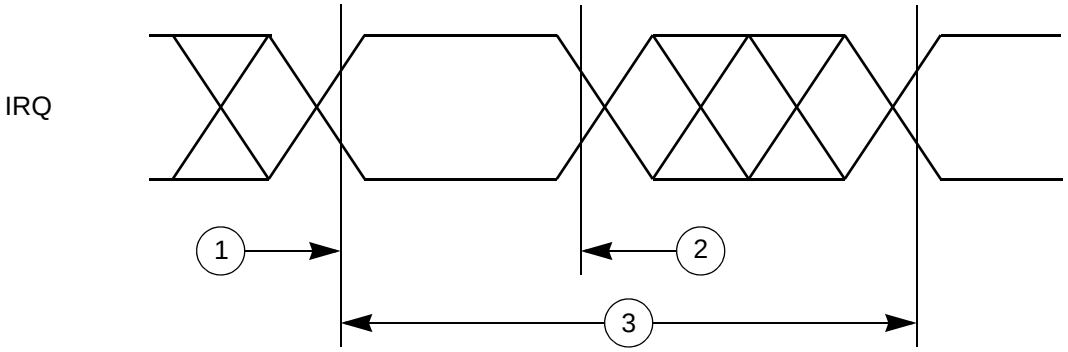


Figure 31. External Interrupt Timing

4.12.7 eTPU Timing

Table 38. eTPU Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

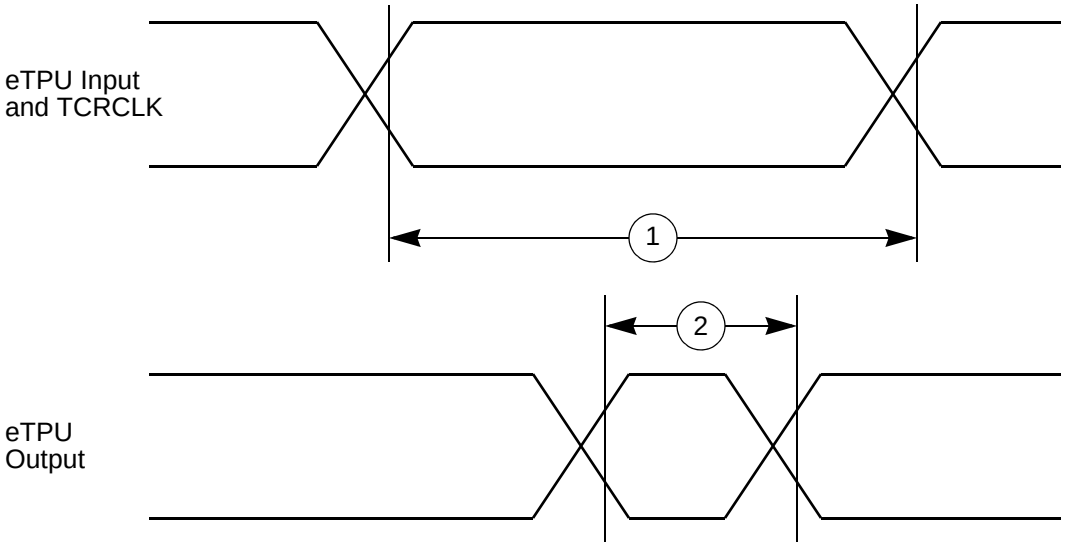


Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 39. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 44. 324 TEPBGA Package (2 of 2)

Figure 48. 516 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	E1	E1
		A1	IRQ11	External interrupt request	I							
		A2	—	—	—							
		G	GPIO137	GPIO	I/O							
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E2	E2
		A1	IRQ12	External interrupt request	I							
		A2	—	—	—							
		G	GPIO138	GPIO	I/O							
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	E3	E3
		A1	IRQ13	External interrupt request	I							
		A2	—	—	—							
		G	GPIO139	GPIO	I/O							
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	E4	E4
		A1	IRQ14	External interrupt request	I							
		A2	—	—	—							
		G	GPIO140	GPIO	I/O							
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	D1	D1
		A1	IRQ15	External interrupt request	I							
		A2	—	—	—							
		G	GPIO141	GPIO	I/O							
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO142	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V26	W24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO167	GPIO	I/O							
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V25	V22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO168	GPIO	I/O							
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	V24	V23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO169	GPIO	I/O							
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W26	U21
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO170	GPIO	I/O							
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W25	Y25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO171	GPIO	I/O							
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	W24	W21
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO172	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
458	ETPUC17_FR_A_RX_ GPIO458[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G22	H25	H23
		A1	FR_A_RX	FlexRay A receive	I							
		A2	—	—	—							
		G	GPIO458	GPIO	I/O							
459	ETPUC18_FR_A_TX_EN_ GPIO459[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G20	H26	H24
		A1	FR_A_TX_EN	FlexRay A transfer enable	O							
		A2	—	—	—							
		G	GPIO459	GPIO	I/O							
460	ETPUC19_TXDA_ GPIO460[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G21	J23	H21
		A1	TXDA	eSCI A transmit	O							
		A2	—	—	—							
		G	GPIO460	GPIO	I/O							
461	ETPUC20_RXDA _ GPIO461[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G19	J24	H25
		A1	RXDA	eSCI A receive	I							
		A2	—	—	—							
		G	GPIO461	GPIO	I/O							
462	ETPUC21_TXDB_ GPIO462[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H22	J25	H26
		A1	TXDB	eSCI B transmit	O							
		A2	—	—	—							
		G	GPIO462	GPIO	I/O							
463	ETPUC22_RXDB_ GPIO463[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H21	J26	J22
		A1	RXDB	eSCI B receive	I							
		A2	—	—	—							
		G	GPIO463	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA10	AE11	AE13
		A1	ETPUA3	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO182	GPIO	I/O							
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB10	AF11	AF13
		A1	ETPUA4	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO183	GPIO	I/O							
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y11	AD12	AF14
		A1	ETPUA5	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO184	GPIO	I/O							
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	—	AE12	AE14
		A1	ETPUA6	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO185	GPIO	I/O							
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB11	AF12	AD14
		A1	ETPUA7	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO186	GPIO	I/O							
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W10	AC13	AC14
		A1	ETPUA8	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO187	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
293	D_ADD_DAT15_GPIO293	P	D_ADD_DAT15	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	K26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO293	GPIO	I/O							
294	D_RD_WR_GPIO294	P	D_RD_WR	EBI read/write	O	F	V_{DDE10}	—/Up	—/Up	—	—	R26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO294	GPIO	I/O							
295	D_WE0_GPIO295	P	D_WE0	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	N1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO295	GPIO	I/O							
296	D_WE1_GPIO296	P	D_WE1	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	—	P5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO296	GPIO	I/O							
297	D_OE_GPIO297	P	D_OE	EBI output enable	O	F	V_{DDE10}	—/Up	—/Up	—	—	P23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO297	GPIO	I/O							
298	D_TS_GPIO298	P	D_TS	EBI transfer start	O	F	V_{DDE9}	—/Up	—/Up	—	—	AE9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO298	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
220	MDO0_GPIO220 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO0[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	MDO0/Low	P3	U3	V3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO220	GPIO	I/O							
221	MDO1_GPIO221 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO1[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	P4	U4	W6
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO221	GPIO	I/O							
222	MDO2_GPIO222 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO2[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	R1	V1	V4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO222	GPIO	I/O							
223	MDO3_GPIO223 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO3[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	R2	V2	V5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO223	GPIO	I/O							
75	MDO4_GPIO75 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO4[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	R3	V3	W1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO75	GPIO	I/O							
76	MDO5_GPIO76 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO5[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	R4	V4	W2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO76	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	VSSSYN	U22	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	VSTBY	K4	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	REGSEL	V20	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	REGCTL	T22	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	VSSFL	V21	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	VDDREG	U21	AA25	AA25

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO . This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

9 This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU_C.

10 During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

11 NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.