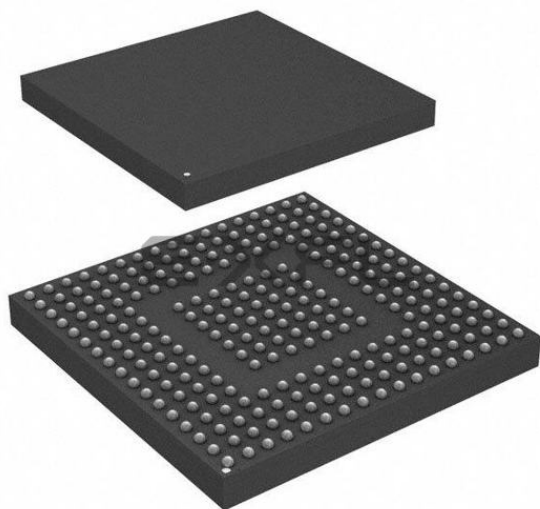




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                             |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                      |
| Core Processor             | e200z7d                                                                                                                                                     |
| Core Size                  | 32-Bit Dual-Core                                                                                                                                            |
| Speed                      | 180MHz                                                                                                                                                      |
| Connectivity               | CANbus, EBI/EMI, Ethernet, FlexRay, I <sup>2</sup> C, LINbus, SPI                                                                                           |
| Peripherals                | DMA, POR, PWM, WDT                                                                                                                                          |
| Number of I/O              | -                                                                                                                                                           |
| Program Memory Size        | 1.5MB (1.5M x 8)                                                                                                                                            |
| Program Memory Type        | FLASH                                                                                                                                                       |
| EEPROM Size                | 64K x 8                                                                                                                                                     |
| RAM Size                   | 384K x 8                                                                                                                                                    |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 5.5V                                                                                                                                                |
| Data Converters            | A/D 22x12b                                                                                                                                                  |
| Oscillator Type            | Internal                                                                                                                                                    |
| Operating Temperature      | -40°C ~ 105°C (TA)                                                                                                                                          |
| Mounting Type              | Surface Mount                                                                                                                                               |
| Package / Case             | 257-LFBGA                                                                                                                                                   |
| Supplier Device Package    | 257-LFBGA (14x14)                                                                                                                                           |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kavmm2r">https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kavmm2r</a> |

## 3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

|    | 1       | 2         | 3          | 4          | 5       | 6     | 7     | 8     | 9       | 10         | 11        | 12     | 13      | 14      | 15      | 16      | 17         | 18        | 19    | 20    | 21     | 22     | 23      | 24      | 25      | 26      |    |
|----|---------|-----------|------------|------------|---------|-------|-------|-------|---------|------------|-----------|--------|---------|---------|---------|---------|------------|-----------|-------|-------|--------|--------|---------|---------|---------|---------|----|
| A  | VSS     | VDD       | RSTOUT     | ANA0       | ANA4    | ANA8  | ANA11 | ANA15 | VDDA_A0 | REF-BYPCA1 | VRL_A     | VRH_A  | AN28    | AN32    | AN36    | VDDA_B0 | REF-BYPCB1 | VRL_B     | VRH_B | ANB7  | ANB11  | ANB14  | ANB17   | ANB21   | ANB23   | VSS     | A  |
| B  | VDDEH1  | VSS       | VDD        | TEST       | ANA1    | ANA5  | ANA10 | ANA14 | VDDA_A1 | VSSA_A1    | REF-BYPCA | AN24   | AN27    | AN29    | AN33    | VDDA_B1 | VSSA_B0    | REF-BYPCB | ANB6  | ANB8  | ANB10  | ANB15  | ANB18   | ANB22   | VSS     | TCRCLK  | B  |
| C  | ETPUA30 | ETPUA31   | VSS        | VDD        | ANA2    | ANA6  | ANA9  | ANA13 | ANA17   | ANA19      | ANA21     | ANA23  | AN26    | AN30    | AN34    | AN37    | AN38       | ANB0      | ANB4  | ANB5  | ANB12  | ANB16  | ANB19   | VSS     | ETPUC0  | ETPUC1  | C  |
| D  | ETPUA27 | ETPUA28   | ETPUA29    | VSS        | VDD     | ANA3  | ANA7  | ANA12 | ANA16   | ANA18      | ANA20     | ANA22  | AN25    | AN31    | AN35    | AN39    | ANB1       | ANB2      | ANB3  | ANB9  | ANB13  | ANB20  | VSS     | VDDEH7  | ETPUC2  | ETPUC3  | D  |
| E  | ETPUA23 | ETPUA24   | ETPUA25    | ETPUA26    |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | VDDEH7  | ETPUC4  | ETPUC5  | ETPUC6  | E  |
| F  | ETPUA19 | ETPUA20   | ETPUA21    | ETPUA22    |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC7  | ETPUC8  | ETPUC9  | ETPUC10 | F  |
| G  | ETPUA15 | ETPUA16   | ETPUA17    | ETPUA18    |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC11 | ETPUC12 | ETPUC13 | ETPUC14 | G  |
| H  | ETPUA11 | ETPUA12   | ETPUA14    | ETPUA13    |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC15 | ETPUC16 | ETPUC17 | ETPUC18 | H  |
| J  | ETPUA7  | ETPUA8    | ETPUA9     | ETPUA10    |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC19 | ETPUC20 | ETPUC21 | ETPUC22 | J  |
| K  | ETPUA3  | ETPUA4    | ETPUA5     | ETPUA6     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC23 | ETPUC24 | ETPUC25 | ETPUC26 | K  |
| L  | TCRCLKA | ETPUA0    | ETPUA1     | ETPUA2     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC27 | ETPUC28 | ETPUC29 | ETPUC30 | L  |
| M  | VDD33_1 | TXDA      | RXDA       | VSTBY      |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUC31 | ETPUB15 | ETPUB14 | VDDEH7  | M  |
| N  | RXDB    | BOOT-CFG1 | WKPCFG     | VDD        |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | VDDEH6  | ETPUB11 | ETPUB12 | ETPUB13 | N  |
| P  | TXDB    | PLLCFG1   | PLLCFG2    | VDDEH1     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUB7  | ETPUB8  | ETPUB9  | ETPUB10 | P  |
| R  | VDDE2   | RESET     | PLLCFG0    | BDV        |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUB3  | ETPUB4  | ETPUB5  | ETPUB6  | R  |
| T  | VDDE2   | MDIO0     | MDIO1      | MDIO2      |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | TCRCLKB | ETPUB0  | ETPUB1  | ETPUB2  | T  |
| U  | MDIO3   | MDIO4     | MDIO5      | MDIO6      |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUB19 | ETPUB18 | ETPUB17 | ETPUB16 | U  |
| V  | MDIO7   | MDIO8     | MDIO9      | MDIO10     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUB26 | ETPUB22 | ETPUB21 | ETPUB20 | V  |
| W  | MDIO11  | MDIO12    | MDIO13     | MDIO14     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | REGSEL  | ETPUB25 | ETPUB24 | ETPUB23 | W  |
| Y  | MDIO15  | MDIO16    | MDIO17     | MDIO18     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | ETPUB29 | ETPUB28 | ETPUB27 | REGCTL  | Y  |
| AA | MDIO19  | MDIO20    | MDIO21     | MDIO22     |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | VDD33_3 | ETPUB30 | VDDREG  | VSSSYN  | AA |
| AB | TDO     | TCK       | TMS        | VDD        |         |       |       |       |         |            |           |        |         |         |         |         |            |           |       |       |        |        | VDD     | ETPUB31 | VSSFL   | EXTAL   | AB |
| AC | VDDE2   | TDI       | VDD        | VSS        | VDDE2   | PCSA1 | PCSA2 | PCSB4 | PCSB1   | VDDEH3     | VDDEH4    | VDD    | EMIOS8  | EMIOS14 | EMIOS18 | EMIOS22 | EMIOS27    | EMIOS31   | CNRXB | CNRXD | VDDEH5 | PCSC1  | VSS     | VDD     | VDDEH6  | XTAL    | AC |
| AD | ENGCLK  | VDD       | VSS        | FR_A_TX    | FR_B_TX | PCSA5 | SOUTA | SCKA  | PCSB0   | PCSB3      | EMIOS2    | EMIOS5 | EMIOS9  | EMIOS15 | EMIOS19 | EMIOS23 | EMIOS26    | EMIOS30   | CNTXB | CNTXD | SCKC   | RXDC   | PCSC3   | VSS     | VDD     | VDDSYN  | AD |
| AE | VDD     | VSS       | FR_A_RX    | FR_B_RX    | PCSA4   | PCSA0 | PCSA3 | SCKB  | SINB    | EMIOS0     | EMIOS3    | EMIOS6 | EMIOS10 | EMIOS13 | EMIOS17 | EMIOS21 | EMIOS25    | EMIOS29   | CNRXA | CNRXC | PCSC0  | SINC   | PCSC2   | PCSC5   | VSS     | VDD     | AE |
| AF | VSS     | VDDE2     | FR_A_TX_EN | FR_B_TX_EN | VDDEH3  | PCSB5 | SINA  | PCSB2 | SOUTB   | EMIOS1     | EMIOS4    | EMIOS7 | EMIOS11 | EMIOS12 | EMIOS16 | EMIOS20 | EMIOS24    | EMIOS28   | CNTXA | CNTXC | SOUTC  | VDDEH4 | TXDC    | PCSC4   | VDDEH5  | VSS     | AF |
|    | 1       | 2         | 3          | 4          | 5       | 6     | 7     | 8     | 9       | 10         | 11        | 12     | 13      | 14      | 15      | 16      | 17         | 18        | 19    | 20    | 21     | 22     | 23      | 24      | 25      | 26      |    |

**MPC5674F 416-ball TEPBGA**  
(as viewed from top through the package)

|       |       |       |     |     |     |     |     |
|-------|-------|-------|-----|-----|-----|-----|-----|
| VSS   | VSS   | VSS   | VSS | VSS | VSS | VSS | VSS |
| VSS   | VSS   | VSS   | VSS | VSS | VSS | VSS | VSS |
| VSS   | VSS   | VSS   | VSS | VSS | VSS | VSS | VSS |
| VDDE2 | VSS   | VSS   | VSS | VSS | VSS | VSS | VSS |
| VDDE2 | VDDE2 | VSS   | VSS | VSS | VSS | VSS | VSS |
| VDDE2 | VDDE2 | VSS   | VSS | VSS | VSS | VSS | VSS |
| VDDE2 | VDDE2 | VDDE2 | VSS | VSS | VSS | VSS | VSS |
| VDDE2 | VDDE2 | VDDE2 | VSS | VSS | VSS | VSS | VSS |

**Figure 6. MPC5674F 416-ball TEPBGA (full diagram)**

- <sup>1</sup> Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
- <sup>2</sup> 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.
- <sup>3</sup> 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.
- <sup>4</sup> Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
- <sup>5</sup> 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.
- <sup>6</sup> MPC5674F has two analog power supply pins on the pinout: VDDA\_A and VDDA\_B.
- <sup>7</sup> MPC5674F has two analog ground supply pins on the pinout: VSSA\_A and VSSA\_B.
- <sup>8</sup> MPC5674F has two analog low reference voltage pins on the pinout: VRL\_A and VRL\_B.
- <sup>9</sup> MPC5674F has two analog high reference voltage pins on the pinout: VRH\_A and VRH\_B.
- <sup>10</sup> Total injection current for all pins must not exceed 25 mA at maximum operating voltage.
- <sup>11</sup> Injection current of  $\pm 5$  mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or  $V_{DDEH}$  supply when under this stress condition.
- <sup>12</sup> Total injection current for all analog input pins must not exceed 15 mA.
- <sup>13</sup> Lifetime operation at these specification limits is not guaranteed.
- <sup>14</sup> Solder profile per CDF-AEC-Q100.
- <sup>15</sup> Moisture sensitivity per JEDEC test method A112.

## 4.2 Thermal Characteristics

**Table 4. Thermal Characteristics, 416-pin TEPBGA Package<sup>1</sup>**

| Characteristic                                                                | Symbol           | Value | Unit |
|-------------------------------------------------------------------------------|------------------|-------|------|
| Junction to Ambient <sup>2,3</sup> Natural Convection (Single layer board)    | $R_{\theta JA}$  | 24    | °C/W |
| Junction to Ambient <sup>2,4</sup> Natural Convection (Four layer board 2s2p) | $R_{\theta JA}$  | 18    | °C/W |
| Junction to Ambient (@200 ft./min., Single layer board)                       | $R_{\theta JMA}$ | 19    | °C/W |
| Junction to Ambient (@200 ft./min., Four layer board 2s2p)                    | $R_{\theta JMA}$ | 14    | °C/W |
| Junction to Board <sup>5</sup>                                                | $R_{\theta JB}$  | 9     | °C/W |
| Junction to Case <sup>6</sup>                                                 | $R_{\theta JC}$  | 6     | °C/W |
| Junction to Package Top <sup>7</sup> Natural Convection                       | $\Psi_{JT}$      | 2     | °C/W |

- <sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.
- <sup>2</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>3</sup> Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- <sup>4</sup> Per JEDEC JESD51-6 with the board horizontal.
- <sup>5</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>6</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>7</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

- <sup>6</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>7</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

## 4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature,  $T_J$ , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \text{Eqn. 1}$$

where:

$T_A$  = ambient temperature for the package ( $^{\circ}\text{C}$ )

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 2}$$

where:

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  = junction to case thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta CA}$  = case to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} * P_D) \quad \text{Eqn. 3}$$

where:

$T_T$  = thermocouple temperature on top of the package ( $^{\circ}\text{C}$ )

$\Psi_{JT}$  = thermal characterization parameter ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

## Electrical Characteristics

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### References:

Semiconductor Equipment and Materials International  
3081 Zanker Road  
San Jose, CA 95134  
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

- C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

## 4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for "radiated emissions." The following tables list the values of the device's radiated emissions operating behaviors.

**Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA**

| Symbol        | Description                                           | Conditions                                                                                                                                                                  | $f_{osc}$<br>$f_{sys}$                                          | Frequency band (MHz) | Level (max.) | Unit       | Notes |
|---------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|----------------------|--------------|------------|-------|
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>416 BGA<br>EBI off<br>CLK on<br>FM off              | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 26           | dB $\mu$ V | 1     |
|               |                                                       |                                                                                                                                                                             |                                                                 | 50–150               | 30           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 150–500              | 34           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 500–1000             | 30           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | IEC and SAE level    | $I^2$        | —          | 1, 3  |
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>416 BGA<br>EBI off<br>CLK off<br>FM on <sup>4</sup> | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 24           | dB $\mu$ V | 1     |
|               |                                                       |                                                                                                                                                                             |                                                                 | 50–150               | 25           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 150–500              | 25           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 500–1000             | 21           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | IEC and SAE level    | $K^5$        | —          | 1, 3  |

<sup>1</sup> Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>2</sup>  $I = 36\text{ dB}\mu\text{V}$

<sup>3</sup> Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>4</sup> “FM on” = FM depth of  $\pm 2\%$

<sup>5</sup> K = 30 dB $\mu$ V

**Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA**

| Symbol        | Description                                           | Conditions                                                                                                                                                              | $f_{osc}$<br>$f_{sys}$                                          | Frequency band (MHz) | Level (max.)   | Unit       | Notes           |
|---------------|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|----------------------|----------------|------------|-----------------|
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^\circ\text{C}$<br>516 BGA<br>EBI on<br>CLK on<br>FM off             | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 40             | dB $\mu$ V | <sup>1</sup>    |
|               |                                                       |                                                                                                                                                                         |                                                                 | 50–150               | 48             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | 150–500              | 48             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | 500–1000             | 47             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | IEC and SAE level    | G <sup>2</sup> | —          | <sup>1, 3</sup> |
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^\circ\text{C}$<br>516 BGA<br>EBI on<br>CLK on<br>FM on <sup>4</sup> | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 40             | dB $\mu$ V | <sup>1</sup>    |
|               |                                                       |                                                                                                                                                                         |                                                                 | 50–150               | 44             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | 150–500              | 41             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | 500–1000             | 36             |            |                 |
|               |                                                       |                                                                                                                                                                         |                                                                 | IEC and SAE level    | G <sup>2</sup> | —          | <sup>1, 3</sup> |

<sup>1</sup> Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>2</sup> G = 48 dB $\mu$ V

<sup>3</sup> Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>4</sup> “FM on” = FM depth of  $\pm 2\%$

## 4.4 ESD Characteristics

**Table 9. ESD Ratings<sup>1,2</sup>**

| Spec | Characteristic                     | Symbol    | Value                        | Unit |
|------|------------------------------------|-----------|------------------------------|------|
| 1    | ESD for Human Body Model (HBM)     | $V_{HBM}$ | 2000                         | V    |
| 2    | ESD for Charged Device Model (CDM) | $V_{CDM}$ | 750 (corners)<br>500 (other) | V    |

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 4.5 PMC/POR/LVI Electrical Specifications

**Note:** For ADC internal resource measurements, see Table 21 in Section 4.9.1, “ADC Internal Resource Measurements.”

**Table 20. eQADC Conversion Specifications (Operating) (continued)**

| Spec | Characteristic                                                                                                                                                          | Symbol                                                              | Min                                            | Max                                                                                                                        | Unit        |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------|
| 9    | Offset Error without Calibration                                                                                                                                        | OFFNC                                                               | 0 <sup>4</sup>                                 | 100 <sup>4</sup>                                                                                                           | LSB         |
| 10   | Offset Error with Calibration                                                                                                                                           | OFFWC                                                               | -4 <sup>4</sup>                                | 4 <sup>4</sup>                                                                                                             | LSB         |
| 11   | Full Scale Gain Error without Calibration                                                                                                                               | GAINNC                                                              | -120 <sup>4</sup>                              | 0 <sup>4</sup>                                                                                                             | LSB         |
| 12   | Full Scale Gain Error with Calibration                                                                                                                                  | GAINWC                                                              | -4 <sup>4,6</sup>                              | 4 <sup>4,6</sup>                                                                                                           | LSB         |
| 13   | Non-Disruptive Input Injection Current <sup>7, 8, 9, 10</sup>                                                                                                           | I <sub>INJ</sub>                                                    | -3                                             | 3                                                                                                                          | mA          |
| 14   | Incremental Error due to injection current <sup>11, 12</sup>                                                                                                            | E <sub>INJ</sub>                                                    | -4 <sup>4</sup>                                | 4 <sup>4</sup>                                                                                                             | Counts      |
| 15   | TUE value at 8 MHz <sup>13, 14</sup> (with calibration)                                                                                                                 | TUE8                                                                | -4 <sup>4,6</sup>                              | 4 <sup>4,6</sup>                                                                                                           | Counts      |
| 16   | TUE value at 16 MHz <sup>13, 14</sup> (with calibration)                                                                                                                | TUE16                                                               | -8                                             | 8                                                                                                                          | Counts      |
| 17   | Maximum differential voltage <sup>15</sup><br>(DANx+ - DANx-) or (DANx- - DANx+)<br>PREGAIN set to 1X setting<br>PREGAIN set to 2X setting<br>PREGAIN set to 4X setting | DIFF <sub>max</sub><br>DIFF <sub>max2</sub><br>DIFF <sub>max4</sub> | —<br>—<br>—                                    | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>(V <sub>RH</sub> - V <sub>RL</sub> )/4<br>(V <sub>RH</sub> - V <sub>RL</sub> )/8 | V<br>V<br>V |
| 18   | Differential input Common mode voltage <sup>15</sup><br>(DANx- + DANx+)/2                                                                                               | DIFF <sub>cmv</sub>                                                 | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>- 5% | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>+ 5%                                                                             | V           |

<sup>1</sup> Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

<sup>2</sup> At V<sub>RH</sub> - V<sub>RL</sub> = 5.12 V, one count = 1.25 mV without using pregain.

<sup>3</sup> INL and DNL are tested from V<sub>RL</sub> + 50 LSB to V<sub>RH</sub> - 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

<sup>4</sup> New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

<sup>5</sup> At V<sub>RH</sub> - V<sub>RL</sub> = 5.12 V, one LSB = 1.25 mV.

<sup>6</sup> The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

<sup>7</sup> Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than V<sub>RH</sub> and \$000 for values less than V<sub>RL</sub>. Other channels are not affected by non-disruptive conditions.

<sup>8</sup> Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

<sup>9</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using V<sub>POSCLAMP</sub> = V<sub>DDA</sub> + 0.5 V and V<sub>NEGCLAMP</sub> = -0.3 V, then use the larger of the calculated values.

<sup>10</sup> Condition applies to two adjacent pins at injection limits.

<sup>11</sup> Performance expected with production silicon.

<sup>12</sup> All channels have same 10 kΩ < R<sub>s</sub> < 100 kΩ Channel under test has R<sub>s</sub> = 10 kΩ, I<sub>INJ</sub> = I<sub>INJMAX</sub> · I<sub>INJMIN</sub>.

<sup>13</sup> The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

<sup>14</sup> TUE does not apply to differential conversions.

<sup>15</sup> Voltages between V<sub>RL</sub> and V<sub>RH</sub> will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

## 4.11.2 Pad AC Specifications

Table 31. Pad AC Specifications ( $V_{DDEH} = 5.0\text{ V}$ ,  $V_{DDE} = 3.3\text{ V}$ )<sup>1</sup>

| Spec | Pad                       | SRC/DSC | Out Delay <sup>2,4</sup><br>L → H/H → L (ns) | Rise/Fall <sup>3,4</sup><br>(ns) | Load Drive<br>(pF) |
|------|---------------------------|---------|----------------------------------------------|----------------------------------|--------------------|
| 1    | Medium <sup>5</sup>       | 00      | 152/165                                      | 70/74                            | 50                 |
| 2    |                           |         | 205/220                                      | 96/96                            | 200                |
| 3    |                           | 01      | 28/34                                        | 12/15                            | 50                 |
| 4    |                           |         | 52/59                                        | 28/31                            | 200                |
| 5    |                           | 11      | 12/12                                        | 5.3/5.9                          | 50                 |
| 6    |                           |         | 32/32                                        | 22/22                            | 200                |
| 7    | Fast <sup>6</sup>         | 00      | 2.5                                          | 1.2                              | 10                 |
| 8    |                           | 01      |                                              |                                  | 20                 |
| 9    |                           | 10      |                                              |                                  | 30                 |
| 10   |                           | 11      |                                              |                                  | 50                 |
| 11   | Fast with Slew Rate       | 00      | 40/40                                        | 16/16                            | 50                 |
| 12   |                           |         | 50/50                                        | 21/21                            | 200                |
| 13   |                           | 01      | 13/13                                        | 5/5                              | 50                 |
| 14   |                           |         | 19/19                                        | 8/8                              | 200                |
| 15   |                           | 10      | 8/8                                          | 2.4/2.4                          | 50                 |
| 16   |                           |         | 12/12                                        | 5/5                              | 200                |
| 17   |                           | 11      | 5/5                                          | 1.1/1/1                          | 50                 |
| 18   |                           |         | 8/8                                          | 2.6                              | 2.6                |
| 19   | Pull Up/Down (3.6 V max)  | —       | —                                            | 7500                             | 50                 |
| 20   | Pull Up/Down (5.25 V max) | —       | 6000                                         | 5000/5000                        | 50                 |

<sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at  $V_{DD} = 1.02\text{ V}$  to  $1.32\text{ V}$ ,  $V_{DDE} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{DDEH} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = T_L$  to  $T_H$ .

<sup>2</sup> This parameter is supplied for reference and is not guaranteed by design and not tested.

<sup>3</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.

<sup>4</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.

<sup>5</sup> Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

<sup>6</sup> Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

## Electrical Characteristics

<sup>1</sup> JTAG timing specified at  $V_{DD} = 1.08 \text{ V to } 1.32 \text{ V}$ ,  $V_{DDE} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ , and  $C_L = 30 \text{ pF}$  with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 35 for functional specifications.

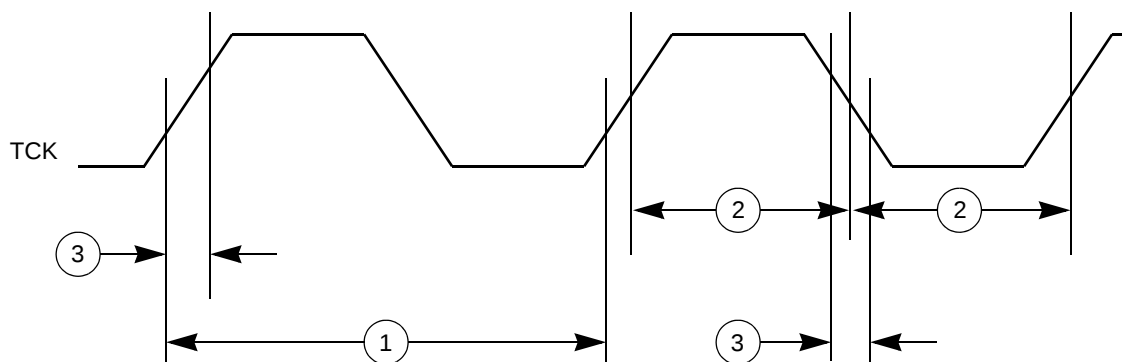


Figure 21. JTAG Test Clock Input Timing

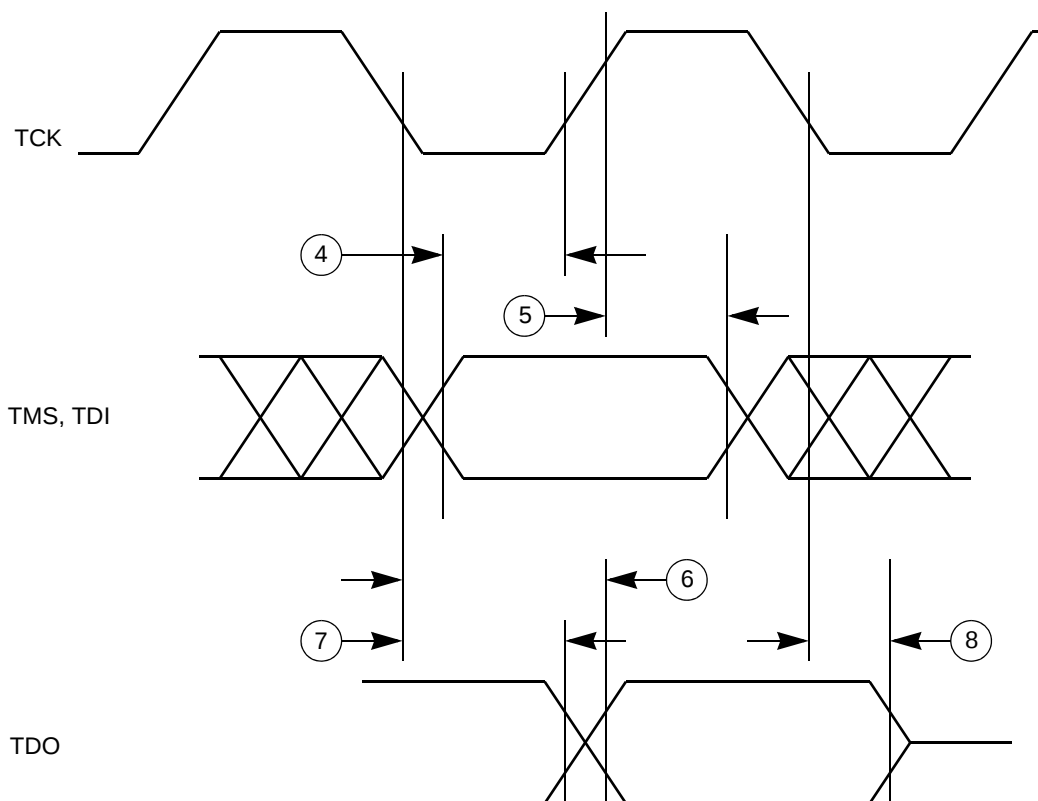


Figure 22. JTAG Test Access Port Timing

Table 40. DSPI Timing<sup>1 2</sup> (continued)

| Spec | Characteristic                           | Symbol    | Peripheral Bus Freq: 132 MHz |     | Unit |
|------|------------------------------------------|-----------|------------------------------|-----|------|
|      |                                          |           | Min                          | Max |      |
| 9    | Data Setup Time for Inputs               | $t_{SUI}$ |                              |     |      |
|      | Master (MTFE = 0)                        |           | 20                           | —   | ns   |
|      | Slave                                    |           | 4                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>8</sup> |           | 6                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | 20                           | —   | ns   |
| 10   | Data Hold Time for Inputs                | $t_{HI}$  |                              |     |      |
|      | Master (MTFE = 0)                        |           | −3                           | —   | ns   |
|      | Slave                                    |           | 7                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>8</sup> |           | 12                           | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | −3                           | —   | ns   |
| 11   | Data Valid (after SCK edge)              | $t_{SUO}$ |                              |     |      |
|      | Master (MTFE = 0)                        |           | —                            | 5   | ns   |
|      | Slave                                    |           | —                            | 25  | ns   |
|      | Master (MTFE = 1, CPHA = 0)              |           | —                            | 13  | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | —                            | 5   | ns   |
| 12   | Data Hold Time for Outputs               | $t_{HO}$  |                              |     |      |
|      | Master (MTFE = 0)                        |           | −5                           | —   | ns   |
|      | Slave                                    |           | 2.5                          | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0)              |           | 3                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | −5                           | —   | ns   |

<sup>1</sup> DSPI timing specified at  $V_{DD} = 1.08 \text{ V}$  to  $1.32 \text{ V}$ ,  $V_{DDEH} = 3.0 \text{ V}$  to  $5.5 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ , and  $T_A = T_L$  to  $T_H$

<sup>2</sup> Speed is the nominal maximum frequency of platform clock ( $f_{platt}$ ). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock ( $f_{sys}$ ) + 2% FM.

<sup>3</sup> The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

<sup>4</sup> The actual minimum SCK cycle time is limited by pad performance.

<sup>5</sup> The maximum value is programmable in DSPI\_CTAR $n$ [PSSCK] and DSPI\_CTAR $n$ [CSSCK].

<sup>6</sup> The maximum value is programmable in DSPI\_CTAR $n$ [PASC] and DSPI\_CTAR $n$ [ASC].

<sup>7</sup> For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

<sup>8</sup> This number is calculated assuming the SMPL\_PT bitfield in DSPI\_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 41. DSPI LVDS Timing<sup>1, 2</sup>

| Characteristic                         | Symbol                | Min                     | Max                     | Unit |
|----------------------------------------|-----------------------|-------------------------|-------------------------|------|
| LVDS Clock to Data/Chip Select Outputs | $t_{LVDS\text{DATA}}$ | $-0.25 \times t_{SCYC}$ | $+0.25 \times t_{SCYC}$ | ns   |

<sup>1</sup> These are typical values that are estimated from simulation.

<sup>2</sup> See DSPI LVDS Pad related data in Table 17.

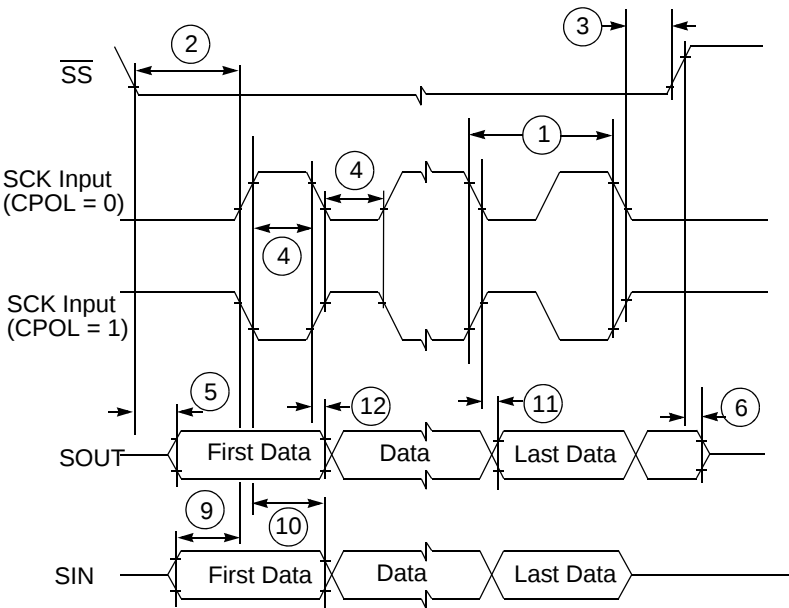


Figure 36. DSPI Classic SPI Timing — Slave, CPHA = 0

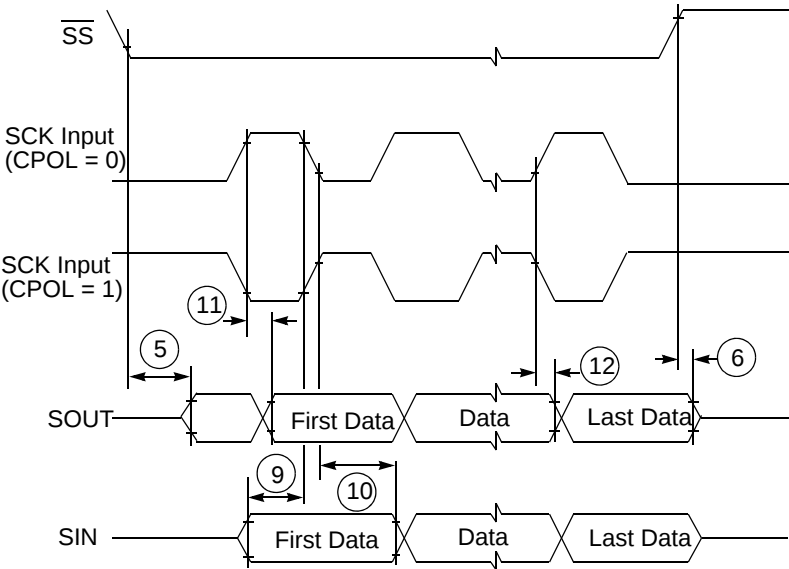


Figure 37. DSPI Classic SPI Timing — Slave, CPHA = 1

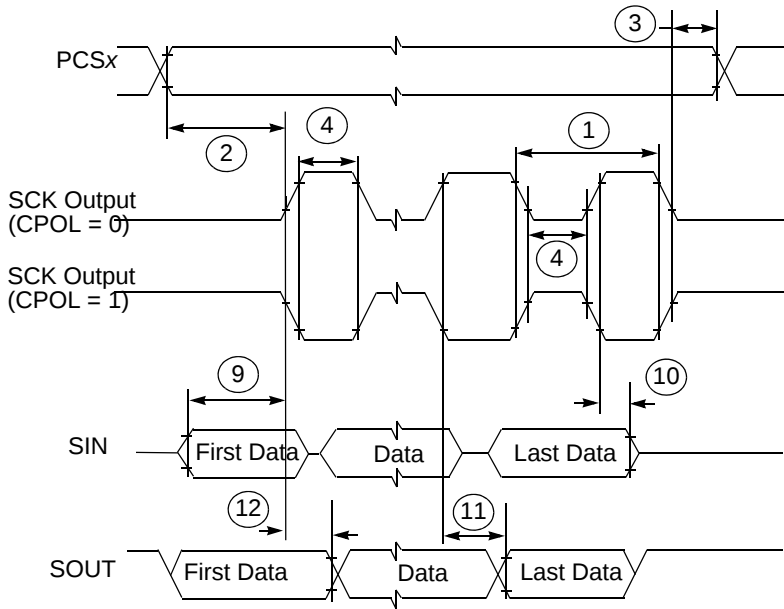


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

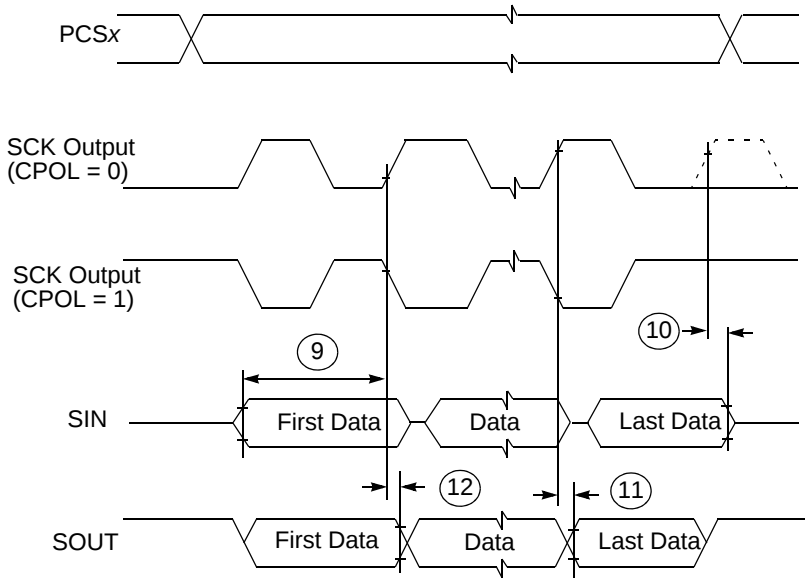


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|----------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                            |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 143                   | ETPUA29_PCSC2_<br>GPIO143  | P                  | ETPUA29               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | D3  | D3  |
|                       |                            | A1                 | PCSC2                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO143               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 144                   | ETPUA30_PCSC3_<br>GPIO144  | P                  | ETPUA30               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | E4               | C1  | C1  |
|                       |                            | A1                 | PCSC3                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO144               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 145                   | ETPUA31_PCSC4_<br>GPIO145  | P                  | ETPUA31               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | D3               | C2  | C2  |
|                       |                            | A1                 | PCSC4                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO145               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| eTPU_B                |                            |                    |                       |                               |           |                       |                      |                                 |                                |                  |     |     |
| 146                   | TCRCLKB_IRQ6_<br>GPIO146   | P                  | TCRCLKB               | eTPU B TCR clock              | I         | MH                    | V <sub>DDEH6</sub>   | —/Up                            | —/Up                           | P19              | T23 | V25 |
|                       |                            | A1                 | IRQ6                  | External interrupt request    | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO146               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 147                   | ETPUB0_ETPUB16_<br>GPIO147 | P                  | ETPUB0                | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | N19              | T24 | V26 |
|                       |                            | A1                 | ETPUB16               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO147               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 148                   | ETPUB1_ETPUB17_<br>GPIO148 | P                  | ETPUB1                | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | R19              | T25 | U22 |
|                       |                            | A1                 | ETPUB17               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO148               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|----------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                            |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 200                   | EMIOS21_ETPUB5_<br>GPIO200 | P                  | EMIOS21               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA14             | AE16 | AE17 |
|                       |                            | A1                 | ETPUB5                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO200               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 201                   | EMIOS22_ETPUB6_<br>GPIO201 | P                  | EMIOS22               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W13              | AC16 | AC16 |
|                       |                            | A1                 | ETPUB6                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO201               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 202                   | EMIOS23_ETPUB7_<br>GPIO202 | P                  | EMIOS23               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y15              | AD16 | AA16 |
|                       |                            | A1                 | ETPUB7                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO202               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 203                   | EMIOS24_PCSB0_<br>GPIO203  | P                  | EMIOS24               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB16             | AF17 | AC17 |
|                       |                            | A1                 | PCSB0                 | DSPI B peripheral chip select | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO203               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 204                   | EMIOS25_PCSB1_<br>GPIO204  | P                  | EMIOS25               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA15             | AE17 | AF18 |
|                       |                            | A1                 | PCSB1                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO204               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 432                   | EMIOS26_PCSB2_<br>GPIO432  | P                  | EMIOS26               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y16              | AD17 | AE18 |
|                       |                            | A1                 | PCSB2                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO432               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                 | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                  |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| —                     | ANB9                     | P                  | ANB9                  | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB9                            | ANB9                           | C14              | D20 | A21 |
| —                     | ANB10                    | P                  | ANB10                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB10                           | ANB10                          | C13              | B21 | B21 |
| —                     | ANB11                    | P                  | ANB11                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB11                           | ANB11                          | C15              | A21 | C21 |
| —                     | ANB12                    | P                  | ANB12                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB12                           | ANB12                          | C16              | C21 | A22 |
| —                     | ANB13                    | P                  | ANB13                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB13                           | ANB13                          | D14              | D21 | B22 |
| —                     | ANB14                    | P                  | ANB14                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB14                           | ANB14                          | C17              | A22 | D20 |
| —                     | ANB15                    | P                  | ANB15                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB15                           | ANB15                          | D15              | B22 | C22 |
| —                     | ANB16                    | P                  | ANB16                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB16                           | ANB16                          | C18              | C22 | D21 |
| —                     | ANB17                    | P                  | ANB17                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB17                           | ANB17                          | D16              | A23 | D22 |
| —                     | ANB18                    | P                  | ANB18                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB18                           | ANB18                          | D17              | B23 | A23 |
| —                     | ANB19                    | P                  | ANB19                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB19                           | ANB19                          | B19              | C23 | B23 |
| —                     | ANB20                    | P                  | ANB20                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB20                           | ANB20                          | C19              | D22 | C23 |
| —                     | ANB21                    | P                  | ANB21                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB21                           | ANB21                          | D18              | A24 | A24 |
| —                     | ANB22                    | P                  | ANB22                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB22                           | ANB22                          | A21              | B24 | B24 |
| —                     | ANB23                    | P                  | ANB23                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB23                           | ANB23                          | B20              | A25 | E20 |
| —                     | VRH_A                    | P                  | VRH_A                 | ADC A Voltage reference high     | I         | VDDINT                | V <sub>RH_A</sub>    | VRH_A                           | VRH_A                          | A10              | A12 | A12 |
| —                     | VRL_A                    | P                  | VRL_A                 | ADC A Voltage reference low      | I         | VSSINT                | V <sub>RL_A</sub>    | VRL_A                           | VRL_A                          | A11              | A11 | A11 |
| —                     | VRH_B                    | P                  | VRH_B                 | ADC B Voltage reference high     | I         | VDDINT                | V <sub>RH_B</sub>    | VRH_B                           | VRH_B                          | A16              | A19 | A19 |
| —                     | VRL_B                    | P                  | VRL_B                 | ADC B Voltage reference low      | I         | VSSINT                | V <sub>RL_B</sub>    | VRL_B                           | VRL_B                          | A15              | A18 | A18 |
| —                     | REFBYPCB                 | P                  | REFBYPCB              | ADC B Reference bypass capacitor | I         | AE                    | V <sub>DDA_B0</sub>  | REFBYPCB                        | REFBYPCB                       | B12              | B18 | B18 |
| —                     | REFBYPCA                 | P                  | REFBYPCA              | ADC A Reference bypass capacitor | I         | AE                    | V <sub>DDA_A1</sub>  | REFBYPCA                        | REFBYPCA                       | B11              | B11 | B11 |
| —                     | VDDA_A0                  | P                  | VDDA_A                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_A0</sub>  | VDDA_A0                         | VDDA_A0                        | A9               | A9  | A9  |
| —                     | VDDA_A1                  | P                  | VDDA_A                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_A1</sub>  | VDDA_A1                         | VDDA_A1                        | B9               | B9  | B9  |
| —                     | REFBYPCA1                | P                  | REFBYPCA1             | ADC A Reference bypass capacitor | I         | AE                    | V <sub>DDA_A1</sub>  | REFBYPCA1                       | REFBYPCA1                      | A12              | A10 | A10 |
| —                     | VSSA_A1                  | P                  | VSSA_A                | Ground                           | I         | VSSE                  | V <sub>SSA_A1</sub>  | VSSA_A1                         | VSSA_A1                        | B10              | B10 | B10 |
| —                     | VDDA_B0                  | P                  | VDDA_B                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_B0</sub>  | VDDA_B0                         | VDDA_B0                        | A13              | A16 | A16 |
| —                     | VDDA_B1                  | P                  | VDDA_B                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_B1</sub>  | VDDA_B1                         | VDDA_B1                        | B13              | B16 | B16 |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 88                    | CNRXC_PCSD4_GPIO88       | P                  | CNRXC                 | FlexCAN C receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | W17              | AE20 | AE20 |
|                       |                          | A1                 | PCSD4                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO88                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 246                   | CNTXD_GPIO246            | P                  | CNTXD                 | FlexCAN D transmit            | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AB21             | AD20 | AD20 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO246               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 247                   | CNRXD_GPIO247            | P                  | CNRXD                 | FlexCAN D receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | Y19              | AC20 | AC20 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO247               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| eSCI                  |                          |                    |                       |                               |           |                       |                      |                                 |                                |                  |      |      |
| 89                    | TXDA_GPIO89              | P                  | TXDA                  | eSCI A transmit               | O         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | M2   | K2   |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO89                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 90                    | RXDA_GPIO90              | P                  | RXDA                  | eSCI A receive                | I         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | M3   | K3   |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO90                | GPIO                          | I         |                       |                      |                                 |                                |                  |      |      |
| 91                    | TXDB_PCSD1_GPIO91        | P                  | TXDB                  | eSCI B transmit               | O         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | P1   | K1   |
|                       |                          | A1                 | PCSD1                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO91                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516  |
| 102                   | SCKB_<br>GPIO102         | P                  | SCKB                  | DSPI B clock                  | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | Y8               | AE8 | AC8  |
|                       |                          | A1                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO102               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 103                   | SINB_<br>GPIO103         | P                  | SINB                  | DSPI B data input             | I         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AA8              | AE9 | AB9  |
|                       |                          | A1                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO103               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 104                   | SOUTB_<br>GPIO104        | P                  | SOUTB                 | DSPI B data output            | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AB8              | AF9 | AA10 |
|                       |                          | A1                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             |           |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO104               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 105                   | PCSB0_PCSD2_<br>GPIO105  | P                  | PCSB0                 | DSPI B peripheral chip select | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | Y9               | AD9 | AF8  |
|                       |                          | A1                 | PCSD2                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO105               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 106                   | PCSB1_PCSD0_<br>GPIO106  | P                  | PCSB1                 | DSPI B peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC9 | AE8  |
|                       |                          | A1                 | PCSD0                 | DSPI D peripheral chip select | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO106               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 107                   | PCSB2_SOUTC_<br>GPIO107  | P                  | PCSB2                 | DSPI B peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | W7               | AF8 | AD8  |
|                       |                          | A1                 | SOUTC                 | DSPI C data output            | O         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO107               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>       | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------------|--------------------|-----------------------|-----------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                                |                    |                       |                                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 108                   | PCSB3_SINC_<br>GPIO108         | P                  | PCSB3                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AD10 | AC9  |
|                       |                                | A1                 | SINC                  | DSPI C data input                             | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO108               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 109                   | PCSB4_SCKC_<br>GPIO109         | P                  | PCSB4                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC8  | AF7  |
|                       |                                | A1                 | SCKC                  | DSPI C clock                                  | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO109               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 110                   | PCSB5_PCSC0_<br>GPIO110        | P                  | PCSB5                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AF6  | AE6  |
|                       |                                | A1                 | PCSC0                 | DSPI C peripheral chip select                 | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO110               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 235                   | SCKC_SCK_C_LVDSP_<br>GPIO235   | P                  | SCKC                  | DSPI C clock                                  | I/O       | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AA19             | AD21 | AD21 |
|                       |                                | A1                 | SCK_C_LVDSP           | LVDS+ downstream signal positive output clock | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO235               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 236                   | SINC_SCK_C_LVDSM_<br>GPIO236   | P                  | SINC                  | DSPI C data input                             | I         | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AA20             | AE22 | AE22 |
|                       |                                | A1                 | SCK_C_LVDSM           | LVDS– downstream signal negative output clock | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO236               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 237                   | SOUTC_SOUT_C_LVDSP_<br>GPIO237 | P                  | SOUTC                 | DSPI C data output                            | O         | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AB18             | AF21 | AF21 |
|                       |                                | A1                 | SOUT_C_LVDSP          | LVDS+ downstream signal positive output data  | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO237               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>        | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|---------------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                 |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 262                   | D_ADD15_<br>GPIO262             | P                  | D_ADD15               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | R4  |
|                       |                                 | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO262               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 263                   | D_ADD16_D_ADD_DAT16_<br>GPIO263 | P                  | D_ADD16               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | R5  |
|                       |                                 | A1                 | D_ADD_DAT16           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO263               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 264                   | D_ADD17_D_ADD_DAT17_<br>GPIO264 | P                  | D_ADD17               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T5  |
|                       |                                 | A1                 | D_ADD_DAT17           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO264               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 265                   | D_ADD18_D_ADD_DAT18_<br>GPIO265 | P                  | D_ADD18               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T2  |
|                       |                                 | A1                 | D_ADD_DAT18           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO265               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 266                   | D_ADD19_D_ADD_DAT19_<br>GPIO266 | P                  | D_ADD19               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T3  |
|                       |                                 | A1                 | D_ADD_DAT19           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO266               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 267                   | D_ADD20_D_ADD_DAT20_<br>GPIO267 | P                  | D_ADD20               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T4  |
|                       |                                 | A1                 | D_ADD_DAT20           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO267               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>                                                             | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary       | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------------------------------------------------------------------|--------------------|-----------------------|------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                                                                      |                    |                       |                        |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 77                    | MDO6_GPIO77<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO6 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T1               | W1  | W3  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO77                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 78                    | MDO7_GPIO78<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO7 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T2               | W2  | Y1  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO78                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 79                    | MDO8_GPIO79<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO8 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T3               | W3  | W5  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO79                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 80                    | MDO9_GPIO80<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO9 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U1               | Y1  | Y2  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO80                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 81                    | MDO10_GPIO81<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO10 <sup>15</sup>   | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U2               | Y2  | Y3  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO81                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 82                    | MDO11_GPIO82<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO11 <sup>15</sup>   | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U3               | Y3  | Y4  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO82                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 47. Revision History (continued)

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
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| 8<br>(Jun-2011)    | <p>Removed spec 3 from Table 27 "PFCPR1 Settings vs Frequency of Operation"</p> <p>Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 "PMC Electrical Specifications" to a max value of <math>V_{DD12OUT} + 17\%</math>.</p> <p>Updated item 26 (Operating Current VDDA Supply) in table 14 "Electrical Specifications" from 30 mA to 40 mA.</p> <p>Updated Note 11 for Table 14 (Electrical Specifications) to read <math>IOH\_F = \{16,32,47,77\}</math> mA and <math>IOL\_F = \{24,48,71,115\}</math> mA for <math>\{00,01,10,11\}</math> drive mode with <math>VDDE = 3.0</math> V.</p> <p>Updated ID 9 in Table 11 (PMC Electrical Specifications) to</p> <p><math>V_{REG} = 4.5</math> V, max DC output current with a max of 80 mA</p> <p><math>V_{REG} = 4.25</math> V, max DC output current, crank condition with a max of 40 mA</p> <p>Updated Table 17 (DSPI LVDS Pad Specification) with the following:</p> <ul style="list-style-type: none"> <li>Spec 1 typical value updated from 40 MHz to 50 MHz</li> <li>Spec 2 added SRC conditions and associated values: <ul style="list-style-type: none"> <li>SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV</li> <li>SRC=0b01 Min 90 mV Max 320 mV</li> <li>SRC=0b10 Min 160 mV Max 480 mV</li> </ul> </li> <li>Spec 3 <ul style="list-style-type: none"> <li>Min value from 1.075 V to 1.06 V</li> <li>Max value from 1.325 V to 1.39 V</li> </ul> </li> <li>Added Spec 5, 6 and 7</li> </ul> <p>Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C</p> <p>Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to &lt; 400 us as the Max vaule.</p> <p>Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications"</p> <p>Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz.</p> <p>Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz.</p> <p>Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications".</p> <p>Updated ID 16 in Table 11, "PMC Electrical Specifications", SMPS regulator clock frequency (after reset) 2.4MHz Max</p> <p>Updated Table 16 "Flash EEPROM Module Life", spec 3, 'Blocks with 10,001–100,000 P/E cycles' to 5 Years.</p> <p>Added Typ column to Table 25, "Flash Program and Erase Specifications"</p> <p>Updated Table 3, "Absolute Maximum Ratings" with the following:</p> <ul style="list-style-type: none"> <li>Spec 1, '1.2 V Core Supply Voltage', to a Max of 2.0 V</li> <li>Spec 3, 'Clock Synthesizer Voltage', to a Max of 5.3 V</li> <li>Spec 4, 'I/O Supply Voltage' to a Max of 5.3 V</li> <li>Spec 5, 'Analog Supply Voltage' to a Max of 5.3 V</li> <li>Note 2 to read, "2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining."</li> <li>Note 3, "... 5.0 V + 10% ..." to "... 5.25 V + 10 % ..."</li> <li>Note 5, "... 3.3 V + 10% ..." to "... 3.60 V + 10 % ..."</li> </ul> <p>Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, "ESD Ratings", to 500 V</p> <p>Updated Table 27, "PFCPR1 Settings vs. Frequency of Operation", Spec 3, APC = RWSC column to 0b100.</p> <p>Updated Spec 26, "Operating Current 5.0 V Supplies @ <math>f_{sys} = 264</math> MHz" for <math>I_{DDA}</math> to 50 mA, in Table 14, "DC electrical specifications".</p> |