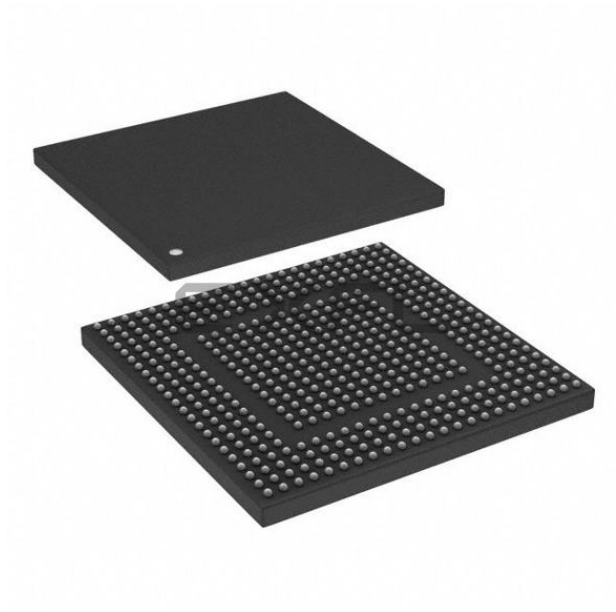

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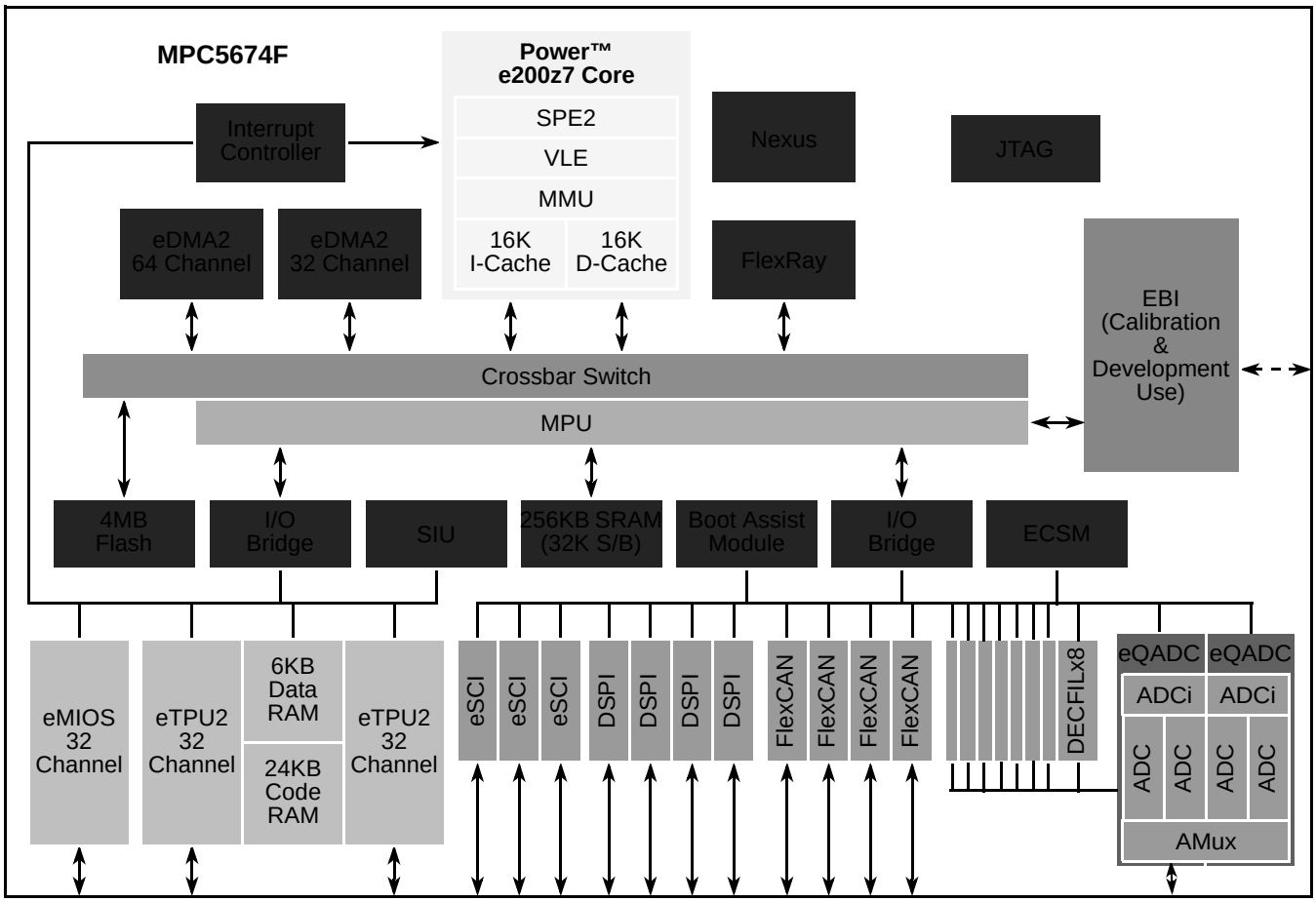
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kavms2r

2 MPC5674F Blocks

2.1 Block Diagram

Figure 2 shows a top-level block diagram of the MPC5674F device.



LEGEND

ADC	– Analog to digital convertor	**eSCI**	– Enhanced serial communications interface
ADCi	– ADC interface	**eTPU2**	– Enhanced time processing unit 2
AMux	– Analog multiplexer	**FlexCAN**	– Controller area network
DECFIL	– Decimation filter	**MMU**	– Memory management unit
DSPI	– Deserial/serial peripheral interface	**MPU**	– Memory protection unit
EBI	– External bus interface	**S/B**	– Stand-by
ECSM	– Error correction status module	**SIU**	– System integration unit
eDMA2	– Enhanced direct memory access	**SPE2**	– Signal processing engine 2
eMIOS	– Enhanced modular I/O system	**SRAM**	– General-purpose static RAM
eQADC	– Enhanced queued A/D converter module	**VLE**	– Variable length instruction encoding

Figure 2. Block Diagram

3 Pin Assignments

The figures in this section show the primary pin function. For the full signal properties and muxing table, see Appendix A, Signal Properties and Muxing.

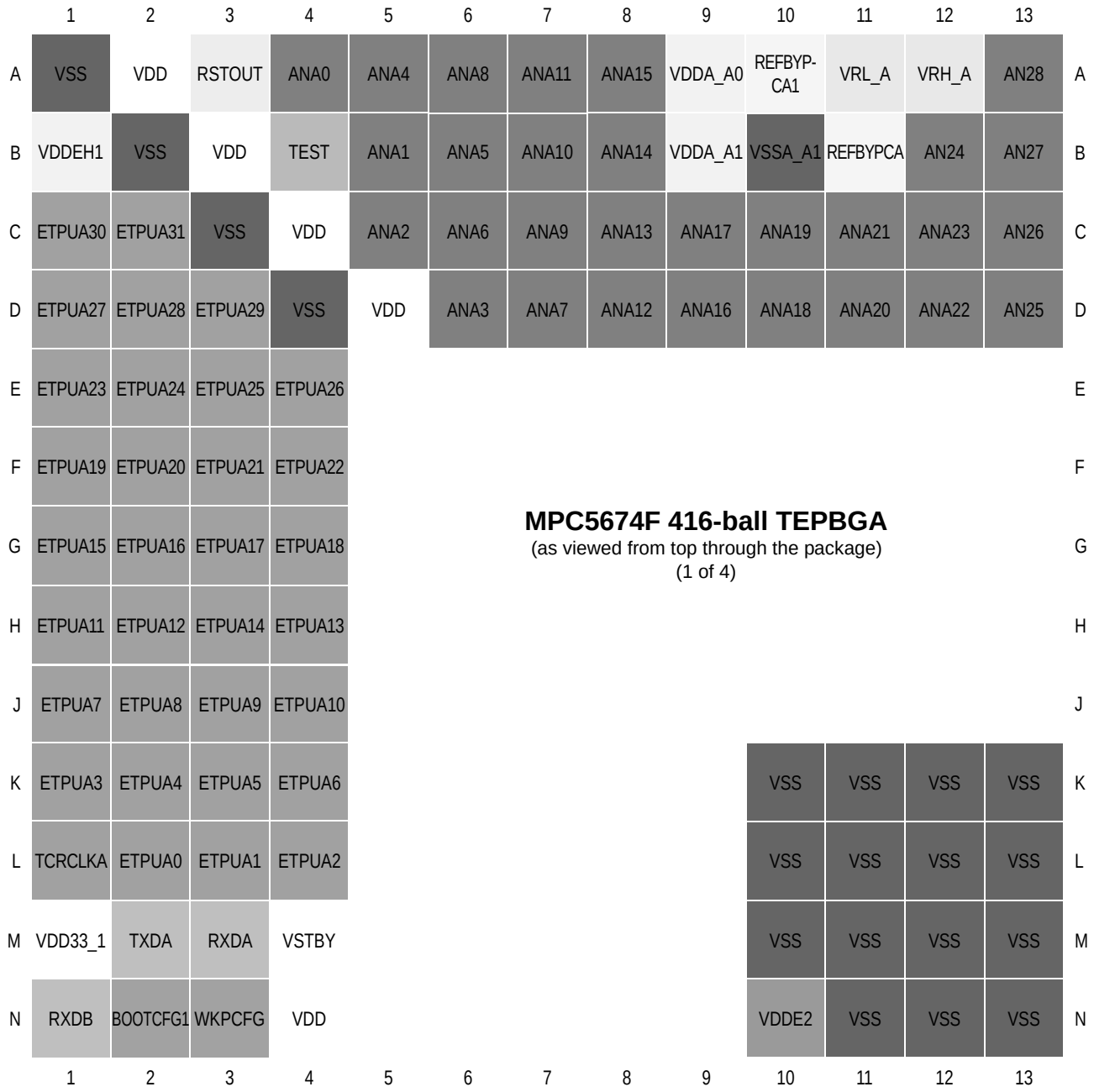
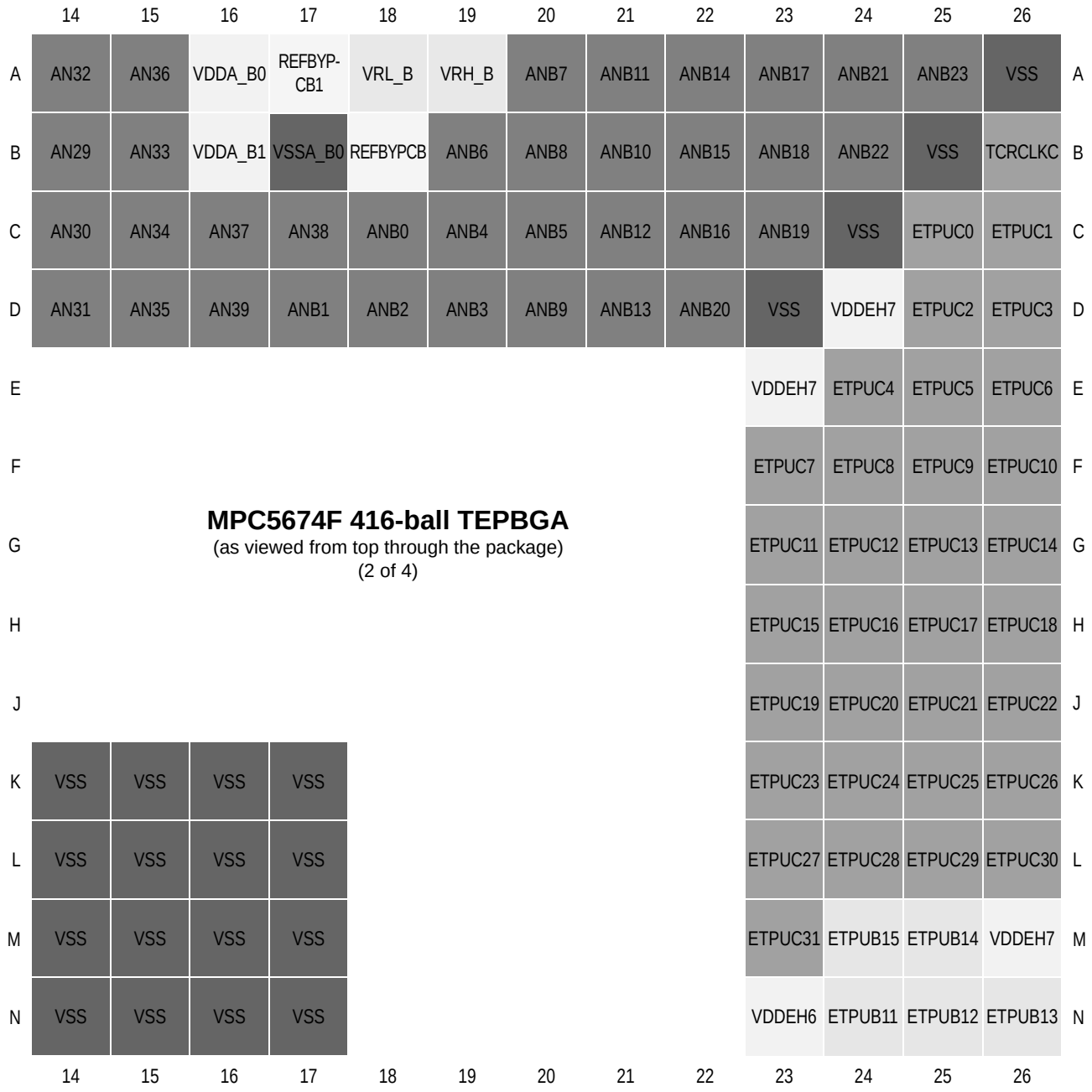
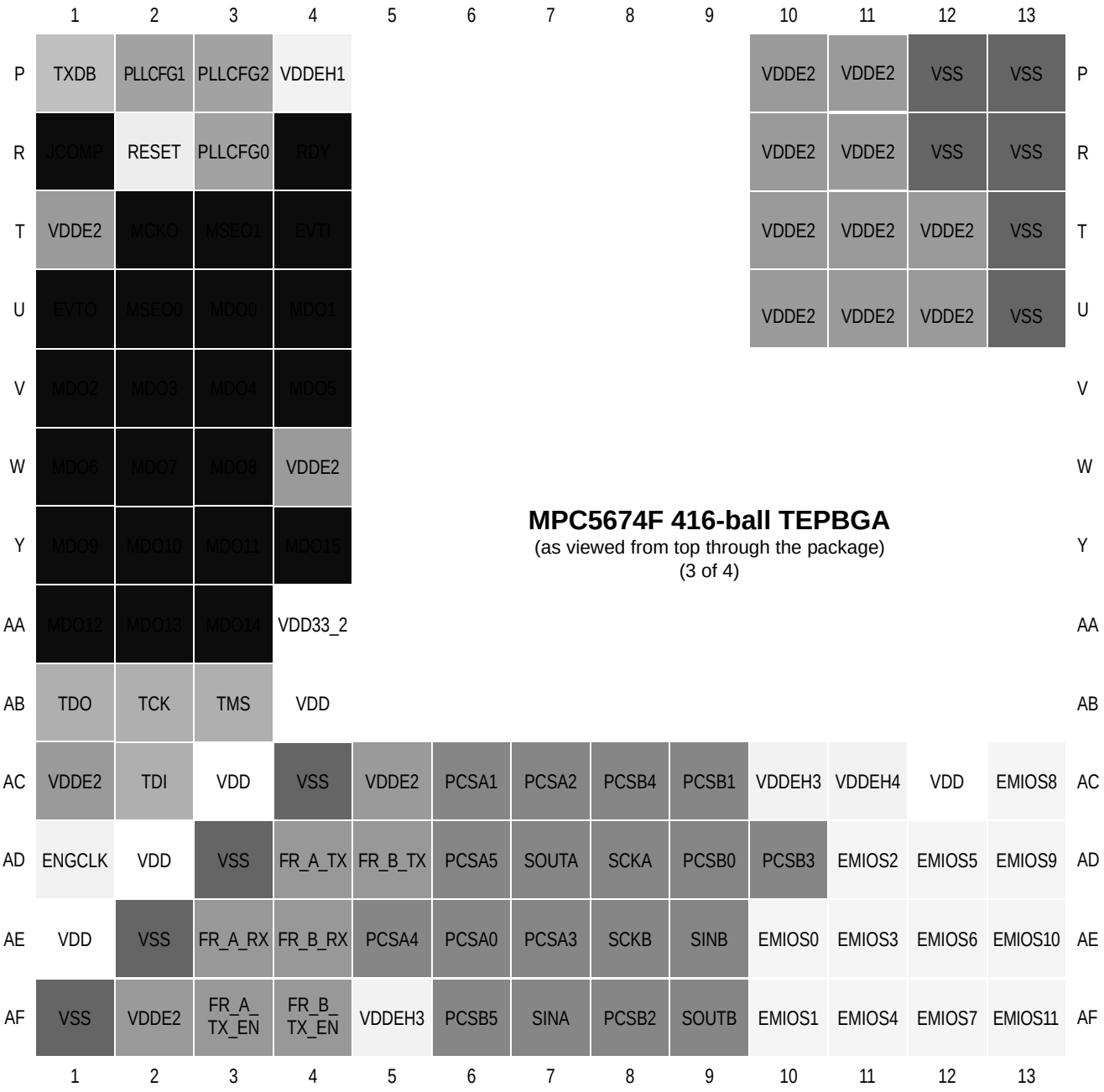


Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN32	AN36	VDDA_B0	REFBYP-CB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	AN29	AN33	VDDA_B1	VSSA_B0	REFBYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E										VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F										ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G										ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H										ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J										ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

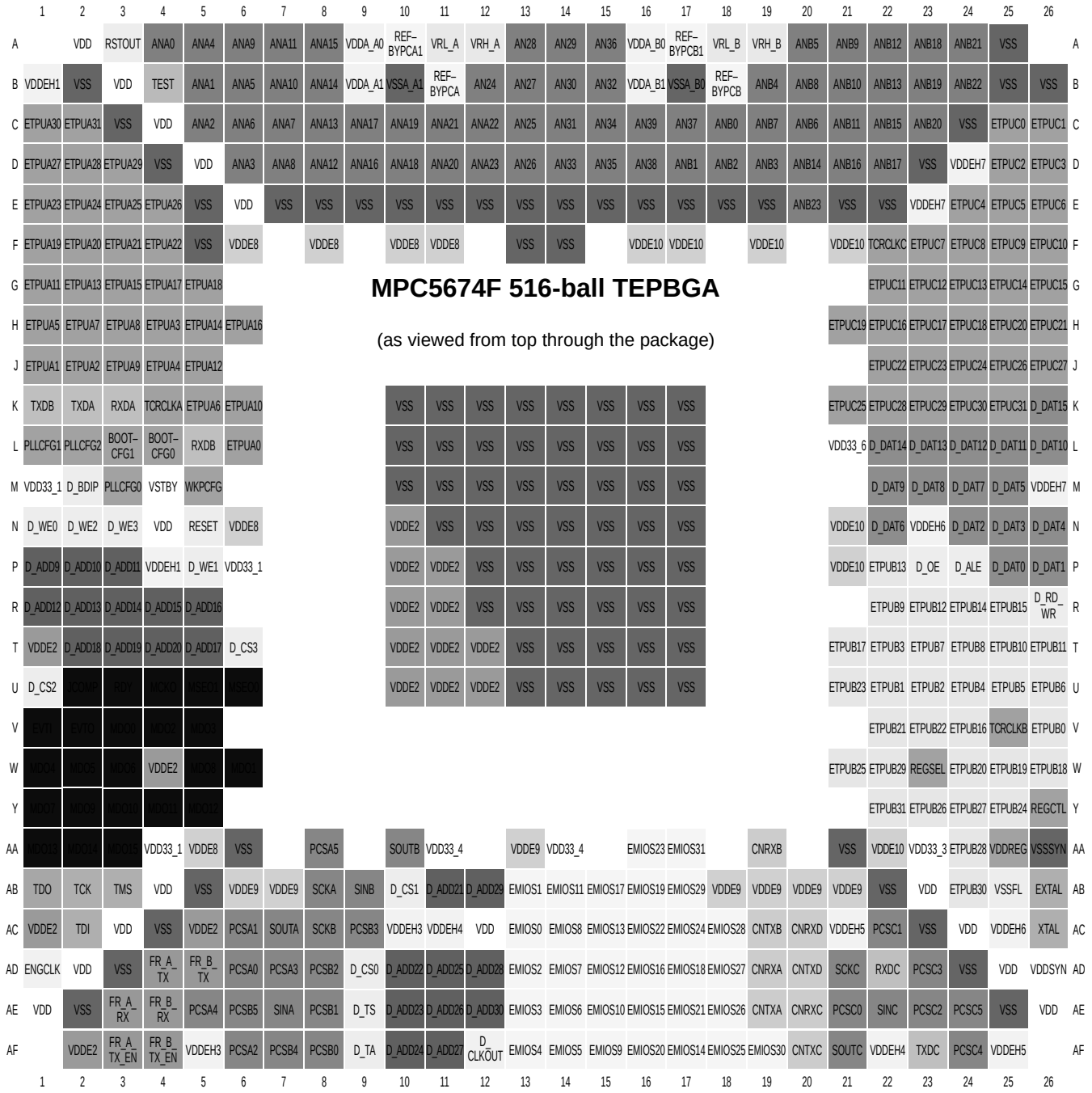


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

4.6.2 Power-Down

If V_{DD} is powered down first, then all drivers are tristated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

4.6.3 Power Sequencing and POR Dependent on V_{DDA}

During power up or down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggers POR (ADC monitors on V_{DDEH1} segment which powers the RESET pin) if the leakage current path created, when V_{DDA} is sufficiently low, causes sufficient voltage drop on V_{DDEH1} node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially V_{DDEH1}) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since $V_{DD} = 1.32$ V max.

4.7 DC Electrical Specifications

Table 14. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (External Regulation)	V_{DD}	1.14	1.32[1,2]	V
1a	Core Supply Voltage (Internal Regulation)[3]	V_{DD}	1.08	1.32	V
2	I/O Supply Voltage (fast I/O pads)	V_{DDE}	3.0	3.6[1,4]	V
3	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	3.0	5.25[1,5]	V
4	3.3 V I/O Buffer Voltage	V_{DD33}	3.0	3.6[1,4]	V
5	Analog Supply Voltage	V_{DDA}	4.75	5.25[1,5]	V
6a	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_LOW}	0.95[6]	1.2	V
6b	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_HIGH}	2	6	V
7	Voltage Regulator Control Input Voltage[7]	V_{DDREG}	2.7[8]	5.5[1,5]	V

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 850 0.10 0.15	 mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[14] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[14] 7[15]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[16] 1.0 22	 mA mA mA

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

Table 32. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

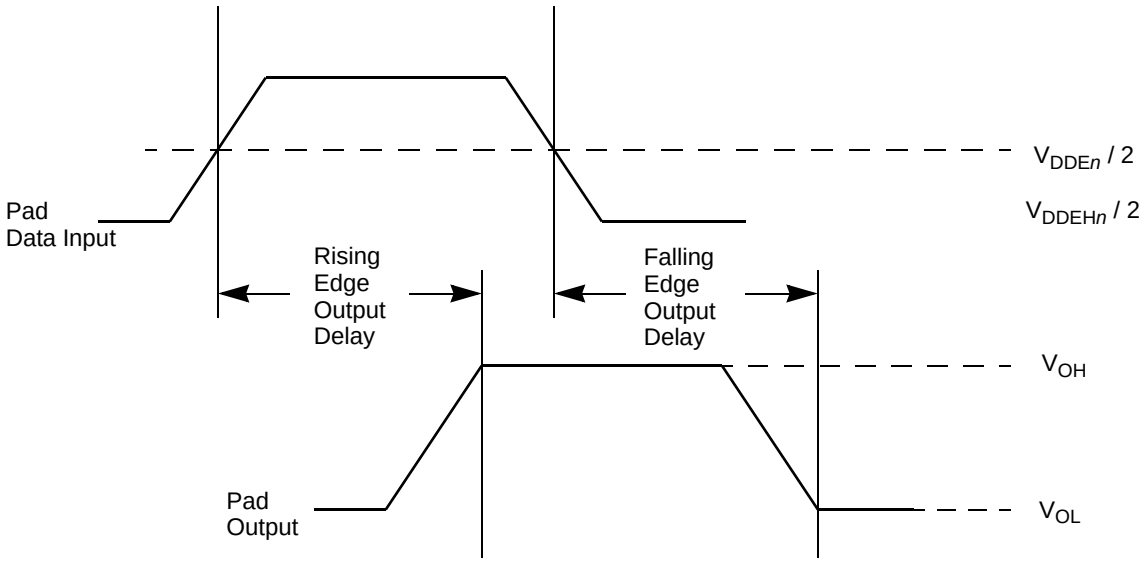


Figure 17. Pad Output Delay

4.12 AC Timing

4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 18 and Figure 19 apply to all I/O pins with pad types F and MH. See Appendix A, Signal Properties and Muxing, for the pad type for each pin.

5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in Figure 43 and Figure 44.

Figure 43. 324 TEPBGA Package (1 of 2)

Figure 44. 324 TEPBGA Package (2 of 2)

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	E1	E1
		A1	IRQ11	External interrupt request	I							
		A2	—	—	—							
		G	GPIO137	GPIO	I/O							
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E2	E2
		A1	IRQ12	External interrupt request	I							
		A2	—	—	—							
		G	GPIO138	GPIO	I/O							
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	E3	E3
		A1	IRQ13	External interrupt request	I							
		A2	—	—	—							
		G	GPIO139	GPIO	I/O							
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	E4	E4
		A1	IRQ14	External interrupt request	I							
		A2	—	—	—							
		G	GPIO140	GPIO	I/O							
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	D1	D1
		A1	IRQ15	External interrupt request	I							
		A2	—	—	—							
		G	GPIO141	GPIO	I/O							
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO142	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA14	AE16	AE17
		A1	ETPUB5	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO200	GPIO	I/O							
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W13	AC16	AC16
		A1	ETPUB6	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO201	GPIO	I/O							
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y15	AD16	AA16
		A1	ETPUB7	eTPU B channel	O							
		A2	—	—	—							
		G	GPIO202	GPIO	I/O							
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB16	AF17	AC17
		A1	PCSB0	DSPI B peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO203	GPIO	I/O							
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA15	AE17	AF18
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO204	GPIO	I/O							
432	EMIOS26_PCSB2_ GPIO432	P	EMIOS26	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y16	AD17	AE18
		A1	PCSB2	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO432	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27	AN27	—	B13	B13
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28	AN28	—	A13	A13
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29	AN29	—	B14	A14
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30	AN30	—	C14	B14
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31	AN31	—	D14	C14
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32	AN32	—	A14	B15
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33	AN33	—	B15	D14
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34	AN34	—	C15	C15
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35	AN35	—	D15	D15
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36	AN36	—	A15	A15
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37	AN37	—	C16	C17
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38	AN38	—	C17	D16
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39	AN39	—	D16	C16
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0	ANB0	B15	C18	C18
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1	ANB1	B16	D17	D17
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2	ANB2	A17	D18	D18
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3	ANB3	A18	D19	D19
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4	ANB4	B17	C19	B19
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5	ANB5	B18	C20	A20
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6	ANB6	A19	B19	C20
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7	ANB7	A20	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	ANB8	D13	B20	B20

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	ANB9	C14	D20	A21
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	ANB10	C13	B21	B21
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	ANB11	C15	A21	C21
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	ANB12	C16	C21	A22
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	ANB13	D14	D21	B22
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	ANB14	C17	A22	D20
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	ANB15	D15	B22	C22
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	ANB16	C18	C22	D21
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	ANB17	D16	A23	D22
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	ANB18	D17	B23	A23
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	ANB19	B19	C23	B23
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	ANB20	C19	D22	C23
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	ANB21	D18	A24	A24
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	ANB22	A21	B24	B24
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	ANB23	B20	A25	E20
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	VRH_A	A10	A12	A12
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	VRL_A	A11	A11	A11
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	VRH_B	A16	A19	A19
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	VRL_B	A15	A18	A18
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	REFBYPCB	B12	B18	B18
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	REFBYPCA	B11	B11	B11
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	VDDA_A0	A9	A9	A9
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	VDDA_A1	B9	B9	B9
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	REFBYPCA1	A12	A10	A10
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	VSSA_A1	B10	B10	B10
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	VDDA_B0	A13	A16	A16
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	VDDA_B1	B13	B16	B16

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
273	D_ADD26_D_ADD_DAT26_ GPIO273	P	D_ADD26	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE11
		A1	D_ADD_DAT26	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO273	GPIO	I/O							
274	D_ADD27_D_ADD_DAT27_ GPIO274	P	D_ADD27	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AF11
		A1	D_ADD_DAT27	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO274	GPIO	I/O							
275	D_ADD28_D_ADD_DAT28_ GPIO275	P	D_ADD28	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AD12
		A1	D_ADD_DAT28	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO275	GPIO	I/O							
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AB12
		A1	D_ADD_DAT29	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO276	GPIO	I/O							
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	I/O	F	V_{DDE9}	—/Up	—/Up	—	—	AE12
		A1	D_ADD_DAT30	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO277	GPIO	I/O							

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
213	WKPCFG_NMI_ GPIO213	P	WKPCFG	Weak pull configuration input	I	MH	V_{DDEH1}	WKPCFG/Up	Input/Up	—	N3	M5
		A1	NMI	Critical interrupt to core[11]	I							
		A2	—	—	—							
		G	GPIO213	GPIO	I							
208	PLLCFG0_IRQ4_ GPIO208	P	PLLCFG0	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	Input/Up	M3	R3	M3
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO208	GPIO	I/O							
209	PLLCFG1_IRQ5_ GPIO209	P	PLLCFG1	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	Input/Up (for Rev2 of the device: —/Up)	L2	P2	L1
		A1	IRQ5	External interrupt request	I							
		A2	SOUTD	DSPI D data output	O							
		G	GPIO209	GPIO	I/O							
—	PLLCFG2	P	PLLCFG2	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/ Down	PLLCFG/ Down	L3	P3	L2
—	XTAL	P	XTAL	Crystal oscillator output	O	AE	V_{DD33}	XTAL	XTAL	W22	AC26	AC26
—	EXTAL	P	EXTAL	Crystal oscillator input	I	AE	V_{DD33}	EXTAL	EXTAL	V22	AB26	AB26
229	D_CLKOUT	P	D_CLKOUT	EBI system clock output	O	F	V_{DDE9}	CLKOUT/ Enabled	CLKOUT/ Enabled	—	—	AF12
214	ENGCLK	P	ENGCLK	EBI engineering clock output Note: EXTCLK (External clock input) selected through SIU register)	O	F	V_{DDE2}	ENGCLK/ Enabled	ENGCLK/ Enabled	AA1	AD1	AD1
JTAG and Nexus (see footnote[12] about resets)												
—	$\overline{\text{EVTI}}$	–[13]	EVTI	Nexus event in	I	F	V_{DDE2}	—/Up	EVTI/Up	N4	T4	V1
227	$\overline{\text{EVTO}}$ (the BAM uses this pin to select if auto baud rate is on or off)	–[13]	EVTO	Nexus event out	O	F	V_{DDE2}	ABS/Up	EVTO/HI	P1	U1	V2
219	MCKO	–[13]	MCKO	Nexus message clock out	O	F	V_{DDE2}	O/Low	Disabled[14]	N2	T2	U4

[12] Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FPM trace is enabled. MSEO and MCKO are also dependent on trace (RPM or FPM) being enabled.

[13] The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of these pins once enabled.

[14] MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).

[15] Do not connect pin directly to a power supply or ground.

Table 47. Revision History (continued)

Revision (Date)	Description of changes
4 (cont)	“Temperature Sensor Electrical Specifications” table: Changed spec #2 to have one temperature range (-40 - 150 C) and changed spec value from ±1.0 to ±10.0 C.
	“eQADC Conversion Specifications (Operating)” table: Changed spec #13 (non-disruptive injection current) values from ±1 to ±3.
	"IPCLKDIV Settings" table, removed footnote "eMIOS and DMA are not considered peripherals here."
5 (Feb-2011)	Note 4 in Maximum Ratings updated from 2.0 V to 1.65 V. Changed I/O Supply Voltage spec in DC Electrical specs, Spec 2, from 1.62 V min to 3.0 V min. Changed the APC=RWSC value in line 1 of PFCPR1 Settings vs. Frequency of Operation table from 0b011 to 0b100 Changed note 1 for Pad AC Specifications table from Vdde = 1.62 V to 1.98 V to read Vdde = 3.0 V to 3.6 V Changed note 6 for Signal Properties and Muxing Summary table by removing the voltage range 1.8 V - 3.3 V to have 3.3 V instead of the range. Spec 2 in Table 9 “ESD Ratings“ the spec for “ESD for Charged Device Model (CDM)” changed to 250 V (other) from 500 V (other) Removed voltage ranges 1.62-1.98 V and 2.25-2.75 V from spec 28 in Table 14
6 (Feb-2011)	Same content as for Rev. 5
7 (Mar-2011)	Added entry for Rev. 6 and Rev. 7 to this table to fix a revision-numbering issue.
8 (Jun-2011)	Added the following footnotes to the “Signal Properties and Muxing Summary” table: • Footnote 10, for the ANA[0:7] signals, “During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.” • Footnote 15, for MDO[0:15] and MSEO[0:1] signals, “Do not connect pin directly to a power supply or ground.”
	Changed min and max values of ID 1 “Nominal bandgap reference voltage“ in Table 11 (PMC Electrical Specifications) to 0.608 V min and 0.632 V max. Changed min and max values of Spec 2 “ADC Bandgap” in Table 23 (ADC Band Gap Reference/LVI Electrical Specifications) to 1.171 V min and 1.269 V max. Changed Spec 3 of Table 26 (Flash EEPROM Module Life) from 'Minimum Data Retention at 25 °C ambient temperature' to 'Minimum Data Retention at 85 °C ambient temperature'
	Added Spec 41, 42, 43 and 44 to the “DC Electrical Specifications” table Added Note 25 to the “DC Electrical Specifications” table for Spec 41, 42 and 43 Added Note 26 to the “DC Electrical Specifications” for Spec 44 Added Spec 17 to the “eQADC Conversion Specifications (Operating)” table. Added Spec 18 to the “eQADC Conversion Specifications (Operating)” table. Added Note 15 to the “eQADC Conversion Specifications (Operating)” table for Spec 17 and 18.