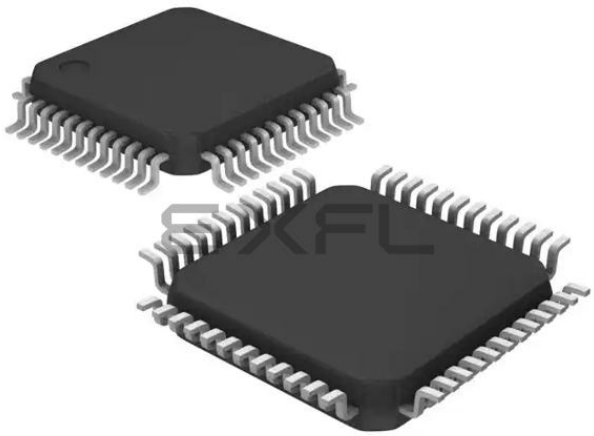

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

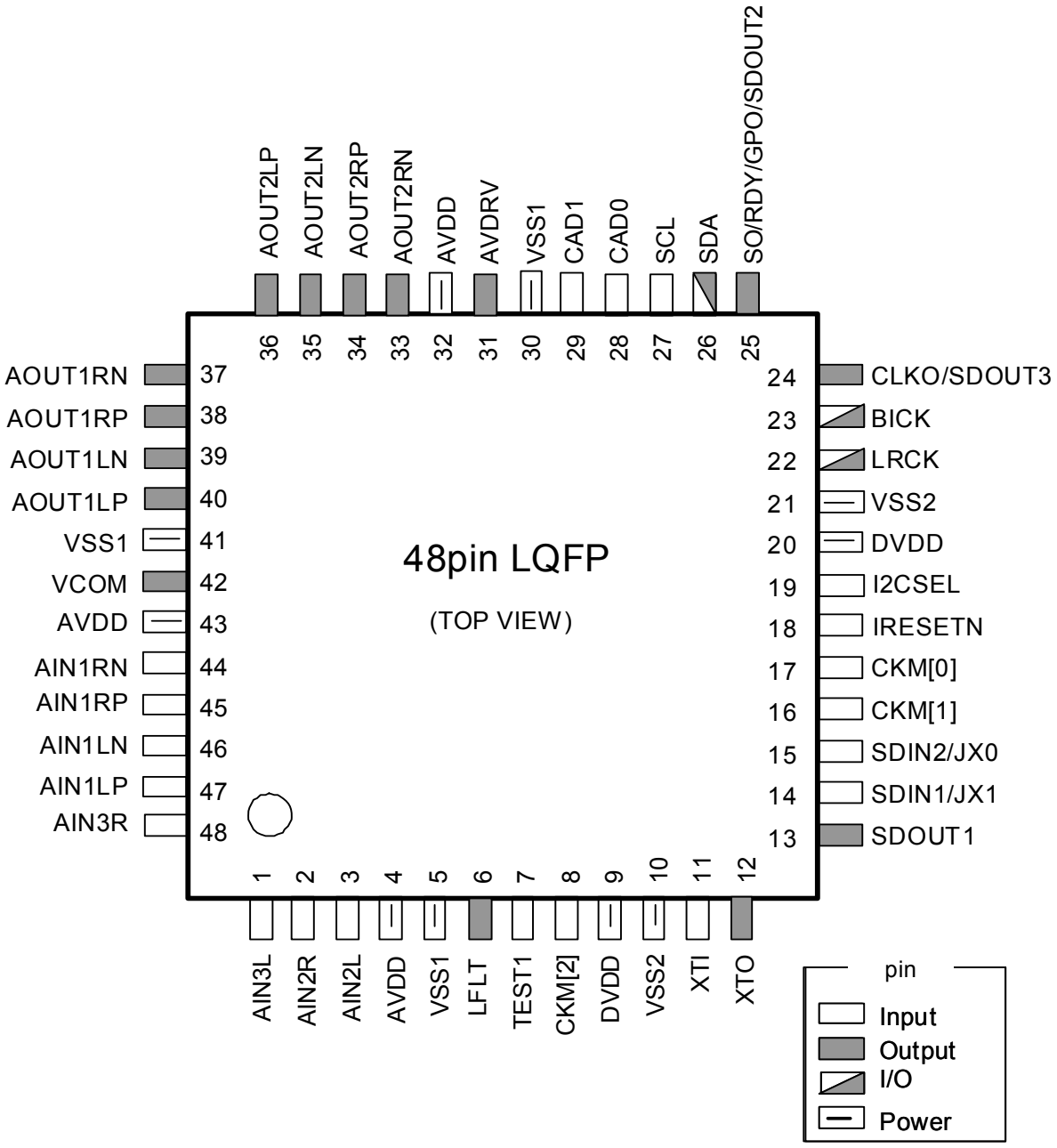
Details	
Product Status	Obsolete
Type	Floating Point
Interface	I²C
Clock Rate	18.6MHz
Non-Volatile Memory	-
On-Chip RAM	23.25kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/akm-semiconductor/ak7742eq

■ Ordering Guide

AK7742EQ	-20 ~ +70°C	48pin LQFP (0.5mm pitch)
AK7742EN	-20 ~ +85°C	48pin QFN (0.4mm pitch)
AKD7742	Evaluation board for the AK7742	

■ Pin Layout

AK7742EQ



31	AVDRV	O	AVDRV Pin Connect 1μF to VSS1. Never to use for external circuit. “L” output during initial reset	Analog power supply
32	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
33	AOUT2RN	O	DAC2 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
34	AOUT2RP	O	DAC2 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
35	AOUT2LN	O	DAC2 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
36	AOUT2LP	O	DAC2 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
37	AOUT1RN	O	DAC1 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
38	AOUT1RP	O	DAC1 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
39	AOUT1LN	O	DAC1 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
40	AOUT1LP	O	DAC1 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
41	VSS1		Analog ground 0V	Analog power supply
42	VCOM	O	Analog common voltage Connect 0.1μF and 2.2μF in parallel to VSS1. Never to use for external circuit. “L” output during initial reset	Analog output
43	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
44	AIN1RN	I	ADC Rch differential inverted analog input pin	Analog input
45	AIN1RP	I	ADC Rch differential non-inverted analog input pin	Analog input
46	AIN1LN	I	ADC Lch differential inverted analog input pin	Analog input
47	AIN1LP	I	ADC Lch differential non-inverted analog input pin	Analog input
48	AIN3R	I	ADC Rch Single-end input 3 pin	Analog input

Note:

Digital input pins are never to be left open.

If analog input pins (AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R) are not used, leave them open.

DIGITAL FILTER CHARACTERISTICS

■ ADC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Pass band (±0.005dB) (Note 18)	PB	0		21.5	kHz
(-0.02dB)			21.768		kHz
(-6.0dB)			24.00		kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 18)	PR			±0.005	dB
Stop band attenuation (Note 19, Note 20)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		30		Ts
Digital filter + Analog filter characteristics					
Amplitude characteristic 20Hz~20.0kHz			±0.01		dB

Note 17. Each parameter is related to the sampling frequency (fs). HPF response is not included.
Note 18. Pass band is from DC to 21.5kHz when fs=48kHz.
Note 19. Stop band is from 26.5kHz to 3.0455MHz when fs=48kHz.
Note 20. When fs=48kHz, the analog modulator samples the analog input at 3.072MHz. Therefore the input signal is not attenuated by the digital filter in multiple bands (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3 …) of the sampling frequency.

■ DAC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 21)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 21)	SB	26.2			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	64			dB
Group delay (Ts=1/fs) (Note 22)	GD	-	24		Ts
Digital filter + Analog filter					
Amplitude characteristic 0~20.0kHz			±0.5		dB

Note 21. Pass band and Stop band parameter is related to sampling frequency(fs). PB=0.4535fs (at-0.05dB), SB=0.5465fs.
Note 22. The digital filter's delay is calculated as the time from setting 24-bit data into the input register until an analog signal is output.

OPERATION OVERVIEW

■ CKM[2:0] Clock Mode Select Pin

Master/Slave mode switching, MCLK/ICLK (internal master clock/generating clock) clock source pin select, and ICLK frequency change are controlled by CKM [2:0] clock mode select pins. CKM[2:0] pins can only be set during initial reset.

CKM Mode	CKM [2:0]	Master Slave	MCLK source	Input frequency for MCLK	Input pin(s) required for system clock	use the oscillator permitted
0	000	Master	XTI	12.288MHz (Note 32)	XTI (256fs)	YES
1	001	Slave	XTI	18.432MHz (Note 32)	XTI (384fs), BICK (32fs, 48fs, 64fs) LRCK (fs)	-
2	010	Slave	XTI	12.288MHz (Note 32, Note 35)	XTI(256fs), BICK (32fs, 48fs, 64fs), LRCK (fs)	-
3	011	Slave	BICK	64fs (fs=48kHz fixed)	BICK, LRCK	-
4	100	Slave	BICK	32fs (fs=8kHz fixed)	BICK, LRCK	-
5	101	Slave	BICK	64fs (fs=8kHz fixed)	BICK, LRCK	-
6	110	TEST	N/A	N/A	N/A	-
7	111	TEST	N/A	N/A	N/A	-

(N/A: Not available)

Note 32. On operating fs=44.1kHz series, multiply 44.1/48.
Note 33. CKM mode 6/7 are for testing purpose only. Cannot be used.
Note 34. The sampling frequency is set by control register CONT0 in CKM mode 0.
Note 35. In case of CKM mode 1/2, XTI and LRCK must be synchronized. The phase is not critical.
Note 36. The sampling frequency on CKM mode 3-5 is fixed. The setting of control register CONT0 is ignored.
Note 37. In case of CKM mode 3-5, BICK must be divided exactly from LRCK. BICK and LRCK must be synchronized.

[Description rule]
Regarding the input / output levels in this Datasheet, the low level is represented as "L" and the high level is represented as "H". The registers or bus pins (such as CKM[2:0] is represented "0" and "1".
##h means hexadecimal code. (# = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

1) CONT0: Sampling rate, I/O interface

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C0h	40h	CONT0	DIFPCM	DIFI2S	PCM[1]	PCM[0]	DFS[2]	DFS[1]	DFS[0]	0	00h

DIFPCM: Audio interface select

0: MSB justified, LSB justified, I²S (default)
1: PCM format

Note 42. When using PCM format, D6: DIFI2S must be set "0".

DIFI2S: Audio interface I²S select

0: Except I²S mode (default)
1: I²S mode

When using I2S mode for SDIN1-2, SDOUT1-3, set to DIFI2S bit = "1". All interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit). DIFI2S bit should be set to "0" when using DSP through mode, and all interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit).

Note 43. When using I²S format, D7: DIFPCM must be set "0".

PCM[1:0]: PCM format select (only slave mode available)

Select PCM interface at DIFPCM bit = "1".
PCM format is available for CKM mode 3/4/5.

PCM Mode	PCM[1:0]	LRCK (FRAME)	LRCK edge referenced to BICK edge	BIT32FS bit 0	BIT32FS bit 1	
0	00	short (SF)	rising (RE)	Figure 21	Figure 22	(default)
1	01	short (SF)	falling (FE)	Figure 23	Figure 24	
2	10	long (LF)	rising (RE)	Figure 25	Figure 26	
3	11	long (LF)	falling (FE)	Figure 27	Figure 28	

Please refer to "Audio Data Interface" section.

DFS[2:0]: Sampling frequency setting (CKM Mode 0/1/2)

fs: sampling frequency

CKM Mode	CKM [2:0]	DFS Mode	DFS [2:0]	fs(kHz) 48kHz series	fs(kHz) 44.1kHz series	
0-2	0XX	0	000	48	44.1	(default)
0-2	0XX	1	001	32	29.4	
0-2	0XX	2	010	16	14.7	
0-2	0XX	3	011	8	-	
0-2	0XX	4	100	96	88.2	
3	011	-	-	48	44.1	
4	100	-	-	8	-	
5	101	-	-	8	-	
6	110	-	-	N/A	N/A	
7	111	-	-	N/A	N/A	

(N/A: Not available)

Note 44. DFS mode is available for CKM mode 0/1/2.
No permission to set DFS mode 5-7.

Write "0" into the "0" register.

2) CONT1: RAM control

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C1h	41h	CONT1	ATSPAD	ATSPDA	BANK[1]	BANK[0]	TEST	SS[1]	SS[0]	0	00h

ATSPAD: ADC soft mute transition

0: 912LRCK(max) (19ms at fs=48kHz) (default)
1: 912LRCK x 4(max) (76ms at fs=48kHz)

ATSPDA: DAC1/2 Volume Transition Time Setting

0: 1/fs (default)
1: 4/fs

BANK[1:0]: DLRAM Mode setting

DLRAM Mode	BANK[1:0]	Ring 24bit limited range floating point	Ring 8.4f	Linear 24bit limited range floating point	
0	00	3072word			(default)
1	01	2048word	2048word		
2	10	1024word	2048word	1024word	
3	11	N/A	N/A	N/A	

(N/A: Not available)

SS[1:0]: DLRAM sampling setting

SS Mode	SS[1]	SS[0]	Sampling set time	
0	0	0	address is updated every sampling	(default)
1	0	1	address is updated every 2 samplings	
2	1	0	address is updated every 4 samplings	
3	1	1	address is updated every 8 samplings	

Note 45. When SS mode 1/2/3 is selected, aliasing noise may be generated.
Note 46. DLRAM mode 1/2 affects to the Ring 8.4f buffer only. DLRAM mode 0 affects to the Ring 20.4f buffer.

Write "0" into the TEST bits and "0" registers.

5) CONT4: Clock / Output setting

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C4h	44h	CONT4	CLKOE	BITCLKEN	LRCLKEN	OUT2EN	OUT1EN	JX1E	JX0E	0	00h

CLKOE: CLKO output enable

0: CLKO output disable (default)
1: CLKO output enable

BITCLKEN:

When the AK7742 is in master mode, BICK output can be stopped.
0: Enable (default)
1: Disable (Low output)
When CKM mode 1-5, AK7742 is in slave mode. Appropriate BICK clock is required.

LRCLKEN:

When the AK7742 is in master mode, LRCK output can be stopped.
0: Enable (default)
1: Disable (Low output)
When CKM mode 1-5, AK7742 is in slave mode. Appropriate LRCK clock is required.

OUT2EN: SO/RDY/GPO/SDOUT2 disable

0: SO/RDY/GPO/SDOUT2 output enable (default)
1: SO/RDY/GPO/SDOUT2 output disable

OUT1EN: SDOUT1 output enable

0: SDOUT1 output disable (default)
1: SDOUT1 output enable

JX1E:

0: Select SDIN1/JX1 pin for DSP input port SDIN1 (default)
1: Select SDIN1/JX1 pin for DSP input port JX1

JX0E:

0: Select SDIN2/JX0 pin for DSP input port DIN2 (default)
1: Select SDIN2/JX0 pin for DSP input port JX0

Write "0" into the "0" registers.

6) CONT5: DSP output select

Write during system reset state.

		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
C5h	45h	CONT5	SELDO5 [0]	SELDO4 [0]	SELDO3	SELDO2[1]	SELDO2[0]	SELDO1	SELDO4 [1]	0	00h

D7: SELDO5[0] DAC2 SDINDA2 input select

SELDO5 Mode	SELDO5[1] CONT6 D3	SELDO5[0] CONT5 D7	Input Data Select	
0	0	0	DSP Port: DOUT5	(default)
1	0	1	SDIN2 Pin	
2	1	0	SDIN1 Pin	
3	1	1	ADC Port: SDOUTAD	

D6: SELDO4[0] DAC1 SDINDA1 input select

SELDO4 Mode	SELDO4[1] CONT5 D1	SELDO4[0] CONT5 D6	Input Data Select	
0	0	0	DSP Port: DOUT4	(default)
1	0	1	SDIN1 Pin	
2	1	0	SDIN2 Pin	
3	1	1	ADC Port: SDOUTAD	

D5: SELDO3 CLKO/SDOUT3 output select

0: CLKO (default)
1: DSP port DOUT3

D4, D3: SELDO2[1:0] SO/RDY/GPO/SDOUT2 output select

SELDO2 Mode	SELDO2[1:0]	Output Function	
0	00	SO	(default)
1	01	RDY	
2	10	DSP GPO	
3	11	DSP DOUT2	

D2: SELDO1 SDOUT1 output select

0: DSP port DOUT1 (default)
1: ADC SDOUTAD

D1: SELDO4[1]

Refer to D6

Write "0" into the TEST bits and "0" registers.

7) CONT6: ADC setting

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C6h	46h	CONT6	ADMUTE	Reserved	ASEL[1]	ASEL[0]	SELDO5[1]	DA2MUTE	DA1MUTE	0	00h

D7: ADMUTE ADC SMUTE setting

0: ADC SMUTE release (default)
1: ADC SMUTE

D6: Reserved

0: normal operation (default)
Set to "0"

D5, D4: ASEL[1:0] ADC input select

ASEL Mode	ASEL1[1:0]	selected pin(s)	
0	00	AIN1LP, AIN1LN, AIN1RP, AIN1RN	(default)
1	01	AIN2L, AIN2R	
2	10	AIN3L, AIN3R	
3	11	N/A	

(N/A: Not available)

In case that this register is changed while an operation, take a measure of mute process to reduce switching noise.

D3: SELDO5[1] DAC2 SDINDA2 Input Setting

Refer to D7

D2: DA2MUTE DAC2 SMUTE Setting

0: DAC2 SMUTE disable (default)
1: DAC2 SMUTE enable

D1: DA1MUTE DAC1 SMUTE Setting

0: DAC1 SMUTE disable (default)
1: DAC1SMUTE enable

Write "0" into the TEST bit(s) and "0" register(s).

■ Reset

1) Definition of reset state

The AK7742 has three types of reset function which are Initial reset, Clock reset and System reset. Operating condition (RUN state) is defined as when these reset are released. In the Initial reset condition, the IRESETN pin= "L" and all blocks DSP/PLL/ADC/DAC and etc. go sleep. The System reset condition is when the IRESETN pin= "H", SRESET bit= "0", PLL and VREF blocks are in operation and DSP/ADC/DAC are not in operation. Clock reset is one of the System reset but CKRST bit = "1". This mode can be used for changing a main clock or clock source when PLL and internal clock are stopped. After the Initial reset is released, during System reset, each register settings and program writings are made. Program down-loading to the DSP is prohibited until PLL oscillation is stabilized.

2) Initial reset

Initial reset is required to initialize all AK7742 blocks. As IRESETN pin= "L", all control registers are initialized, internal counters, ADC, DAC, DSP, PLL, etc. are stopped. When changing the IRESETN pin to "H", VREF circuit (Analog reference voltage) and PLL for master clock starts operating and control register writing become valid.

CKM[2:0] pin setting or main clock source must be changed during this initial reset. CKM[2:0] pins are related to main PLL circuit and internal counter control, therefore these pin sate changing on another state of the device may cause erroneous operation.

3) System reset

DSP Program download is executed in system reset. It is recommended that set all control registers except for SRESETN in this state. In system reset, ADC / DAC / DSP are stopped. VREF circuit and PLL are in operation. LRCK and BICK output is stopped if the AK7742 is in master mode. System reset state will be released when set SRESETN register to "1" and the AK7742 switches to RUN.

4) Clock Reset

CKM[2:0] pin settings and Input clock ICLK (XTI@CKM Mode 0/1/2 or BICK@CKM Mode 3/4/5) can be also changed during the clock reset as well as during initial reset.

By this reset, both the PLL and the internal clocks stop and clock selection can be safely done during System Reset. After System Reset, the AK7742 enters Clock Reset condition by setting the CKRST bit = "1" (CONT8 D1). Change pin settings and input clock frequency during Clock Reset. The PLL re-starts by exiting the clock reset condition (CKRST bit = "1" to "0") after those changes are made and the input clock settles to its final setting. Transmission of DSP program, Coefficient Data and other data from an external microcontroller is prohibited until the PLL reaches stable oscillation (50ms). After transferring DSP program, Coefficient Data and other data, the AK7742 returns to normal operation by bringing SRESETN bit to "1".

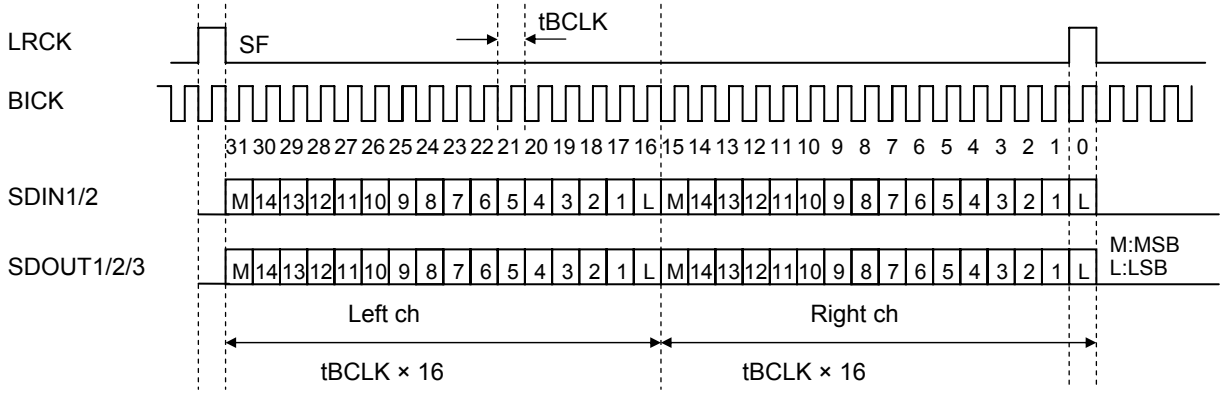


Figure 24. 32fs Short-frame, Falling-edge (CKM Mode 4)

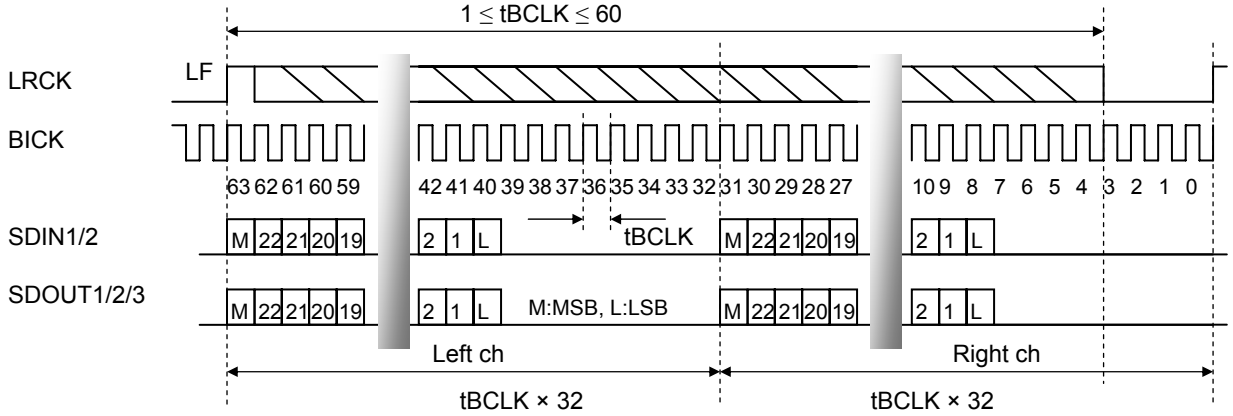


Figure 25. 64fs Long-frame, Rising-edge

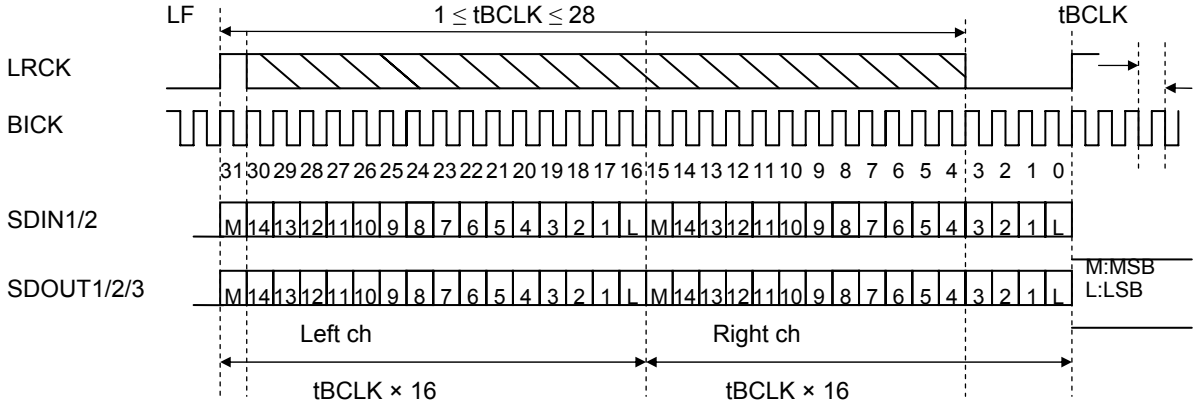


Figure 26. 32fs Long-frame, Rising-edge

[4] Read in system reset

1. Program RAM (PRAM) read (during System Reset)

	Input	Output
(1) COMMAND	38h	
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8	
(3) ADDRESS2	A7-A0	
(4) DATA1		0 0 0 0 D35 D34 D33 D32
(5) DATA2		D31-D24
(6) DATA3		D23-D16
(7) DATA4		D15-D8
(8) DATA5		D7-D0
	(It is possible to read data from sequential address by 1word:5byte unit)	

2. Coefficient RAM (CRAM) read (during System Reset)

	Input	Output
(1) COMMAND	34h	
(2) ADDRESS1	0 0 0 0 0 0 A9 A8	
(3) ADDRESS2	A7-A0	
(4) DATA1		D15-D8
(5) DATA2		D7-D0
	(It is possible to read data from sequential address by 1word:2byte unit)	

3. Offset RAM (OFRAM) read (during System Reset)

	Input	Output
(1) COMMAND	32h	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0	
(4) DATA1		0 0 0 D12 D11 D10 D9 D8
(5) DATA2		D7-D0
	(It is possible to read data from sequential address by 1word:2byte unit)	

[5] Read in system reset state and in operation state

1. Control register read (during System Reset and RUN)

	Input	Output
(1) COMMAND	40h-5Fh	
(2) DATA		D7-D0

2. Device identification (during System Reset and RUN)

	Input	Output							
(1) COMMAND	60h								
(2) DATA		D7	D6	D5	D4	D3	D2	D1	D0
		0	1	0	0	0	0	1	0
		4				2			

[6] Read in operation state

1. @MICR read (during RUN)

	Input	Output
(1) COMMAND	76h	
(2) DATA1		D27-D20
(3) DATA2		D19-D12
(4) DATA3		D11-D4
(5) DATA4		D3 D2 D1 D0 (flag) (flag) (flag) (flag)

Note 54. Flag bit all “0” shows that data is valid.

2. @MIR2 read (during RUN)

	Input	Output
(1) COMMAND	78h	
(2) DATA1		D27-D20
(3) DATA2		D19-D12
(4) DATA3		D11-D4
(5) DATA4		D3 D2 D1 D0 (flag) (flag) (flag) (flag)

Note 54. Flag bit all “0” shows that data is valid.

3. Read Sequence

In the AK7742, when a "write- slave-address assignment" is received at the first byte, the read command at the second byte and the data at the third and succeeding bytes are received. At the data block, the address is received in a single byte unit in accordance with a read command code. In a command code without an address assignment, the sequence does not have to be repeated (*2 in Figure 36).

When the last address byte (or command code if no address assignment is specified) is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a "read- slave-address assignment" is received in the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes (*3 in Figure 36) is fixed by the received read command.

After reading the last byte, assure that a "not acknowledged" signal is received. If this "not acknowledged" signal is not received, the AK7742 continues to send data regardless whether data is present or not, and since it did not release the BUS, the stop condition cannot be properly received.

Usable command codes in the read sequence are listed in the following "(Table 2) Read Command".

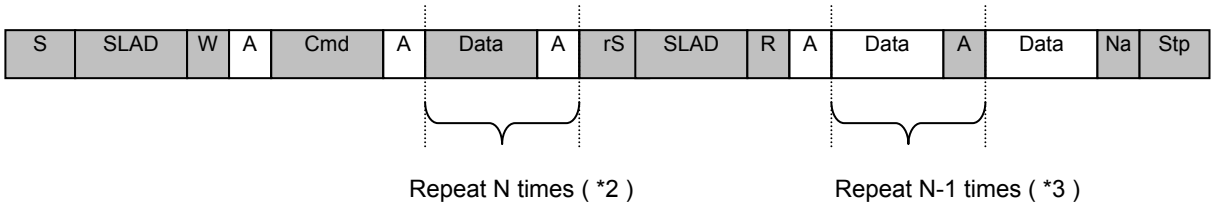


Figure 36. Read Sequence

Command Code	Address	Data length	Content
32h	2byte	2byte×n	Read from OFRAM (in system reset state)
34h	2byte	2byte×n	Read from CRAM (in system reset state)
38h	2byte	5byte×n	Read from PRAM (in system reset state)
40h-4Fh	none	1byte	Read from Register 0-15
60h	none	1byte	Device identification
76h	none	4byte	Read @MICR. 28-bit data is upper-bit-justified. Lower 4-bits are for validity flags. Valid at 0000.
78h	none	4byte	Read @MIR2. 28-bit data is upper-bit-justified. Lower 4-bits are for validity flags. Valid at 0000.

Note 59. Length of data is variable with the area to be read. As for access to RAM, it is possible to read data at sequential address locations by reading data continuously.

Table 2. Read Command

Note: The meaning of symbols in the I^2C format figures

SLAD	•••SlaveAddress (7 bits)
Cmd	•••Command Code (8 bits)
S	•••StartCondition
rS	•••Repeated StartCondition
Stp	•••StopCondition
W	•••R / W bit, the lowest bit of the first byte is at write (= 0) condition, Write (1 bit)
R	•••R / W bit, the lowest bit of the first byte is at read (= 1) condition, Read (1 bit)
A	•••Acknowledge (1 bit)
Na	•••NotAcknowledge (1 bit)
(Gray)	••• (Gray) where it is controlled by Master device.
(White)	••• (White) where it is controlled by Slave device. It is done by the AK7742.

■ ADC block

1. ADC High-pass filter

The AK7742 ADC has digital High Pass Filter (HPF) for DC offset cancellation. The cut-off frequency of the HPF is approximately 1Hz (at fs=48kHz). This cut-off frequency is proportional to the sampling frequency.

Sampling frequency (fs)	48kHz	44.1kHz	8kHz
Cut-off frequency	0.93Hz	0.86Hz	0.16Hz

Table 3. Cut-off Frequency of the High Pass Filter

2. Soft mute

The ADC block has digital soft mute circuit. When the ADSMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA x ATT transition time from the current ATT level. When the ADSMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in ATT_DATA x ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission. The transition time is 912 LRCK clock (depends on DATT register setting).

The soft mute function works when the ADC is in operation.
ATT_DATA is initialized by the INITRSTN pin = "L".

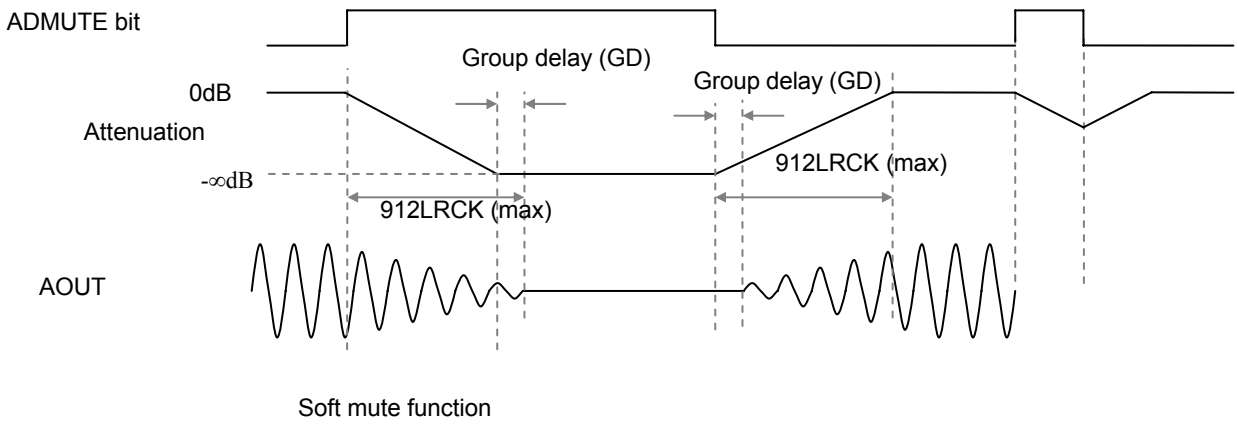


Figure 38. Soft Mute

4. ADC Digital Volume

The AK7742 has channel-independent digital volume control (256 levels, 0.5dB step).
The VOLADL[7:0] and VOLADR[7:0] bit set the volume level of each ADC channel.

ADC Lch VOLADL [7:0]	ADC Rch VOLADR [7:0]	Attenuation Level	
00h	00h	+24.0dB	
01h	01h	+23.5dB	
02h	02h	+23.0dB	
:	:	:	
2Fh	2Fh	+0.5dB	
30h	30h	0.0dB	(default)
31h	31h	-0.5dB	
:	:	:	
FDh	FDh	-102.5dB	
FEh	FEh	-103.0dB	
FFh	FFh	Mute (-∞)	

Table 4. ADC Digital Volume Level Setting

Transition time between set values of VOLADL[7:0] and VOLADR[7:0] bits can be selected by ATSPAD bit.

Mode	ATSPAD bit	Attenuation speed	
0	0	1/fs	(default)
1	1	4/fs	

Table 5 Transition Time between set values of VOLADL[7:0], VOLADR[7:0] bits

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00H to FFH(MUTE) in Mode 0. If the INITRSTN pin goes to “L”, the VOLADL[7:0] and VOLADR[7:0] bits are initialized to 30h.

■ DAC block

1. De-emphasis Filter Control

The AK47742 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter corresponding to f 48kHz sampling frequency. DEM1[1:0] bits control the de-emphasis filter for DAC1 and DEM2[1:0] bits control the de-emphasis filter for DAC2.

DEM Mode	DEM[1:0] bit	fs	
0	00	Off	(default)
1	01	48KHz	
2	10	44.1KHz	
3	11	32KHz	

Table 6. De-emphasis Control

2. DAC Digital Volume control

The DACs of the AK7742 have channel-independent digital volume control (256 levels, 0.5dB step). The VOLDA1L[7:0] and VOLDA1R[7:0] (DAC1), VOLDA2L[7:0] and VOLDA2R[7:0] (DAC2) bits set the volume level of each DAC channel.

VOLDA2L[7:0] byte VOLDA2R[7:0] byte VOLDA1L[7:0] byte VOLDA1R[7:0] byte	Attenuation Level	
00h	+12dB	
01h	+11.5dB	
02h	+11.0dB	
17h	+0.5dB	
18h	0.0dB	(default)
19h	-0.5dB	
FDh	-114.5dB	
FEh	-115dB	
FFh	Mute	

Table 7. DAC1 and DAC2 Digital Volume Level Setting

Transition time between set values can be selected independently by ATSPDA bit.

Mode	ATSPDA bit	Attenuation speed	
0	0	1/fs	(default)
1	1	4/fs	

Table 8. DAC1 and DAC2 Volume Transition Time

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00H to FFH(MUTE) in Mode 0. If the INITRSTN pin goes to “L”, the VOLDA2L[7:0], VOLDA2R[7:0], VOLDA1L[7:0] and VOLDA1R[7:0] bits are initialized to 18H.

4) Analog Output

The analog output is full differential. The output range is ±1.83Vpp (typ.) centered on VCOM voltage of AVDD/2(typ). The input code format is in 2's complement. Positive full-scale output corresponds to 7FFFFFh(@24bit) input code, Negative full scale is 800000h(@24bit) and VCOM voltage ideally is 000000h(@24bit)
The differential output has AVDD/2 + few mV DC offset. A capacitor to cut DC component should be connected. Figure 44 is an example of output buffer circuit.

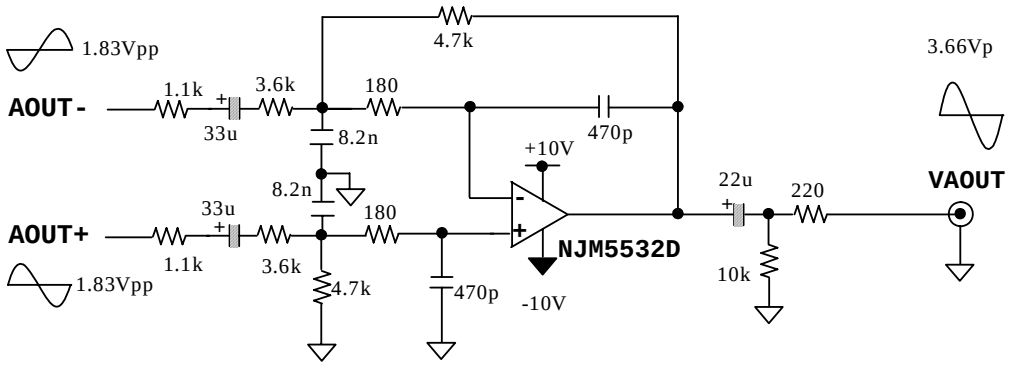


Figure 44. Output buffer circuit

1.1kΩ resisters should be connected as near as possible to the pin.

5) Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown in Table 9.

CKM Mode	Equivalent Circuit Parameter		XTI, XTO pin external (CL)
	R1 (max)	C0 (max)	
0	70Ω	5pF	22pF

Table 9. Cristal Oscillator

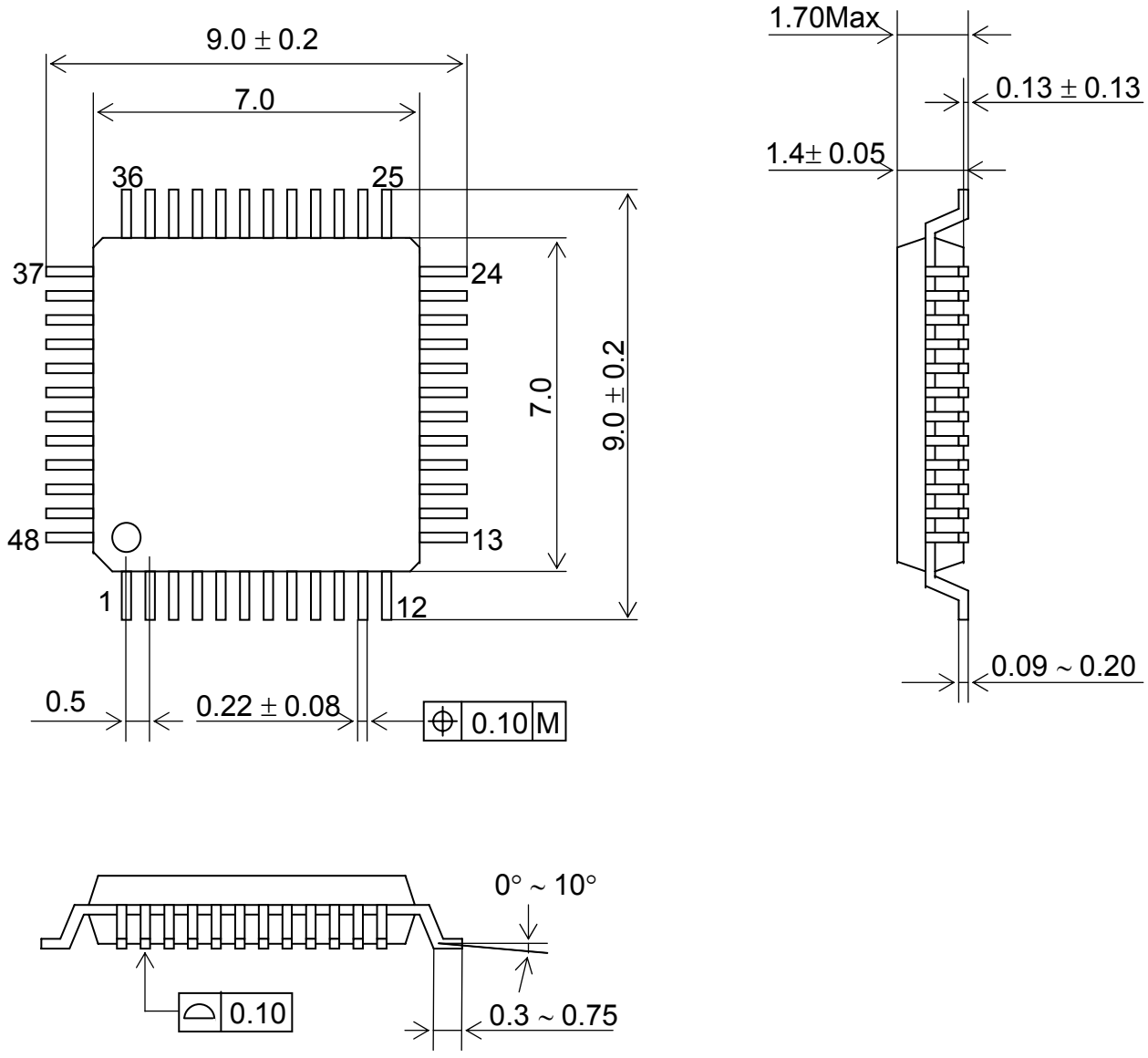
6) LFLT Pin External

The LFLT pin should be connected a capacitor with the following specification.

C1
12 nF ± 30%

PACKAGE (AK7742EQ)

48pin LQFP (Unit: mm)



■ Materials and Lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate