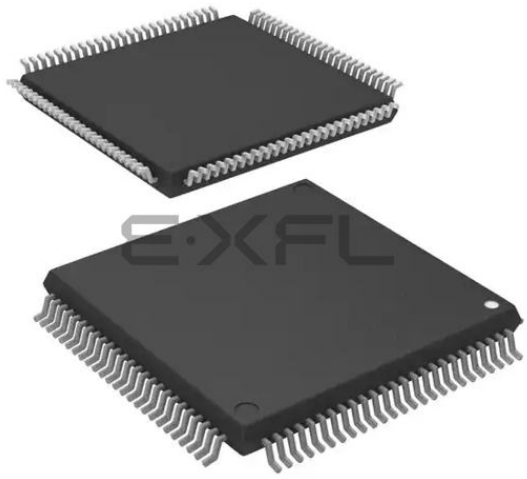

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3913gc-r-ueu-ax

(5) Port n function control expansion register (PFCEn)

The PFCEn register specifies the alternate function of a port pin to be used if the pin has three or more alternate functions.

Each bit of this register corresponds to one pin of port n, and the alternate function of a port pin can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCEn	PFCEn7	PFCEn6	PFCEn5	PFCEn4	PFCEn3	PFCEn2	PFCEn1	PFCEn0

	7	6	5	4	3	2	1	0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCEnm	PFCnm	Specification of alternate function
0	0	Alternate function 1
0	1	Alternate function 2
1	0	Alternate function 3
1	1	Alternate function 4

(6) Pull-up resistor option register (PUn)

PUn is a register that specifies the connection of an on-chip pull-up resistor.

Each bit of the pull-up resistor option register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PUn	PUn7	PUn6	PUn5	PUn4	PUn3	PUn2	PUn1	PUn0

PUnm	Control of on-chip pull-up resistor connection
0	Not connected
1	Connected

Table 4-15. Output Data and Port Read Value for Each Setting (7/10)

Port Name	Function	PMCmn	PFCEmn	PFCmn	PMmn	Output Data	Pmn Read Value	Remark
P40[Note]	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	SIF0	1	0	0	0	–	Port latch	Alternate input (serial input)
					1		Pin level	
	RXDA0	1	0	1	0	–	Port latch	Alternate input (serial input)
					1		Pin level	
	TOA00	1	1	1	0	Alternate output (timer output)	Port latch	
					1		Pin level	
P41	Output port	0	None	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	SOF0	1	None	0	0	Alternate output 1 (serial output)	Port latch	
					1		Pin level	
	TXDA0	1	None	1	0	Alternate output 2 (serial output)	Port latch	
					1		Pin level	

Note The P40 pin is also used for on-chip debugging. Switching between the on-chip debug function and port function (including the alternate function) can be done by using the $\overline{\text{DRST}}$ pin level. The following shows the setting method.

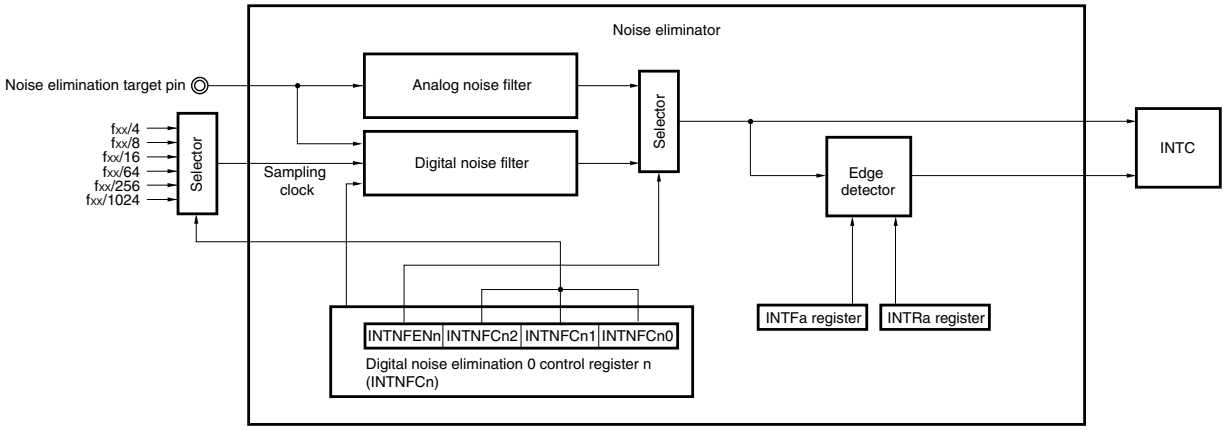
Port 4 Functions	
Low-Level Input to $\overline{\text{DRST}}$ Pin	High-Level Input to $\overline{\text{DRST}}$ Pin
P40/SIF0/RXDA0/TOA00	DDI

Remark ×: 0 or 1

The components of the noise eliminator are shown below.

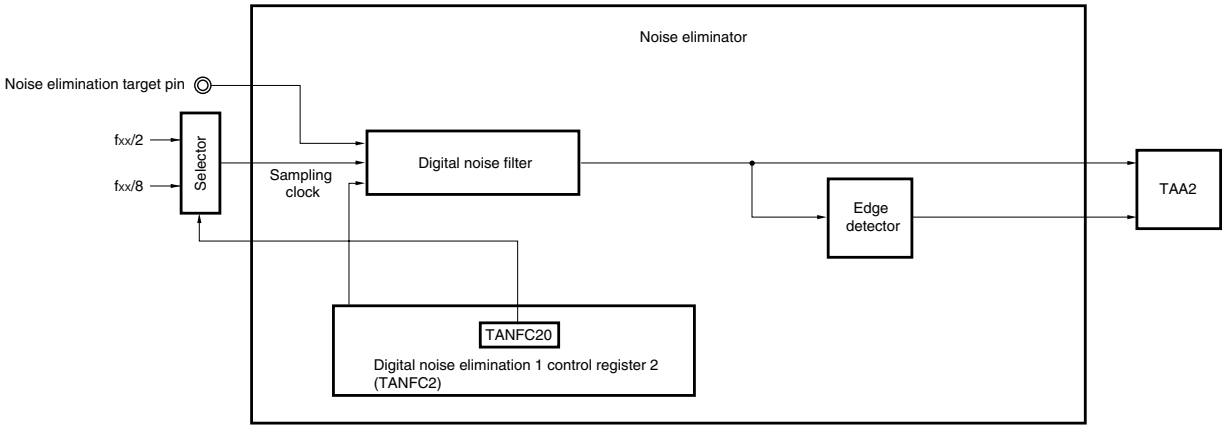
Figure 4-5. Components of Noise Eliminator (1/2)

(a) Eliminating noise on the INTP00 to INTP02, or INTP17 to INTP19 pins



Remark n = 00 to 02, 17 to 19
a = 2 when n = 00 to 02
a = 3 when n = 17 to 19

(b) Eliminating noise on the TIA20 or TIA21 pin



(2) TAAn control register 1 (TAAnCTL1)

The TAAnCTL1 register is an 8-bit register that controls the TAAn operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(1/2)

After reset: 00H R/W Address: TAA0CTL1 FFFFF661H, TAA1CTL1 FFFFF681H, TAA2CTL1 FFFFF6A1H

TAAnCTL1 (n = 0 to 2, a = 0, 1)

7	6	5	4	3	2	1	0
TAAaSYE Note 1	TAAnEST	TAA2EEE Note 2	0	0	TAAnMD2	TAAnMD1	TAAnMD0

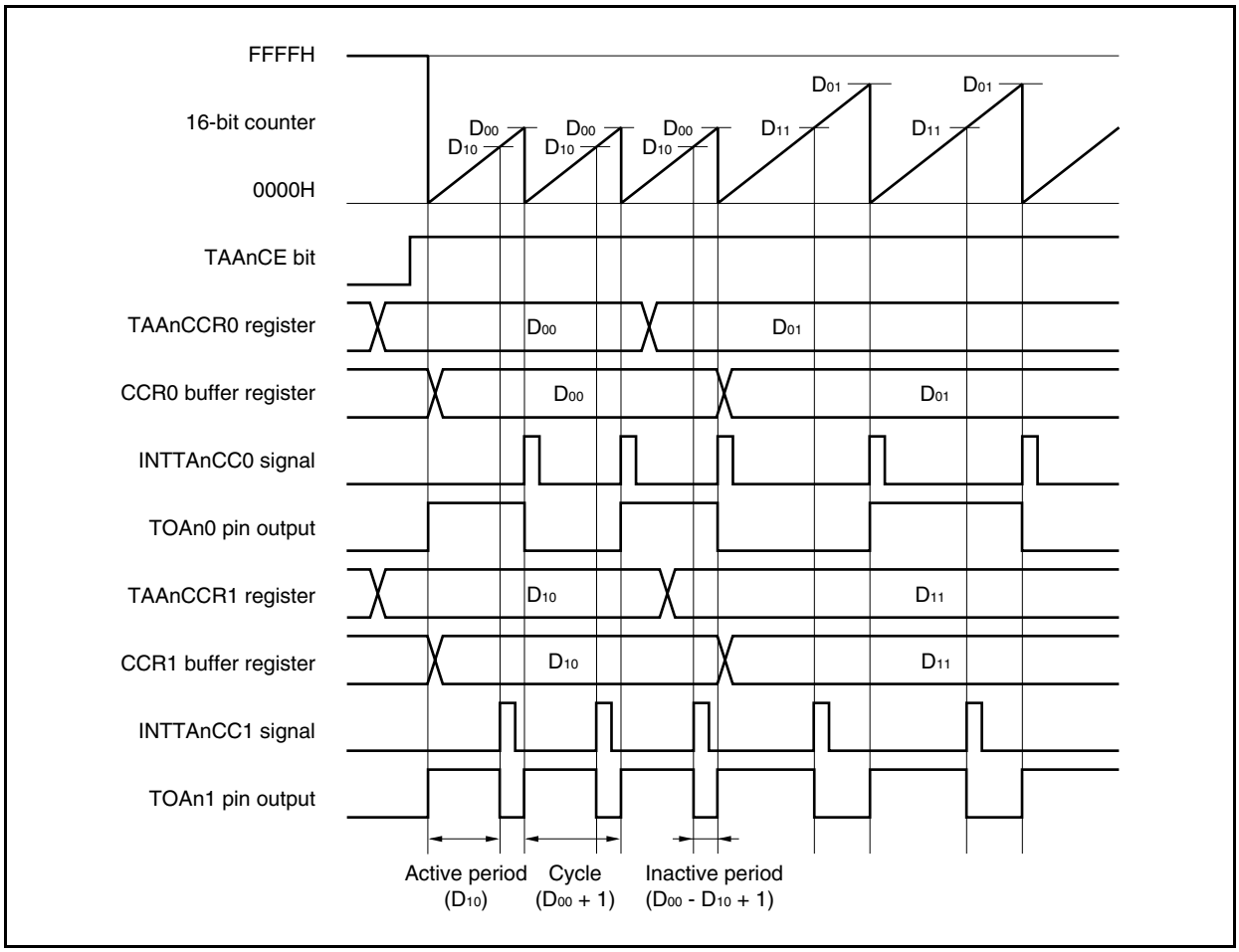
TAAaSYE Note 1	Operation mode selection
0	TAAa single mode
1	Tuning operation mode (see **10.4.5**)
TAAa can be used only as an A/D conversion start trigger factor of A/D converters 0 and 1 during the tuning operation. In the tuning operation mode, this bit always operates in synchronization with TABa.	

TAAnEST	Software trigger control
0	–
1	Generates a valid signal for external trigger input. • In one-shot pulse output mode: A one-shot pulse is output with writing 1 to the TAAnEST bit as the trigger. • In external trigger pulse output mode: A PWM waveform is output with writing 1 to the TAAnEST bit as the trigger.
The read value of the TAAnEST bit is always 0.	

Notes 1. This bit can be set only in TAA0 and TAA1. Be sure to set bit 7 of TAA2 to “0”.
For details of tuning operation mode, see **CHAPTER 10 MOTOR CONTROL FUNCTION**.

2. This bit can be set only in TAA2. Be sure to set bits 5 of TAA0 and TAA1 to “0”.

Figure 6-34. Basic Timing in PWM Output Mode



When the TAAnCE bit is set to 1, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a PWM waveform from the TOAn1 pin.

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TAAnCCR1 register) × Count clock cycle
Cycle = (Set value of TAAnCCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TAAnCCR1 register)/(Set value of TAAnCCR0 register + 1)

The PWM waveform can be changed by rewriting the TAAnCCRa register while the counter is operating. The newly written value is reflected when the count value of the 16-bit counter matches the value of the CCR0 buffer register and the 16-bit counter is cleared to 0000H.

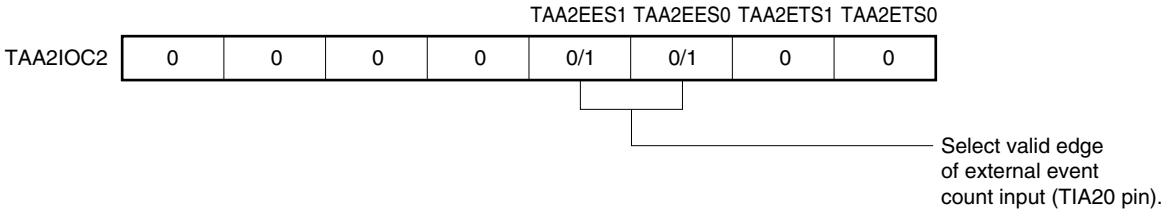
The compare match interrupt request signal INTTAnCC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTAnCC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The value set to the TAAnCCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

Remark n = 0 to 2
a = 0, 1

Figure 6-35. Register Setting in PWM Output Mode (2/2)

(d) TAA2 I/O control register 2 (TAA2IOC2)



(e) TAAn counter read buffer register (TAAnCNT)

The value of the 16-bit counter can be read by reading the TAAnCNT register.

(f) TAAn capture/compare registers 0 and 1 (TAAnCCR0 and TAAnCCR1)

If D_0 is set to the TAAnCCR0 register and D_1 to the TAAnCCR1 register, the cycle and active level of the PWM waveform are as follows.

Cycle = (D_0 + 1) × Count clock cycle

Active level width = D_1 × Count clock cycle

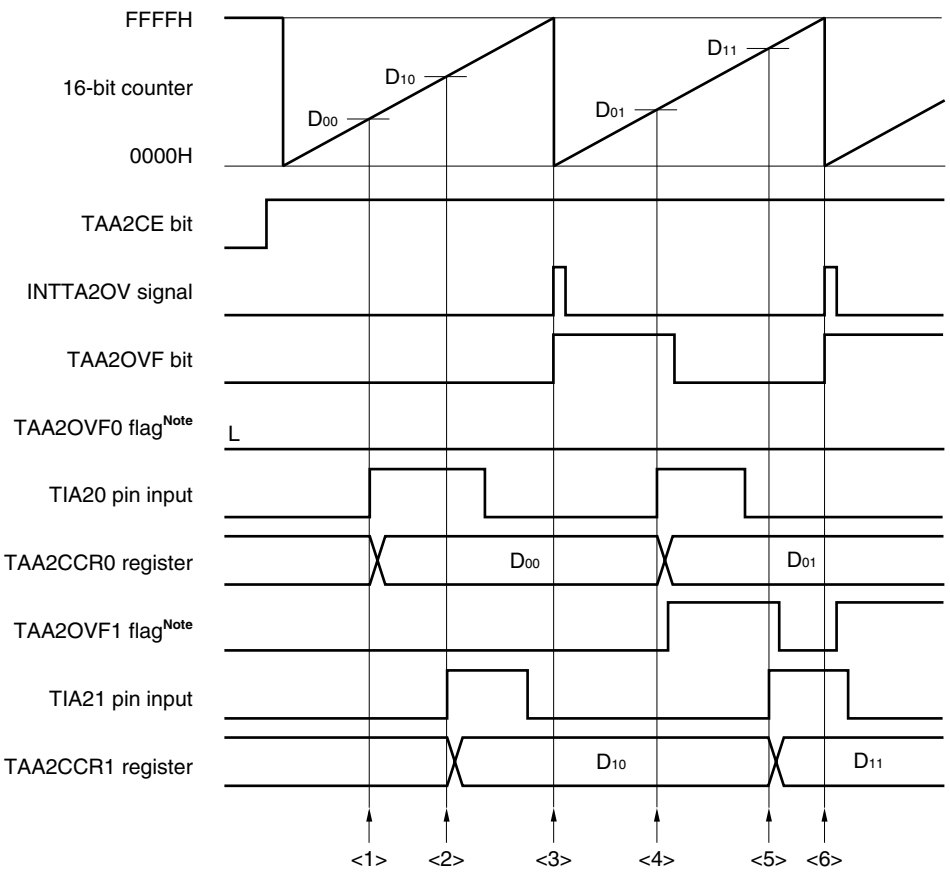
Remarks 1. TAA2 I/O control register 1 (TAA2IOC1) and TAAn option register 0 (TAAnOPT0) are not used in the PWM output mode.

2. n = 0 to 2

a = 0, 1

(2/2)

Example when two capture registers are used (without using overflow interrupt)



Note The TAA2OVF0 and TAA2OVF1 flags are set on the internal RAM by software.

<1> Read the TAA2CCR0 register (setting of the default value of the TIA20 pin input).
<2> Read the TAA2CCR1 register (setting of the default value of the TIA21 pin input).
<3> An overflow occurs. Nothing is done by software.
<4> Read the TAA2CCR0 register.
Read the overflow flag. If the overflow flag is 1, set only the TAA2OVF1 flag to 1, and clear the overflow flag to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).
<5> Read the TAA2CCR1 register.
Read the overflow flag. Because the overflow flag is cleared in <4>, 0 is read.
Read the TAA2OVF1 flag. If the TAA2OVF1 flag is 1, clear it to 0.
Because the TAA2OVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} − D_{10}) (correct).
<6> Same as <3>

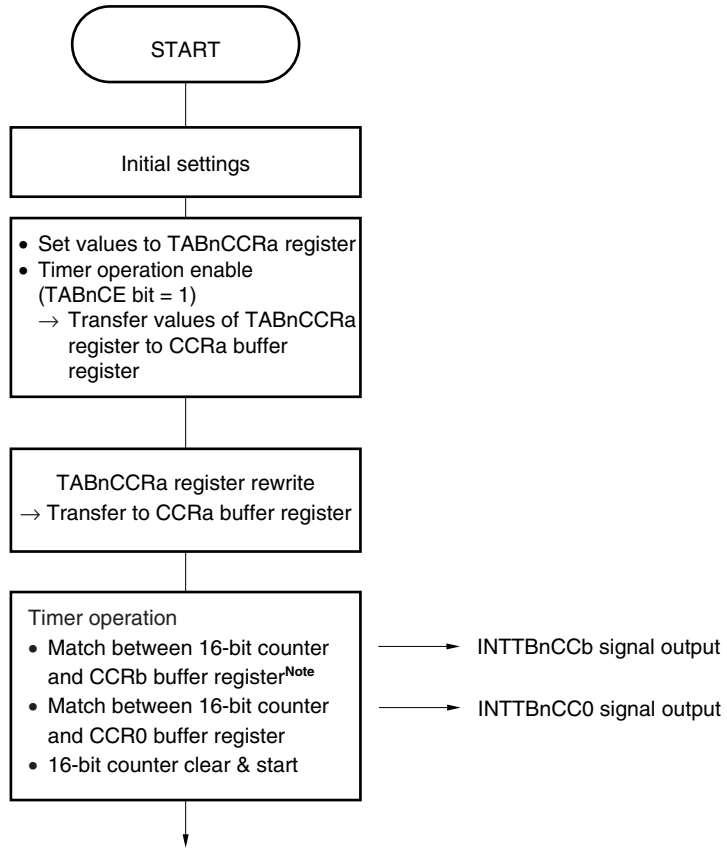
(2) Anytime write and batch write

The TABnCCR0 to TABnCCR3 registers can be rewritten in the TABn during timer operation (TABnCTL0.TABnCE bit = 1), but the write method (anytime write, batch write) of the CCR0 to CCR3 buffer registers differs depending on the mode.

(a) Anytime write

In this mode, data is transferred at any time from the TABnCCR0 to TABnCCR3 registers to the CCR0 to CCR3 buffer registers during the timer operation.

Figure 7-2. Flowchart of Basic Operation for Anytime Write



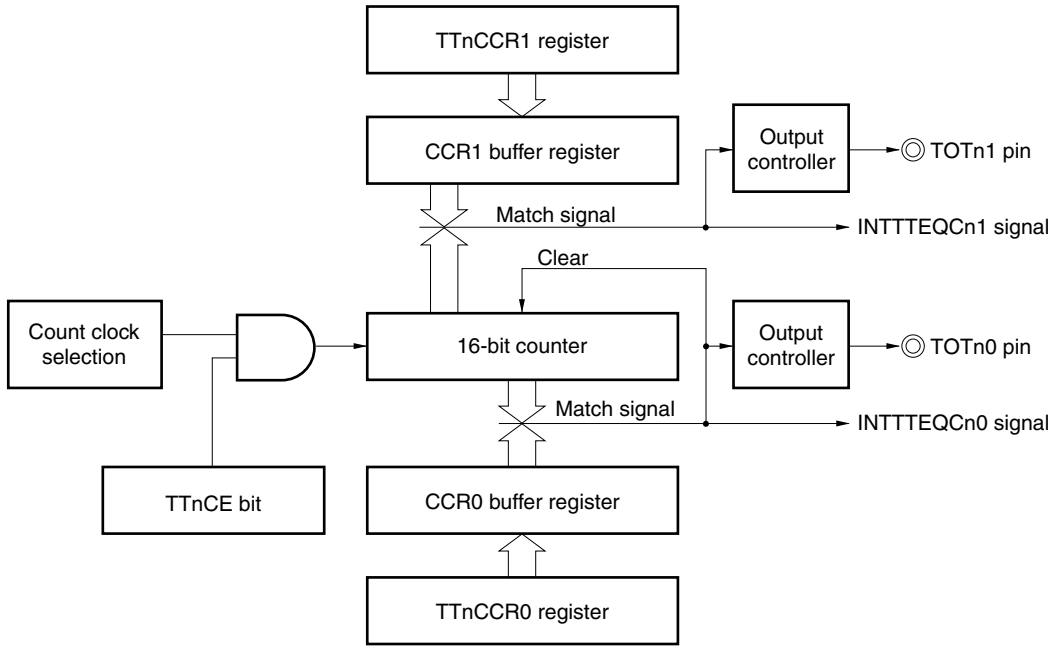
Note The 16-bit counter is not cleared upon a match between the 16-bit counter value and the CCRb buffer register value. It is cleared upon a match between the 16-bit counter value and the CCR0 buffer register value.

Remarks 1. The above flowchart illustrates an example of the operation in the interval timer mode.

2. n = 0, 1
a = 0 to 3
b = 1 to 3

(d) Operation of TTnCCR1 register

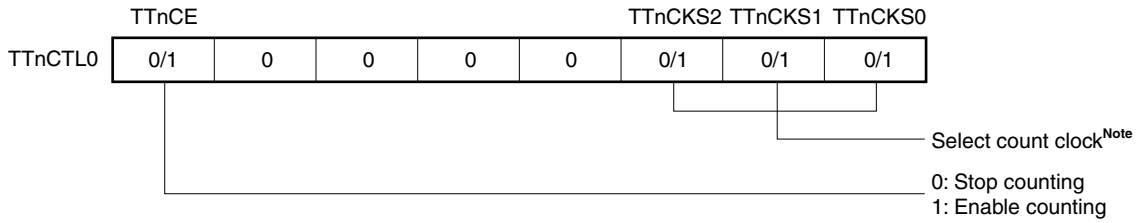
Figure 8-11. Configuration of TTnCCR1 Register



Remark n = 0 to 3

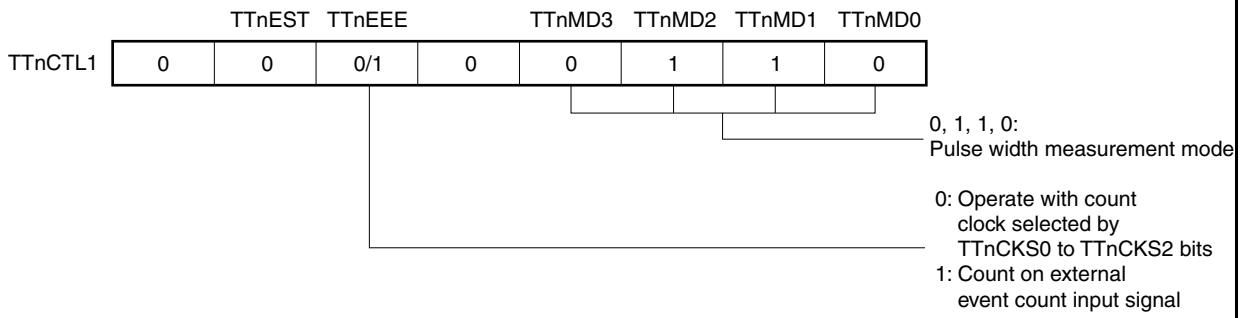
Figure 8-47. Register Setting in Pulse Width Measurement Mode (1/2)

(a) TMTn control register 0 (TTnCTL0)

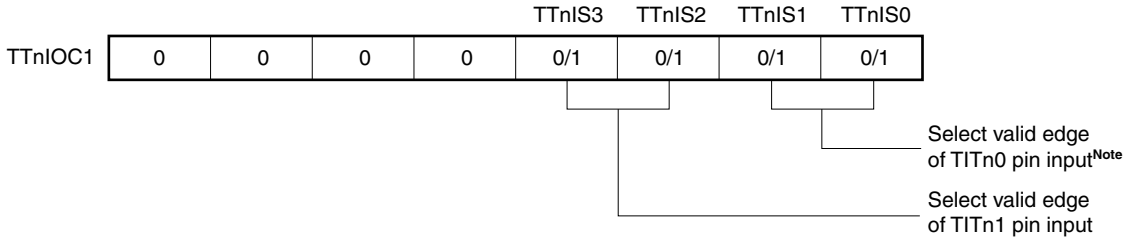


Note Setting is invalid when the TTnCTL1.TTnEEE bit = 1.

(b) TMTn control register 1 (TTnCTL1)



(c) TMTn I/O control register 1 (TTnIOC1)



Note In the case of TMT2 and TMT3, specify “No edge detection” as the valid edge of the external input signal not being used.

(5) D/A converter

The D/A converter is connected between AV_{DD2} and AV_{SS2} and generates a voltage to be compared with an input analog signal.

(6) ANI2n pin

The ANI2n pin is an analog input pin for A/D converter 2. This pin inputs the analog signals to be A/D converted. Pins other than the one that is selected by the AD2S register as analog signal input pins can be used as input port pins.

Cautions 1. Make sure that the voltages input to the ANI2n pin do not exceed the rated values. If a voltage higher than or equal to AV_{DD2} or lower than or equal to AV_{SS2} is input to a channel, the conversion value of the channel is undefined, and the conversion values of the other channels may also be affected.

2. The analog input pin (ANI2n) is alternately used as input port pin (P7n). If an instruction to input a signal to port 7 is executed during conversion when one of ANI2n is selected for A/D conversion, the resolution for conversion may drop.

(7) AV_{DD2} pin

The AV_{DD2} pin alternately functions as the pin for inputting the positive power supply and reference voltage of A/D converter 2. This pin converts signals input to the ANI2n pin to digital signals based on the voltage applied between AV_{DD2} and AV_{SS2}.

Always make the potential at this pin the same as that at the EV_{DD0}, EV_{DD1}, EV_{DD2}, and EV_{DD3} pins (V850E/IH4 only) even when A/D converter 2 is not used.

The operating voltage range of the AV_{DD2} pin is $EV_{DD0} = EV_{DD1} = EV_{DD2} = EV_{DD3}$ (V850E/IH4 only) = AV_{DD2} = 4.0 to 5.5 V.

(8) AV_{SS2} pin

This is the ground pin of A/D converter 2. Always make the potential at this pin the same as that at the EV_{SS0}, EV_{SS1}, EV_{SS2}, EV_{SS3} (V850E/IH4 only) and EV_{SS4} (V850E/IH4 only) pins even when A/D converter 2 is not used.

Remark n = 0 to 11

CHAPTER 16 CLOCKED SERIAL INTERFACE F (CSIF)

16.1 Features

- Transfer rate: 6.25 Mbps (using internal clock)
- Master mode and slave mode selectable
- Interrupt request signals: 3
  - Reception end interrupt request signal (INTCFnR): This signal is generated when reception is enabled and receive data is transferred from the shift register to the CSIFn receive data register (CFnRX) after completion of a serial transfer.
  - Transmission enable interrupt request signal (INTCFnT): This signal is generated when transmission is enabled in the continuous transmission or continuous transmission/reception mode and transmission data is transferred from the CSIFn transmit data register (CFnTX) to the shift register.
  - Reception error interrupt request signal (INTCFnRE): This signal is generated if an overrun error occurs (CFnSTR.CFnOVE bit = 1) when reception is enabled in the continuous transfer mode.
- Serial clock and data phase switchable
- 3-wire serial interface, transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire transfer SOFn: Serial data output
  SIFn: Serial data input
  $\overline{\text{SCK}}$Fn: Serial clock I/O

  Transmission mode, reception mode, and transmission/reception mode specifiable
- Double buffer for both transmission and reception
- Overrun error detection

Remark n = 0 to 2

17.7 I²C Interrupt Request Signals (INTIIC)

The following shows the value of the IICS0 register at the INTIIC interrupt request signal generation timing and at the INTIIC signal timing.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

CHAPTER 18 DMA (DMA CONTROLLER)

The V850E/IG4 and V850E/IH4 include a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer.

The DMAC controls data transfer between the internal RAM and on-chip peripheral I/O based on interrupt requests issued by the peripheral I/O (serial interface, timer, A/D converter, interrupts from an external input pin), or DMA transfer requests triggered by software.

18.1 Features

- 7 independent DMA channels
- Transfer unit: 8/16/32 bits
- Maximum transfer count: 4096
- Transfer type: Two-cycle transfer
- Two transfer modes
  - Single transfer mode
  - Single-step transfer mode
- Transfer request
  - Request by interrupts from on-chip peripheral I/O (serial interface, timer, A/D converter) or interrupts from an external input pin
  - Requests triggered by software
- Transfer sources and destinations
  - Internal RAM ↔ on-chip peripheral I/O
- Next address setting function

19.3.2 Return processing

Execution is returned from non-maskable interrupt servicing by using the RETI instruction.

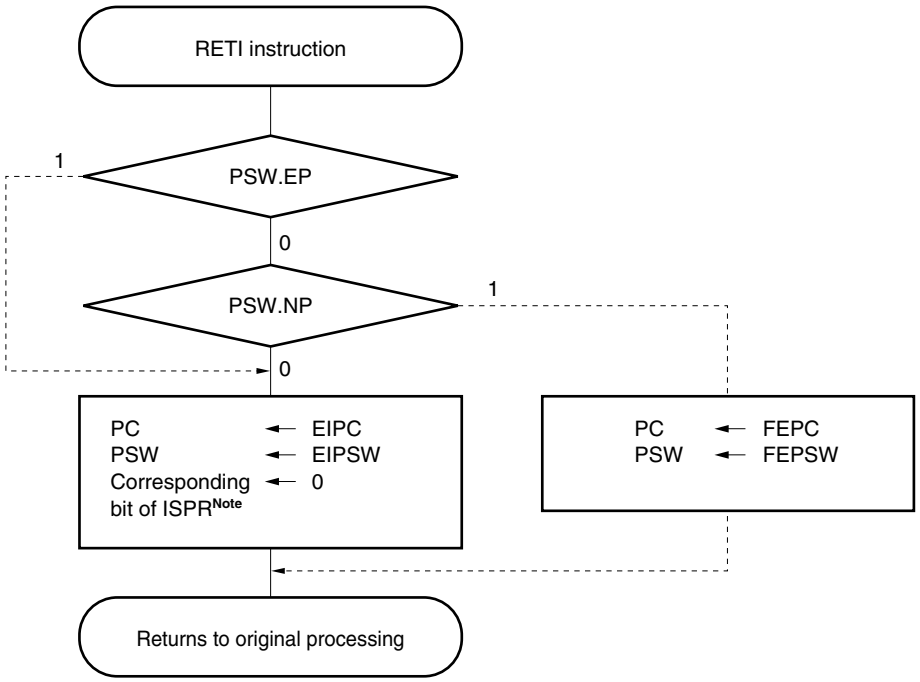
When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the return PC.

<1> Loads the values of the PC and the PSW from EIPC and EIPSW, respectively, because the PSW.EP bit is 0 and the PSW.NP bit is 0.

<2> Transfers control back to the address of the return PC and PSW.

The processing of the RETI instruction is shown below.

Figure 19-5. RETI Instruction Processing



Note For the ISPR register, see **19.3.6 In-service priority register (ISPR)**.

Caution **When the EP and NP bits are changed by the LDSR instruction during non-maskable interrupt servicing, to restore the PC and PSW correctly when returning by using the RETI instruction, the EP bit must be cleared (= 0) and the NP bit must be set (= 1) using the LDSR instruction immediately before the RETI instruction.**

Remark The solid line shows the CPU processing flow.

(2) Releasing HALT mode by $\overline{\text{RESET}}$ pin input or by WDTRES, LVIRES, or POCRES signal generation

The same operation as the normal reset operation is performed.

Table 20-3. Operation Status in HALT Mode

Setting of HALT Mode / Item		Operation Status
Clock generator, PLL		Operates
System clock (f_{XX})		Supply
CPU		Stops operation
DMA		Operable
Interrupt controller		Operable
Timer	TAA0 to TAA2	Operable
	TAB0, TAB1	Operable
	TMT0 to TMT3	Operable
	TMM0 to TMM3	Operable
Watchdog timer		Operable
Serial interface	CSIF0 to CSIF2	Operable
	UARTA0 to UARTA2	Operable
	UARTB	Operable
	I^2C	Operable
A/D converters 0 to 2		Operable
Clock monitor		Operable
Low-voltage detector		Operable
Power-on-clear circuit		Operable
Port function		Retains status before HALT mode was set.
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the HALT mode was set.

21.2 Control Register

(1) Reset source flag register (RESF)

The RESF register is an 8-bit register that indicates occurrence of a reset request from the watchdog timer (WDT) or low-voltage detector (LVI).

The WDTRF or LVIRF bit of this register is set to 1 when the internal reset source signal from WDT or LVI is asserted. The WDTRF or LVIRF bit is cleared by a reset signal (the one generated by inputting the $\overline{\text{RESET}}$ pin, the POCRES signal generated by the power-on-clear circuit (POC), or the forced reset signal generated by the on-chip debug function), a bit manipulation instruction, or a store instruction (writing 0 to the WDTRF or LVIRF bit).

The RESF register is a special register and can be written only in a combination of specific sequences (see **3.4.8 Special registers**).

This register can be read or written in 8-bit or 1-bit units. However, bits 0 and 4 can only be cleared (0) by writing.

This register is set to 00H by $\overline{\text{RESET}}$ pin input and reset by the power-on-clear circuit (POC). This register is set to 00H by RESET pin input, a reset by the power-on-clear circuit (POC), or a forced reset by the on-chip debug function. For details on reset conflict, see **Cautions** on the next page.

CHAPTER 23 POWER-ON CLEAR CIRCUIT

23.1 Function

Functions of the power-on-clear circuit (POC) are shown below.

- Generates a reset signal (POCRES) upon power application.
- Compares the supply voltage (V850E/IG4: EV_{DD0}, EV_{DD1}, EV_{DD2}, V850E/IH4: FV_{DD}) and detection voltage (V_{POC0}), and generates a reset signal when the supply voltage drops below the detection voltage (detection voltage (V_{POC0}): 3.7 V ±0.2 V).

Remark The V850E/IG4 and V850E/IH4 have the reset source flag register (RESF) that indicates generation of a reset signal (WDTRES) by watchdog timer overflow and a reset signal (LVIRES) by low-voltage detector (LVI).
The RESF register is not cleared to 00H when a reset signal (WDTRES or LVIRES) is generated, and its flag corresponding to the reset source is set to 1.
The RESF register is cleared (00H) when a reset signal (POCRES) by power-on-clear circuit (POC) is generated.
For details of the RESF register, see **CHAPTER 21 RESET FUNCTIONS**.

(7/16)

Symbol	Name	Unit	Page
DSAR2	DMA source address register 2	DMAC	954
DSAR2H	DMA source address register 2H	DMAC	954
DSAR2L	DMA source address register 2L	DMAC	954
DSAR3	DMA source address register 3	DMAC	954
DSAR3H	DMA source address register 3H	DMAC	954
DSAR3L	DMA source address register 3L	DMAC	954
DSAR4	DMA source address register 4	DMAC	954
DSAR4H	DMA source address register 4H	DMAC	954
DSAR4L	DMA source address register 4L	DMAC	954
DSAR5	DMA source address register 5	DMAC	954
DSAR5H	DMA source address register 5H	DMAC	954
DSAR5L	DMA source address register 5L	DMAC	954
DSAR6	DMA source address register 6	DMAC	954
DSAR6H	DMA source address register 6H	DMAC	954
DSAR6L	DMA source address register 6L	DMAC	954
DTCR0	DMA transfer times specification register 0	DMAC	957
DTCR1	DMA transfer times specification register 1	DMAC	957
DTCR2	DMA transfer times specification register 2	DMAC	957
DTCR3	DMA transfer times specification register 3	DMAC	957
DTCR4	DMA transfer times specification register 4	DMAC	957
DTCR5	DMA transfer times specification register 5	DMAC	957
DTCR6	DMA transfer times specification register 6	DMAC	957
DTFR0	DMA trigger factor register 0	DMAC	965
DTFR0H	DMA trigger factor register 0H	DMAC	965
DTFR0L	DMA trigger factor register 0L	DMAC	965
DTFR1	DMA trigger factor register 1	DMAC	965
DTFR1H	DMA trigger factor register 1H	DMAC	965
DTFR1L	DMA trigger factor register 1L	DMAC	965
DTFR2	DMA trigger factor register 2	DMAC	965
DTFR2H	DMA trigger factor register 2H	DMAC	965
DTFR2L	DMA trigger factor register 2L	DMAC	965
DTFR3	DMA trigger factor register 3	DMAC	965
DTFR3H	DMA trigger factor register 3H	DMAC	965
DTFR3L	DMA trigger factor register 3L	DMAC	965
DTFR4	DMA trigger factor register 4	DMAC	965
DTFR4H	DMA trigger factor register 4H	DMAC	965
DTFR4L	DMA trigger factor register 4L	DMAC	965
DTFR5	DMA trigger factor register 5	DMAC	965
DTFR5H	DMA trigger factor register 5H	DMAC	965
DTFR5L	DMA trigger factor register 5L	DMAC	965
DTFR6	DMA trigger factor register 6	DMAC	965
DTFR6H	DMA trigger factor register 6H	DMAC	965
DTFR6L	DMA trigger factor register 6L	DMAC	965
HZA0CTL0	High-impedance output control register 00	Timer	571

(3/6)

Mnemonic	Operand	Opcode	Operation		Execution Clock			Flags				
					i	r	l	CY	OV	S	Z	SAT
LD.H	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Halfword))		1	1	Note 11					
LDSR	reg2,regID	rrrrr111111RRRRR 0000000000100000 **Note 12**	SR[regID]←GR[reg2]	Other than regID = PSW	1	1	1					
				regID = PSW	1	1	1	×	×	×	×	×
LD.HU	disp16[reg1],reg2	rrrrr111111RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Halfword)		1	1	Note 11					
LD.W	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr,Word)		1	1	Note 11					
MOV	reg1,reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]		1	1	1					
	imm5,reg2	r r r r r 0 1 0 0 0 0 i i i i i	GR[reg2]←sign-extend(imm5)		1	1	1					
	imm32,reg1	00000110001RRRRR i i i i i i i i i i i i i i i i l l l l l l l l l l l l l l l l	GR[reg1]←imm32		2	2	2					
MOVEA	imm16,reg1,reg2	rrrrr110001RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1					
MOVHI	imm16,reg1,reg2	rrrrr110010RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+(imm16 ll 0^{16})		1	1	1					
MUL Note 22	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100000	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	2 Note 14	2					
	imm9,reg2,reg3	r r r r r 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 l l l l 0 0 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xsign-extend(imm9)		1	2 Note 14	2					
MULH	reg1,reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2] Note 6 xGR[reg1] Note 6		1	1	2					
	imm5,reg2	r r r r r 0 1 0 1 1 1 i i i i i	GR[reg2]←GR[reg2] Note 6 xsign-extend(imm5)		1	1	2					
MULHI	imm16,reg1,reg2	rrrrr110111RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] Note 6 ximm16		1	1	2					
MULU Note 22	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100010	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	2 Note 14	2					
	imm9,reg2,reg3	r r r r r 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 l l l l 1 0 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xzero-extend(imm9)		1	2 Note 14	2					
NOP		0000000000000000	Pass at least one clock cycle doing nothing.		1	1	1					
NOT	reg1,reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])		1	1	1		0	×	×	
NOT1	bit#3,disp16[reg1]	01bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100010	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	