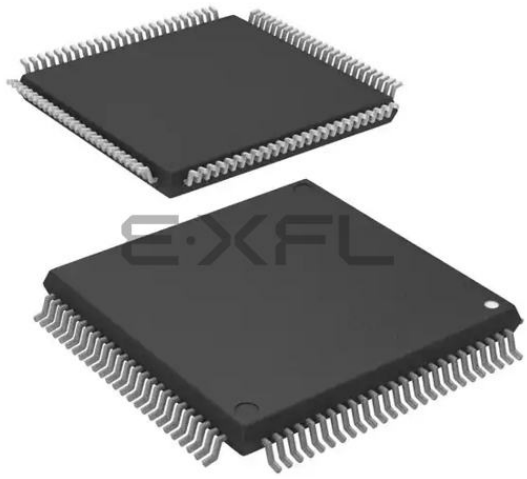


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3914gc-r-ueu-ax

CHAPTER 1 INTRODUCTION

The V850E/IG4 and V850E/IH4 are products of the Renesas Electronics V850 single-chip microcontrollers. This chapter gives an outline of the V850E/IG4 and V850E/IH4.

1.1 Overview

The V850E/IG4 and V850E/IH4 are 32-bit single-chip microcontrollers that use the V850E1 CPU core and incorporate ROM/RAM and various peripheral functions such as DMA controller, timer/counter, watchdog timer, serial interfaces, A/D converter, and on-chip debug function.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850E/IG4 and V850E/IH4 feature instructions such as multiply instructions realized by a hardware multiplier, saturated operation instructions, and bit manipulation instructions, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850E/IG4 and V850E/IH4 enable an extremely high cost-performance for applications such as motor inverter control.

Table 1-1 lists the V850E/IG4 and V850E/IH4 products.

Table 1-1. V850E/IG4, V850E/IH4 Product List

Function / Part Number		Package	ROM		RAM Size	Operating Frequency (MAX.)	Maskable Interrupt		Non-Maskable Interrupt
			Type	Size			External	Internal	
V850E/IG4	μPD70F3913	100GC/100GF	Flash memory	256 KB	24 KB	100 MHz	22	81	1
	μPD70F3914			384 KB					
	μPD70F3915			480 KB					
V850E/IH4	μPD70F3916	128GF		256 KB					
	μPD70F3917			384 KB					
	μPD70F3918			480 KB					

Remark 100GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
100GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
128GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

(f) Settings of alternate functions of port 4

PFC43	Specification of Alternate Function of P43 Pin
0	INTP13 input
1	TOA11 output

PFCE42	Specification of Alternate Function of P42 Pin
0	$\overline{\text{SCKF0}}$ input/output
1	TOA10 output

PFC41	Specification of Alternate Function of P41 Pin
0	SOF0 output
1	TXDA0 output

PFCE40	PFC40	Specification of Alternate Function of P40 Pin
0	0	SIF0 input
0	1	RXDA0 input
1	0	Setting prohibited
1	1	TOA00 output

(g) Pull-up resistor option register 4 (PU4)

After reset: 00H R/W Address: FFFFFC48H

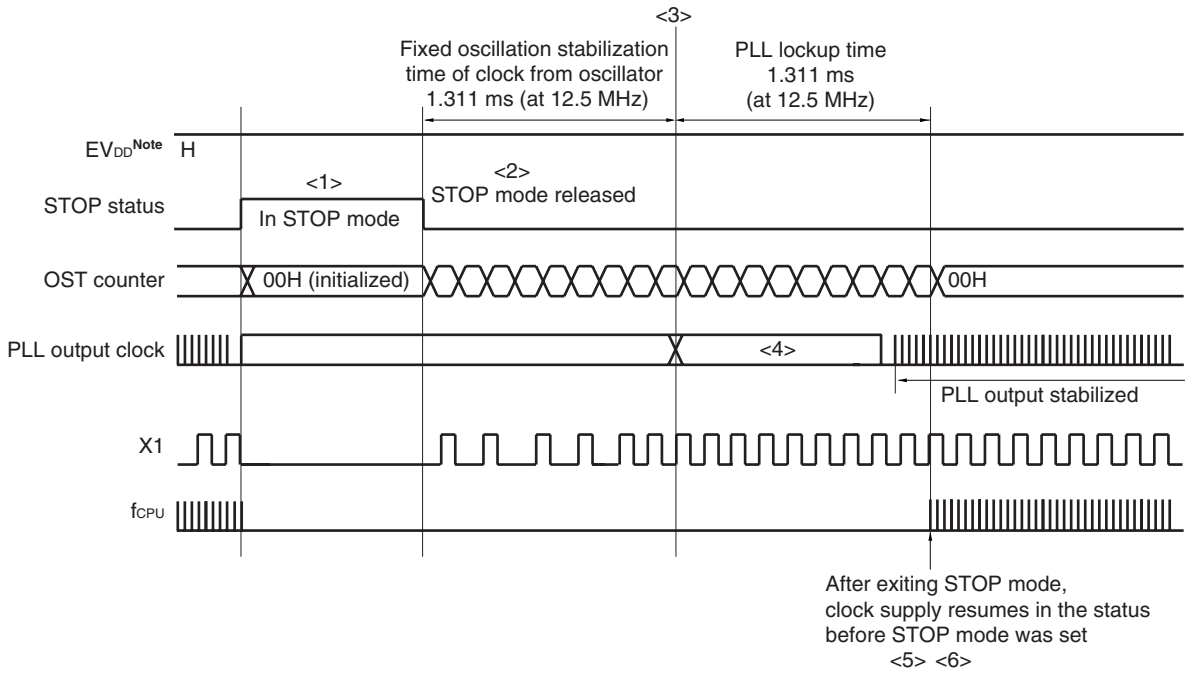
	7	6	5	4	3	2	1	0
PU4	0	0	0	PU44	PU43	PU42	PU41	PU40

PU4n	Control of on-chip pull-up resistor connection
0	Do not connect
1	Connect[Note]

Note An on-chip pull-up resistor can be connected only when the pins are in input mode in the port mode or when the pins function as input pins in the alternate-function mode (including the $\overline{\text{SCKF0}}$ pin in the slave mode). An on-chip pull-up resistor cannot be connected when the pins are in output mode.

Remark n = 0 to 4

(3) When releasing STOP mode by interrupt request



<1> When the STOP mode is set, both the oscillator and PLL stop.
At this time, PLL is stopped in the STOP mode. The OST counter is initialized.

<2> When the STOP mode is released, the oscillator is activated and the OST counter starts counting the oscillation stabilization time. At this time, PLL remains stopped.

<3> When a fixed oscillation stabilization time (1.311 ms) has elapsed, PLL starts operating. The clock generated by the oscillator must be stabilized before PLL starts operating. The actual oscillation stabilization time is “fixed oscillation stabilization time”. Take this into consideration when setting a value to the OSTS register.

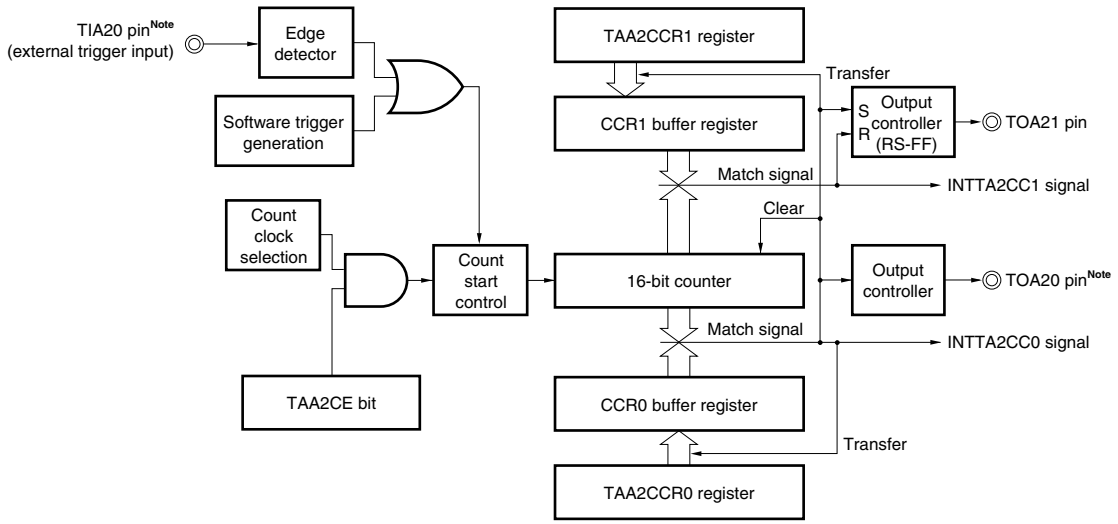
<4> After a fixed oscillation stabilization time (1.311 ms) has elapsed, the lockup wait time starts. The remaining count time of the OST counter is the lockup wait time.

<5> When the lockup time of PLL is over, clock supply to the internal circuitry resumes in the status before the STOP mode was set.

<6> The operation to be performed when the STOP mode is released by a reset signal ($\overline{\text{RESET}}$ pin input, reset signal (LVIRES) generation by the low-voltage detector (LVI), reset signal (POCRES) generation by the power-on-clear circuit (POC)) is the same as that in **(1) Power on (power-on reset)** and **(2) Reset input with power on**.

Note V850E/IG4: EV_{DD0}, EV_{DD1}, EV_{DD2}
V850E/IH4: EV_{DD0}, EV_{DD1}, EV_{DD2}, EV_{DD3}

Figure 6-23. Configuration of TAA2 in External Trigger Pulse Output Mode

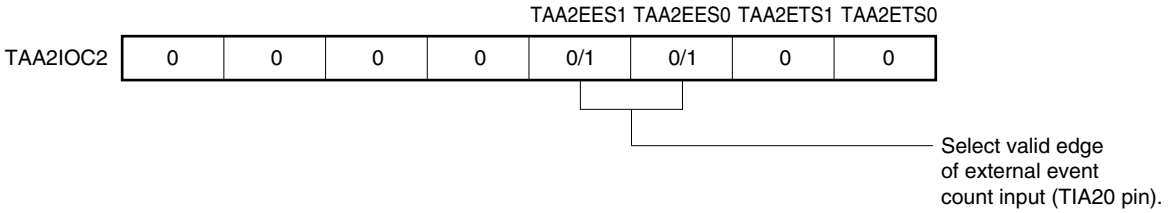


Note Because the external trigger input pin (TIA20) and timer output pin (TOA20) are the same pin, the two functions cannot be used at the same time.

Caution In the external trigger pulse output mode, select the internal clock as the count clock (by clearing the TAA2CTL1.TAA2EEE bit to 0).

Figure 6-35. Register Setting in PWM Output Mode (2/2)

(d) TAA2 I/O control register 2 (TAA2IOC2)



(e) TAAn counter read buffer register (TAAnCNT)

The value of the 16-bit counter can be read by reading the TAAnCNT register.

(f) TAAn capture/compare registers 0 and 1 (TAAnCCR0 and TAAnCCR1)

If D_0 is set to the TAAnCCR0 register and D_1 to the TAAnCCR1 register, the cycle and active level of the PWM waveform are as follows.

Cycle = (D_0 + 1) × Count clock cycle

Active level width = D_1 × Count clock cycle

Remarks 1. TAA2 I/O control register 1 (TAA2IOC1) and TAAn option register 0 (TAAnOPT0) are not used in the PWM output mode.

2. n = 0 to 2

a = 0, 1

(b) Batch write

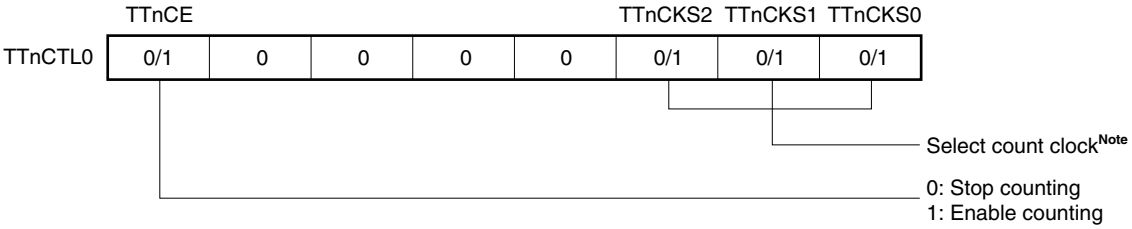
In this mode, data is transferred all at once from the TTnCCR0 and TTnCCR1 registers to the CCR0 and CCR1 buffer registers during timer operation. This data is transferred upon a match between the value of the CCR0 buffer register and the value of the 16-bit counter. Transfer is enabled by writing to the TTnCCR1 register. Whether to enable or disable the next transfer timing is controlled by writing or not writing to the TTnCCR1 register.

In order for the set value when the TTnCCR0 and TTnCCR1 registers are rewritten to become the 16-bit counter comparison value (in other words, in order for this value to be transferred to the CCR0 and CCR1 buffer registers), it is necessary to rewrite the TTnCCR0 register and then write to the TTnCCR1 register before the 16-bit counter value and the CCR0 buffer register value match. Therefore, the values of the TTnCCR0 and TTnCCR1 registers are transferred to the CCR0 and CCR1 buffer registers upon a match between the count value of the 16-bit counter and the value of the CCR0 buffer register. Thus even when wishing only to rewrite the value of the TTnCCR0 register, also write the same value (same as preset value of the TTnCCR1 register) to the TTnCCR1 register.

Remark n = 0 to 3

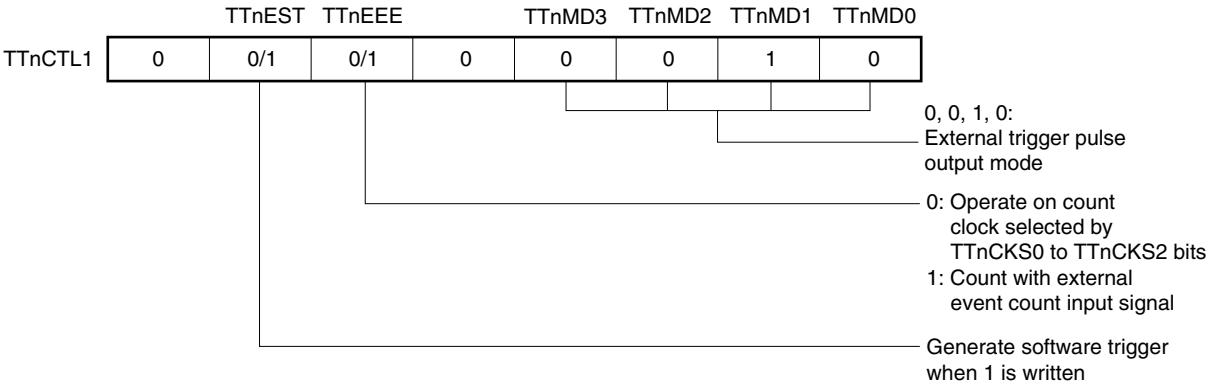
Figure 8-25. Setting of Registers in External Trigger Pulse Output Mode (1/2)

(a) TMTn control register 0 (TTnTL0)

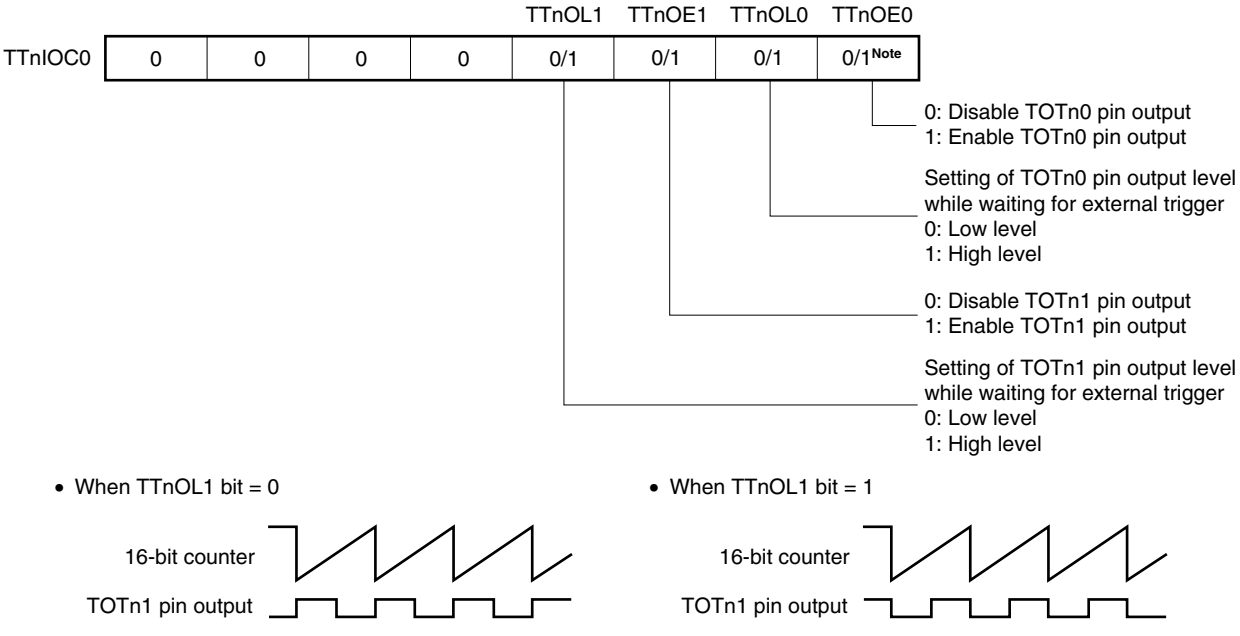


Note The setting is invalid when the TTnCTL1.TTnEEE bit = 1.

(b) TMTn control register 1 (TTnCTL1)



(c) TMTn I/O control register 0 (TTnIOC0)

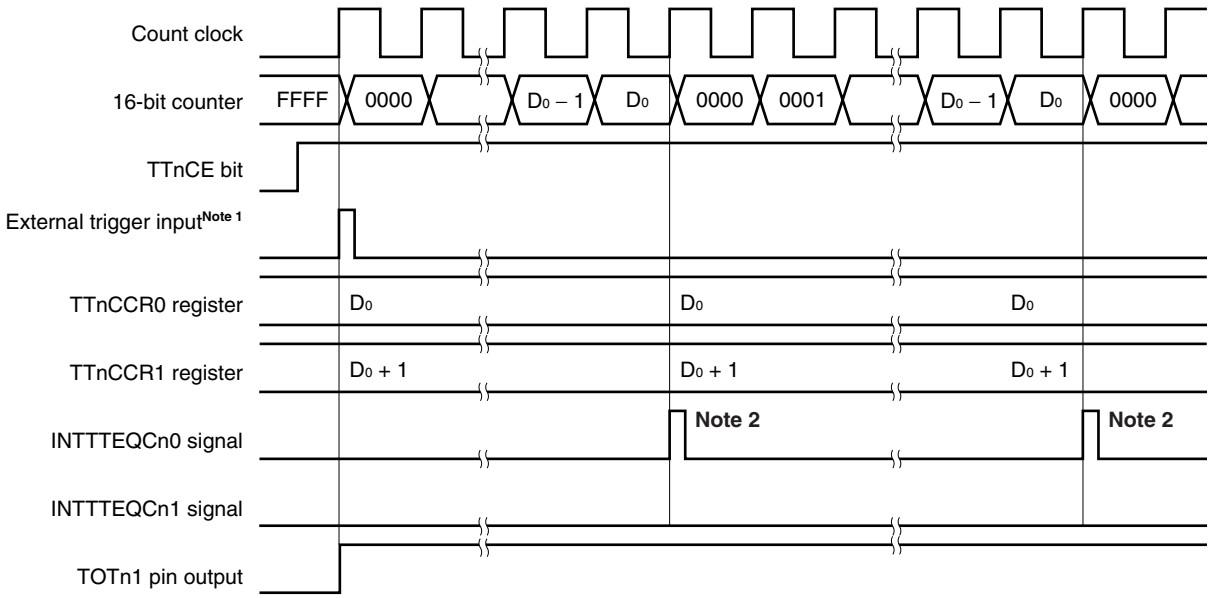


- When TTnOL1 bit = 0

- When TTnOL1 bit = 1

Note Set this bit to 0 when not using the TOTn0 pin in the external trigger pulse output mode.

To output a 100% waveform, set a value of (set value of TTnCCR0 register + 1) to the TTnCCR1 register. If the set value of the TTnCCR0 register is FFFFH, 100% output cannot be produced.



Notes 1. TMT0 and TMT1: EVTTm pin input
TMT2 and TMT3: TITk0 pin input

2. The timing is actually delayed by one operating clock (fxx).

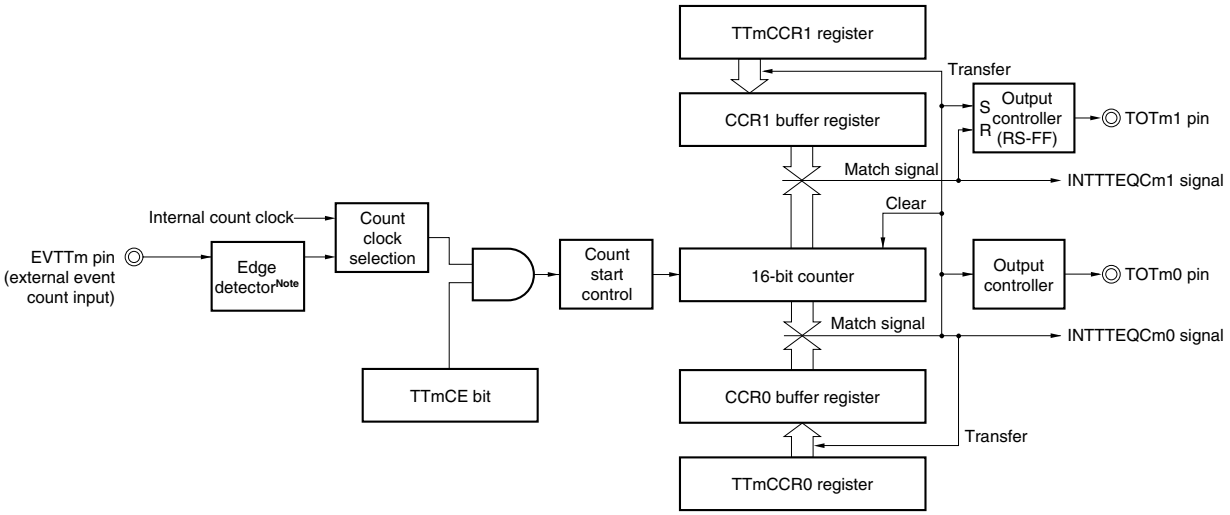
Remark n = 0 to 3
m = 0, 1
k = 2, 3

8.6.8 Triangular-wave PWM output mode (TTnMD3 to TTnMD0 bits = 0111)

In the triangular-wave PWM output mode, a triangular-wave PWM waveform is output from the TOTn1 pin when the TTnCTL0.TTnCE bit is set to 1.

An inverted PWM waveform is output from the TOTn0 pin when the count value of the 16-bit counter matches the value of the CCR0 buffer register and when the 16-bit counter is set to 0000H.

Figure 8-49. Configuration of TMT0 and TMT1 in Triangular-Wave PWM Output Mode



Note Set by the TTmIOC2.TTmEES1 and TTmIOC2.TTmEES0 bits.

Remark m = 0 to 3

When the 16-bit counter starts operating (TTmCE bit = 0 → 1), the set value of the TTmTCW register is transferred to the counter and the 16-bit counter starts operating.

When the count value of the counter matches the value of the CCR0 buffer register, the compare match interrupt request signal (INTTTEQCm0) is generated. Because the TTmECM0 bit = 1, the 16-bit counter is cleared to 0000H if the next count operation is counting up.

When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the compare match interrupt request signal (INTTTEQCm1) is generated. Because the TTmECM1 bit = 0, the 16-bit counter is not cleared to 0000H when its value matches that of the CCR1 buffer register.

When the TTmLDE bit = 1 and TTmECM0 bit = 1, the counter can operate in a range from 0000H to the set value of the TTmCCR0 register.

12.4.6 Operation of multiple channel conversion

The signals of two or more analog input pins (ANInk) specified by the ADnCHEN register are converted. The signals are sequentially converted starting from the pin with the lowest number (in the example in Figure 12-13, ANI00 → ANI02 → ANI03). An analog input pin that is not specified is skipped. The result of conversion is stored in the ADnCRk register corresponding to the ANInk pin. The ANInk pin and ADnCRk register correspond to each other on a one-to-one basis. When conversion of the signal of the specified analog input pins is completed, an A/Dn conversion end interrupt request signal (INTADn) is generated.

After completion of A/D conversion, the conversion operation is stopped in the A/D trigger mode or A/D trigger polling mode. In the hardware trigger mode, the A/D converter waits for a trigger.

Remark A/D converter 0: n = 0
k = 0 to 3, 5 to 7
A/D converter 1: n = 1
V850E/IG4: k = 0 to 2, 5 to 7
V850E/IH4: k = 0 to 3, 5 to 7

Cautions 1. If there is noise at the analog input pin (ANI2n) and at the A/D converter power supply voltage pin (AV_{DD2}), that noise may generate an illegal conversion result.
Software processing will be needed to avoid a negative effect on the system from this illegal conversion result.
An example of this software processing is shown below.
- **Take the average result of a number of A/D conversions and use that as the A/D conversion result.**
- **Execute a number of A/D conversions successively and use those results, omitting any exceptional results that may have been obtained.**
- **If an A/D conversion result that is judged to have generated a system malfunction is obtained, be sure to recheck the system malfunction before performing malfunction processing.**

2. Do not apply a voltage outside the AV_{SS2} to AV_{DD2} range to the pins that are used as input pins of A/D converter 2.

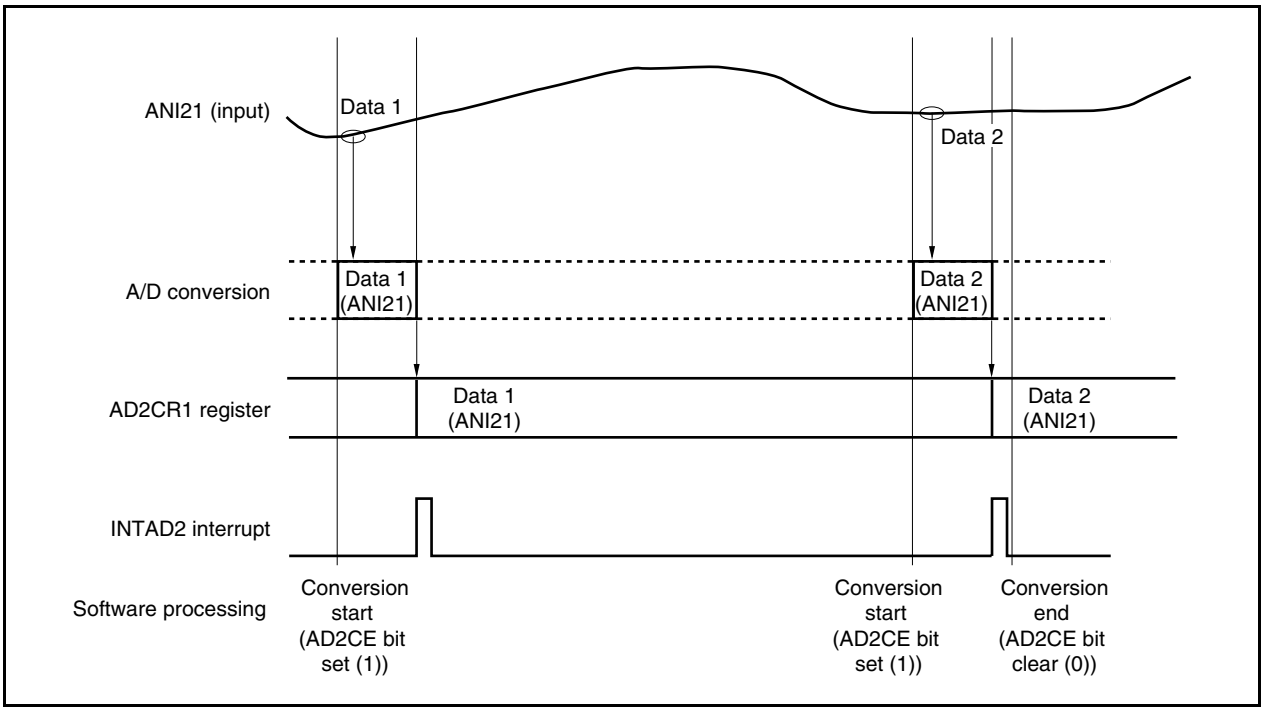
(3) One-shot select mode

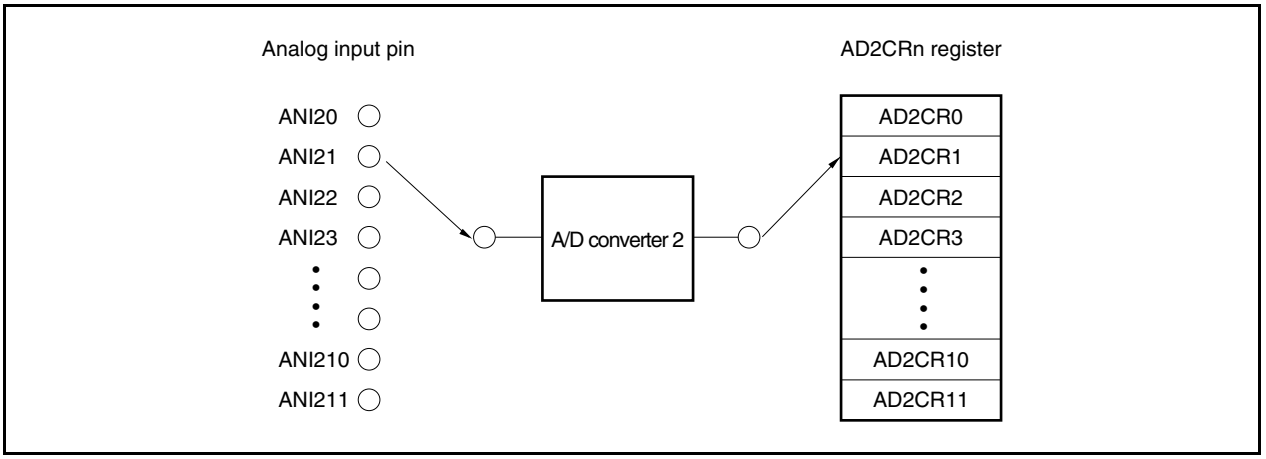
In this mode, the analog input pin (ANI2n) specified by the AD2S register is A/D-converted once. The conversion result is stored in the AD2CRn register corresponding to the ANI2n pin. The ANI2n pin and the AD2CRn register correspond one to one, and an A/D2 conversion end interrupt request signal (INTAD2) is generated each time one A/D conversion ends.

After A/D conversion ends, the conversion operation is stopped.

Remark n = 0 to 11

Figure 13-6. One-Shot Select Mode Operation Timing
(When AD2M0.AD2MD1 and AD2M0.AD2MD0 Bits = 10, AD2S.AD2S3 to AD2S.AD2S0 Bits = 0001)





16.3 Mode Switching Between CSIF and Other Serial Interface

16.3.1 Mode switching between CSIF0 and UARTA0

In the V850E/IG4 and V850E/IH4, CSIF0 and UARTA0 share a pin, and these functions cannot be used at the same time. To use the pin for the CSIF0 function, set up the PMC4, PFC4, and PFCE4 registers in advance.

Switching the operation mode between CSIF0 and UARTA0, the serial interfaces, is described below.

Caution The operations related to transmission and reception of CSIF0 or UARTA0 are not guaranteed if the operation mode is switched during transmission or reception. Be sure to disable the unit that is not used.

Figure 16-2. Operation Mode Switch Settings of CSIF0 and UARTA0

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	PMC44	PMC43	PMC42	PMC41	PMC40

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	0	0	0	0	PFC43	0	PFC41	PFC40

After reset: 00H R/W Address: FFFFF708H

	7	6	5	4	3	2	1	0
PFCE4	0	0	0	0	0	PFCE42	0	PFCE40

PMC42	PFCE42	Operation mode
0	×	Port I/O mode
1	0	$\overline{\text{SCKF0}}$

PMC4n	PFC4n	Operation mode
0	×	Port I/O mode
1	0	CSIF0 mode
1	1	UARTA0 mode

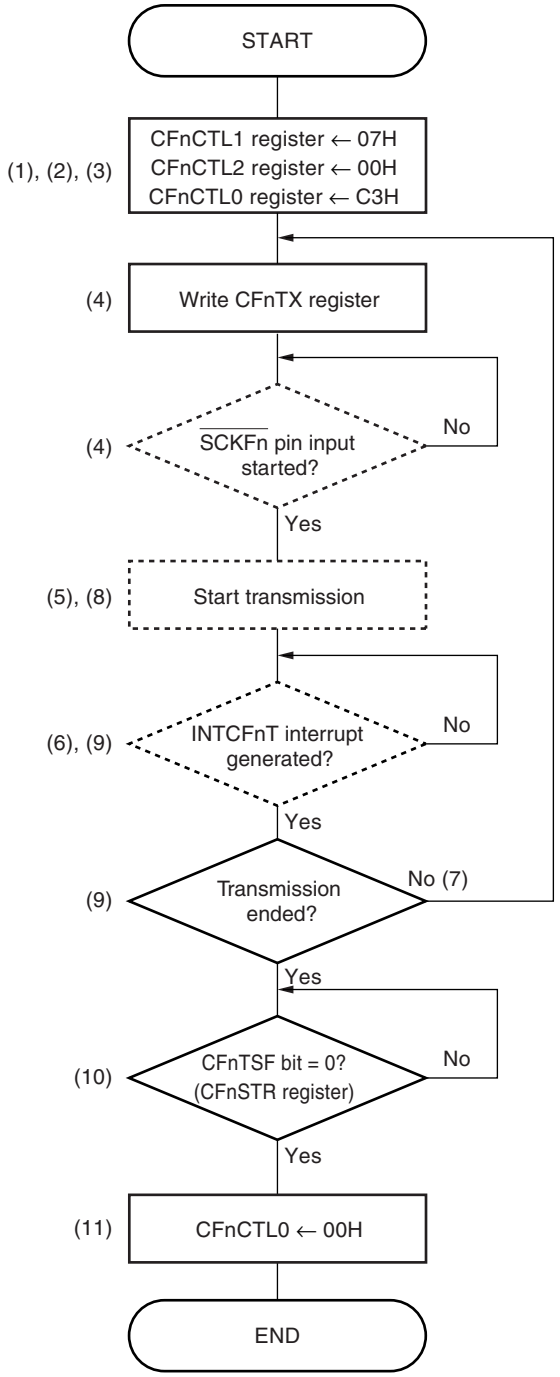
Remarks 1. n = 0, 1

2. × = 0 or 1

16.5.10 Continuous transfer mode (slave mode, transmission mode)

MSB first (CFnCTL0.CFnDIR bit = 0), communication type 1 (CFnCTL1.CFnCKP and CFnCTL1.CFnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKFn}$) (CFnCTL1.CFnCKS2 to CFnCTL1.CFnCKS0 bits = 111), transfer data length = 8 bits (CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits = 0000)

(1) Operation flow



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

3. n = 0 to 2

Figure 17-19. Slave Operation Flowchart (1)

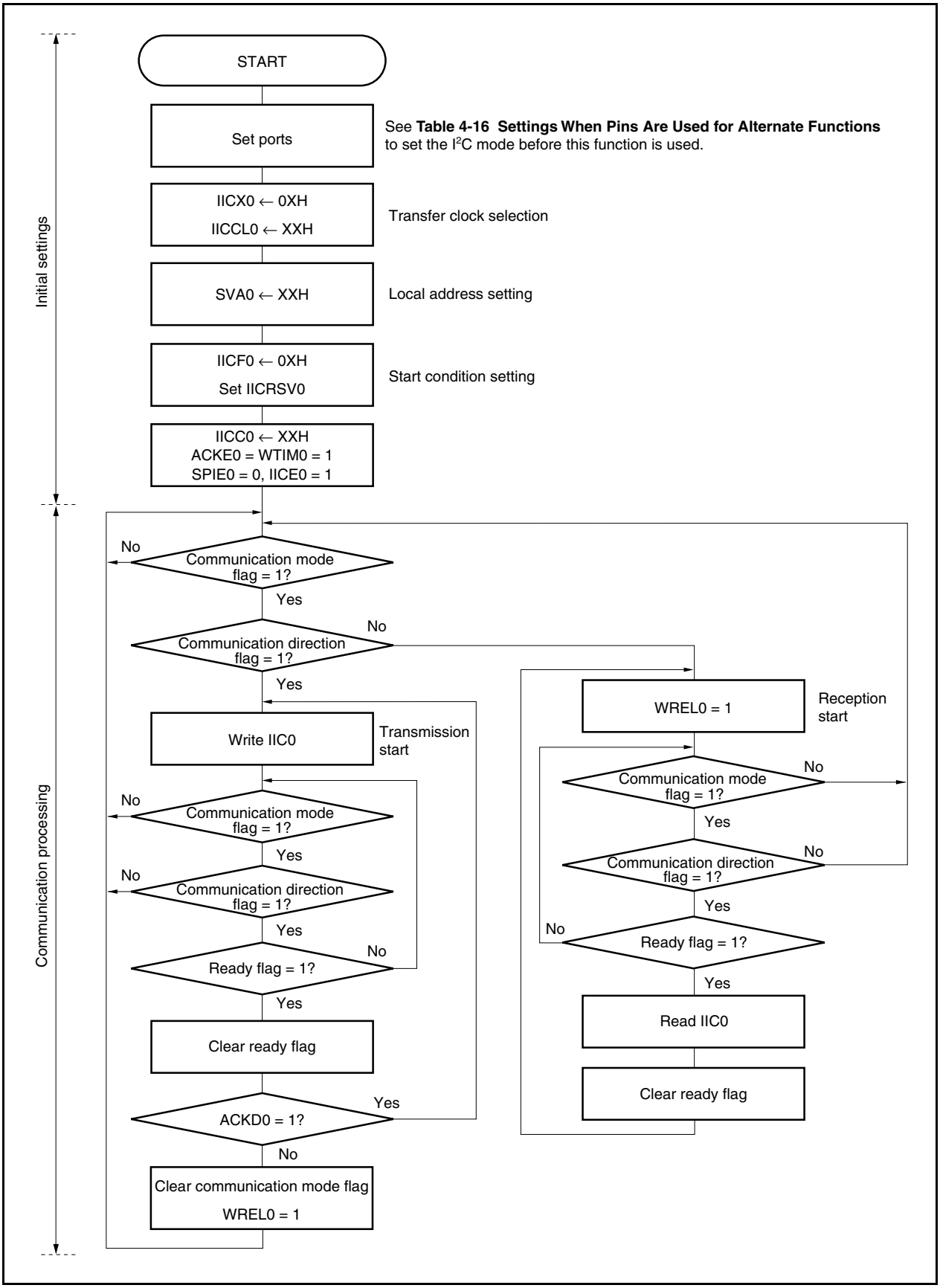
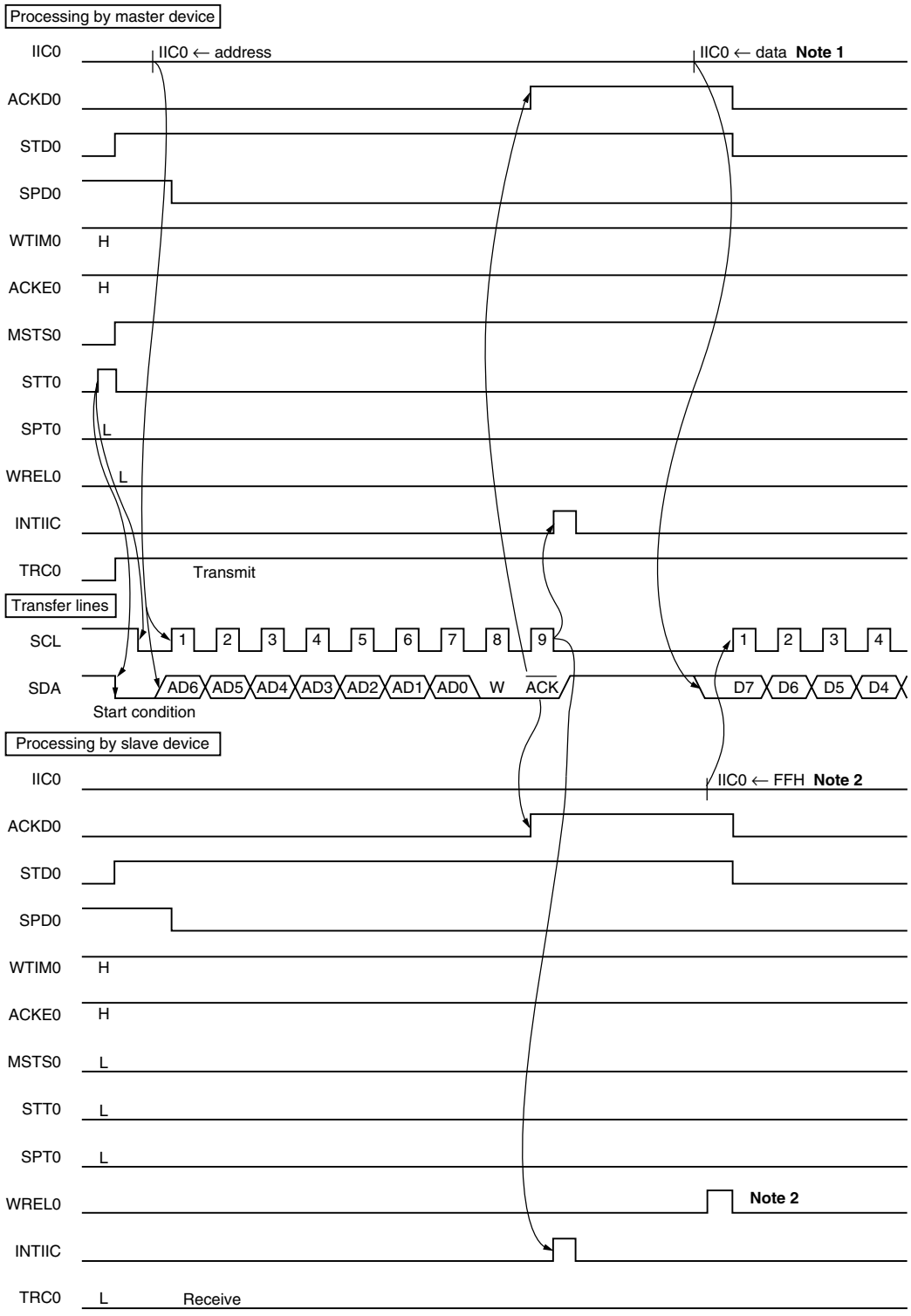


Figure 17-21. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Notes 1. Cancel waits during master transmission by writing data to IIC0, not by setting WREL0.

2. To cancel slave wait, write FFH to IIC0 or set WREL0.

(7) Registers that must not be set under certain conditions

The following registers must not be written to when a specific operation is performed. If these registers are written to, the operation cannot be guaranteed.

Status	Register That Must Not Be Set
Stop (ENn/ENnn bit = 0)	None
During operation (ENn/ENnn bit = 1)	DADCn[Note 1], DTFRn
During suspension[Note 2] (STPn/STPnn bit = 1)	DADCn[Note 1], DTFRn

Notes 1. The same value may be written to the register.

2. Setting the register is prohibited when the operation that was suspended is resumed. The register can be set when the operation is stopped (ENn/ENnn bit = 0) after the register is written.

Remark n = 0 to 6

24.2.4 Cautions

(1) If a reset signal is input (from the target system or due to the execution of an internal reset) while the program is running, the software breaks specified for the on-chip flash memory area will no longer occur. Use hardware breaks to avoid this problem. The disabled software breaks can be enabled again by generating a forcible break or a hardware break.

(2) Pin reset during a break is masked and the CPU and peripheral I/O are not reset. If pin reset or internal reset is generated as soon as the flash memory is rewritten by DMA or read by the RAM monitor function while the user program is being executed, the CPU and peripheral I/O may not be correctly reset.

(3) In the on-chip debug mode, the DDO pin is forcibly set to the high-level output.

(4) The flash memory of the device used in debugging is rewritten during debugging, so the number of flash memory rewrites cannot be guaranteed. Therefore, do not use the device used in debugging for a mass production product.

(5) Because the DDI and DCK pins function alternately as the CSIF0 I/O pins (SIF0, $\overline{\text{SCKF0}}$), UARTA0 input pin (RXDA0), and TAA output pin (TOA00, TOA10), CSIF0, UARTA0, and TAA0 cannot be used while the on-chip debug function is being used.

(6) When the on-chip debug function is used, the clock generator and PLL continue operating even if the STOP mode is set.

- Security ID setting

  The ID code must be embedded in the area between 0000070H and 0000079H in Figure 24-7, to prevent the memory from being read by an unauthorized person. For details, see **24.4 ROM Security Function**.

(2) Reset vector

A reset vector includes the jump instruction for the debug monitor program.

[How to secure areas]

It is not necessary to secure this area intentionally. When downloading a program, however, the debugger rewrites the reset vector in accordance with the following cases. If the rewritten pattern does not match the following cases, the debugger generates an error (F0c34 when using the ID850QB).

(a) When two nop instructions are placed in succession from address 0

Before rewriting		After rewriting
0x0 nop	→	Jumps to debug monitor program at 0x0
0x2 nop		0x4 xxxx
0x4 xxxx		

(b) When two 0xFFFF are successively placed from address 0 (already erased device)

Before rewriting		After rewriting
0x0 0xFFFF	→	Jumps to debug monitor program at 0x0
0x2 0xFFFF		0x4 xxxx
0x4 xxxx		

(c) The *jr* instruction is placed at address 0 (when using CA850)

Before rewriting		After rewriting
0x0 jr disp22	→	Jumps to debug monitor program at 0x0
		0x4 jr disp22 - 4

(d) *mov32* and *jmp* are placed in succession from address 0 (when using IAR compiler ICCV850)

Before rewriting		After rewriting
0x0 mov imm32,reg1	→	Jumps to debug monitor program at 0x0
0x6 jmp [reg1]		0x4 mov imm32,reg1
		0xa jmp [reg1]

(e) The jump instruction for the debug monitor program is placed at address 0

Before rewriting		After rewriting
Jumps to debug monitor program at 0x0	→	No change