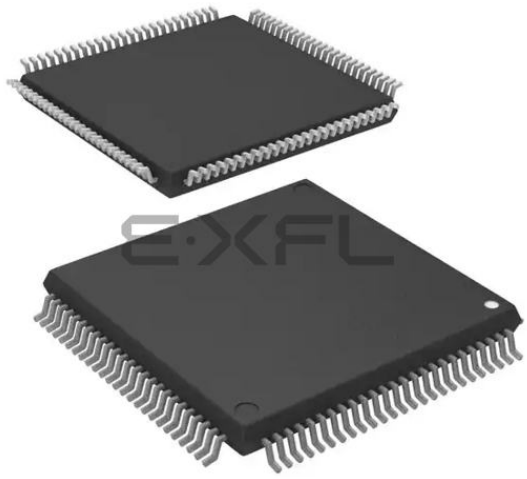
Renesas Electronics America Inc - UPD70F3914GF(R)-GAS-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3914gf-r-gas-ax

(17/18)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1	8	16	
FFFFFD06H	CSIF0 transmit data register	CF0TX	R/W			√	0000H
FFFFFD06H	CSIF0 transmit data register L	CF0TXL			√		00H
FFFFFD10H	CSIF1 control register 0	CF1CTL0		√	√		01H
FFFFFD11H	CSIF1 control register 1	CF1CTL1		√	√		00H
FFFFFD12H	CSIF1 control register 2	CF1CTL2			√		00H
FFFFFD13H	CSIF1 status register	CF1STR		√	√		00H
FFFFFD14H	CSIF1 receive data register	CF1RX	R			√	0000H
FFFFFD14H	CSIF1 receive data register L	CF1RXL			√		00H
FFFFFD16H	CSIF1 transmit data register	CF1TX	R/W			√	0000H
FFFFFD16H	CSIF1 transmit data register L	CF1TXL			√		00H
FFFFFD20H	CSIF2 control register 0	CF2CTL0		√	√		01H
FFFFFD21H	CSIF2 control register 1	CF2CTL1		√	√		00H
FFFFFD22H	CSIF2 control register 2	CF2CTL2			√		00H
FFFFFD23H	CSIF2 status register	CF2STR		√	√		00H
FFFFFD24H	CSIF2 receive data register	CF2RX	R			√	0000H
FFFFFD24H	CSIF2 receive data register L	CF2RXL			√		00H
FFFFFD26H	CSIF2 transmit data register	CF2TX	R/W			√	0000H
FFFFFD26H	CSIF2 transmit data register L	CF2TXL			√		00H
FFFFFD80H	IIC shift register 0	IIC0			√		00H
FFFFFD82H	IIC control register 0	IICC0		√	√		00H
FFFFFD83H	Slave address register 0	SVA0			√		00H
FFFFFD84H	IIC clock select register 0	IICCL0		√	√		00H
FFFFFD85H	IIC function expansion register 0	IICX0		√	√		00H
FFFFFD86H	IIC status register 0	IICS0	R	√	√		00H
FFFFFD8AH	IIC flag register 0	IICF0	R/W	√	√		00H
FFFFFD90H	IIC OPS clock select register	IICOCKS			√		00H
FFFFFE00H	High-impedance output control register 40	HZA4CTL0		√	√		00H
FFFFFE01H	High-impedance output control register 41	HZA4CTL1		√	√		00H
FFFFFE08H	High-impedance output control register 50	HZA5CTL0		√	√		00H
FFFFFE09H	High-impedance output control register 51	HZA5CTL1		√	√		00H
FFFFFE10H	High-impedance output control register 60	HZA6CTL0		√	√		00H
FFFFFE11H	High-impedance output control register 61	HZA6CTL1		√	√		00H
FFFFFE18H	High-impedance output control register 70	HZA7CTL0		√	√		00H
FFFFFE19H	High-impedance output control register 71	HZA7CTL1		√	√		00H
FFFFFE20H	High-impedance output control register 80	HZA8CTL0		√	√		00H
FFFFFE21H	High-impedance output control register 81	HZA8CTL1		√	√		00H
FFFFFE28H	High-impedance output control register 90	HZA9CTL0		√	√		00H
FFFFFE29H	High-impedance output control register 91	HZA9CTL1		√	√		00H
FFFFFE30H	High-impedance output control register 100	HZA10CTL0		√	√		00H
FFFFFE31H	High-impedance output control register 101	HZA10CTL1		√	√		00H
FFFFFE38H	High-impedance output control register 110	HZA11CTL0		√	√		00H

4.4 Output Data and Port Read Value for Each Setting

Table 4-15 shows the values used to select the alternate function of the respective pins, output data and port read values for each setting. In addition to the settings shown in Table 4-15, the setting of each peripheral function control register is required.

5.4 PLL Function

5.4.1 Overview

The CPU and the operating clock of the peripheral macro can be switched between output of the oscillation frequency multiplied by 8, and clock-through mode.

When PLL function is used: Input clock (f_X) = 10 to 12.5 MHz, output clock (f_{XX}) = 80 to 100 MHz
Clock-through mode: Input clock (f_X) = 10 to 12.5 MHz, output clock (f_{XX}) = 10 to 12.5 MHz

5.4.2 PLL mode

In the PLL mode, the oscillation frequency (f_X) is multiplied by 8 with the PLL to generate a system clock (f_{XX}).

In the PLL mode, the clock is input from the oscillator to the PLL. A clock at a stable frequency must be supplied to the internal circuit after the lapse of the lockup time (frequency stabilization time) during which the phase is locked at a specific frequency and oscillation is stabilized. In the V850E/IG4 and V850E/IH4, the lockup time after release of reset is secured automatically.

Caution When a resonator of f_X = 12.5 MHz is used and if the oscillation stabilization time of that resonator must be 3 ms (MAX.), the reset input ($\overline{\text{RESET}}$ active) width must be 1.7 ms (MIN.).

5.4.3 Clock-through mode

In the clock-through mode, a system clock (f_{XX}) of the same frequency as the oscillation frequency (f_X) is generated.

(2/2)

Cautions 1. If the setting of the TAAnIOC0 register is changed when TOAn0 and TOAn1 are set in the output mode, the output of the pins change. Set the port in the input mode and make the port go into a high-impedance state, noting changes in the pin status.

2. Rewrite the TAAnOL1, TAAnOE1, TAAnOL0, and TAAnOE0 bits when the TAAnCTL0.TAAnCE bit = 0. (The same value can be written when the TAAnCE bit = 1.) If rewriting was mistakenly performed, clear the TAAnCE bit to 0 and then set the bits again.

3. Even if the TAAnOL0 or TAAnOL1 bit is manipulated when the TAAnCE, TAAnOE0, and TAAnOE1 bits are 0, the output level of the TOAn0 and TOAn1 pins changes.

Figure 7-26. Register Setting in One-Shot Pulse Output Mode (3/3)

(f) TABn capture/compare registers 0 to 3 (TABnCCR0 to TABnCCR3)

If D_0 is set to the TABnCCR0 register and D_b to the TABnCCRb register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_b - D_0 + 1) \times$ Count clock cycle

Output delay period = $D_b \times$ Count clock cycle

Caution One-shot pulses are not output even in the one-shot pulse output mode, if the value set in the TABnCCRb register is greater than that set in the TABnCCR0 register.

Remarks 1. TABn I/O control register 1 (TABnIOC1) and TABn option register 0 (TABnOPT0) are not used in the one-shot pulse output mode.

2. n = 0, 1

b = 1 to 3

(1) 16-bit counter

This 16-bit counter can count internal clocks or external events.

The count value of this counter can be read by using the TTmCNT register.

When the TTmCTL0.TTmCE bit = 0, the value of the 16-bit counter is FFFFH. If the TTmCNT register is read at this time, 0000H is read.

Reset sets the TTmCE bit to 0.

(2) CCR0 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TTmCCR0 register is used as a compare register, the value written to the TTmCCR0 register is transferred to the CCR0 buffer register. When the count value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTTEQCm0) is generated.

The CCR0 buffer register cannot be read or written directly.

The CCR0 buffer register is set to 0000H after reset, and the TTmCCR0 register is set to 0000H.

(3) CCR1 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TTmCCR1 register is used as a compare register, the value written to the TTmCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTTEQCm1) is generated.

The CCR1 buffer register cannot be read or written directly.

The CCR1 buffer register is set to 0000H after reset, and the TTmCCR1 register is set to 0000H.

(4) Edge detector

This circuit detects the valid edges input to the TITm0, TITm1, EVTTm, TENCm0, TENCm1, and TECRm pins. No edge, rising edge, falling edge, or both the rising and falling edges can be selected as the valid edge by using the TTmIOC1, TTmIOC2, and TTmIOC3 registers.

(5) Output controller

This circuit controls the output of the TOTm0, and TOTm1 pins. The output controller is controlled by the TTmIOC0 registers.

(6) Selector

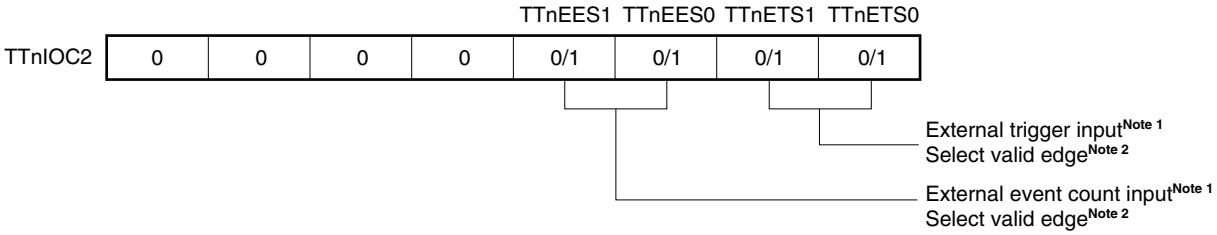
This selector selects the count clock for the 16-bit counter. Eight types of internal clocks or an external event can be selected as the count clock.

(7) Counter control

The count operation is controlled by the timer mode selected by the TTmCTL1 register.

Figure 8-30. Setting of Registers in One-Shot Pulse Output Mode (2/2)

(d) TMTn I/O control register 2 (TTnIOC2)



Notes 1. TMT0 and TMT1: EVTTm pin input
TMT2 and TMT3: TITk0 pin input

2. Set the valid edge selection of the unused alternate external input signals to “No edge detection”.

(e) TMTn counter read buffer register (TTnCNT)

The value of the 16-bit counter can be read by reading the TTnCNT register.

(f) TMTn capture/compare registers 0 and 1 (TTnCCR0 and TTnCCR1)

If D_0 is set to the TTnCCR0 register and D_1 to the TTnCCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_0 - D_1 + 1) \times$ Count clock cycle

Output delay period = $D_1 \times$ Count clock cycle

Caution One-shot pulses are not output even in the one-shot pulse output mode, if the value set in the TTnCCR1 register is greater than that set in the TTnCCR0 register.

Remarks 1. TMTm control register 2 (TTmCTL2), TMTn I/O control register 1 (TTnIOC1), TMTm I/O control register 3 (TTmIOC3), TMTn option register 0 (TTnOPT0), TMTm option register 1 (TTmOPT1), TMTm capture input select register (TTISLm), and TMTm counter write register (TTmTCW) are not used in the one-shot pulse output mode.

2. n = 0 to 3
m = 0, 1
k = 2, 3

9.3 Control Register

(1) TMMn control register 0 (TMnCTL0)

The TMnCTL0 register is an 8-bit register that controls the TMMn operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TMnCTL0 register by software.

After reset: 00H R/W Address: TM0CTL0 FFFFF540H, TM1CTL0 FFFFF550H, TM2CTL0 FFFFF560H, TM3CTL0 FFFFF570H

	<7>	6	5	4	3	2	1	0
TMnCTL0 (n = 0 to 3)	TMnCE	0	0	0	0	TMnCKS2	TMnCKS1	TMnCKS0

TMnCE	Internal clock operation enable/disable specification
0	TMMn operation disabled (16-bit counter reset asynchronously)
1	TMMn operation enabled. Start operation clock supply. Start TMMn operation.
The internal clock control and internal circuit reset for TMMn are performed asynchronously with the TMnCE bit. When the TMnCE bit is cleared to 0, the internal clock of TMMn is stopped (fixed to low level) and 16-bit counter is reset asynchronously.	

TMnCKS2	TMnCKS1	TMnCKS0	Count clock selection
0	0	0	$f_{XX}/2$
0	0	1	$f_{XX}/4$
0	1	0	$f_{XX}/8$
0	1	1	$f_{XX}/32$
1	0	0	$f_{XX}/256$
1	0	1	$f_{XX}/1024$
1	1	0	$f_{XX}/2048$
1	1	1	$f_{XX}/4096$

Cautions 1. Set the TMnCKS2 to TMnCKS0 bits when the TMnCE bit = 0.
However, when changing the value of the TMnCE bit from 0 to 1, it is impossible to set the value of the TMnCKS2 to TMnCKS0 bits simultaneously.

2. Be sure to clear bits 3 to 6 to "0".

Remark f_{XX}: Peripheral clock frequency

10.4.5 TAAn tuning operation for A/D conversion start trigger signal output

This section explains the tuning operation of TAAn and TABn in the 6-phase PWM output mode.

In the 6-phase PWM output mode, the tuning operation is performed with TABn serving as the master and TAAn as a slave. The conversion start trigger signal of A/D converters 0 and 1 can be set as the A/D conversion start trigger source by the INTTAnCC0 and INTTAnCC1 signals of TAAn and the INTTBnOV and INTTBnCC0 signals of TABn.

Remark n = 0, 1

(1) Tuning operation starting procedure

The TAAn and TABn registers should be set using the following procedure to perform the tuning operation.

(a) Setting of TAAn register (stop the operations of TABn and TAAn (by setting the TABnCTL0.TABnCE bit and TAAnCTL0.TAAnCE bit to 0))

- Set the TAAnCTL1 register to 85H (set the tuning operation slave mode and free-running timer mode).
- Set the TAAnOPT0 register to 00H (select the compare register).
- Set an appropriate value to the TAAnCCR0 and TAAnCCR1 registers (set the default value for comparison for starting the operation).

(b) Setting of TABn register

- Set the TABnCTL1 register to 07H (set the master mode and 6-phase PWM output mode).
- Set an appropriate value to the TABnIOC0 register (set the output mode of TOBnT1 to TOBnT3). However, set the TABnOL0 bit to 0 and the TABnOE0 bit to 1 (enable positive phase output). Unless this setting is made, the crest interrupt (INTTBnCC0) and valley interrupt (INTTBnOV) do not occur. Consequently, the conversion start trigger signal of A/D converters 0 and 1 is not correctly generated.
- Clear the TABnIOC1 and TABnIOC2 registers to 00H (the TIBn0 to TIBn3, EVTBn, and TRGBn pins of TABn are not used).
- Clear the TABnOPT0 register to 00H (select the compare register).
- Set an appropriate value to the TABnCCR0 to TABnCCR3 registers (set the default value for comparison for starting the operation).
- Set the TABnCTL0 register to 0xH (set the TABnCE bit to 0 and the operating clock of TABn). The operating clock of TABn set by the TABnCTL0 register is also supplied to TAAn, and the count operation is performed at the same timing. The operating clock of TAAn set by the TAAnCTL0 register is ignored.

(c) Setting of TMQOPn (TMQn option) register

- Set an appropriate value to the TABnOPT1 and TABnOPT2 registers.
- Set an appropriate value to the TABnIOC3 register (set TOBnB1 to TOBnB3 in the output mode).
- Set an appropriate value to the TABnDTC register (set the default value for comparison for starting the operation).

(d) Setting of alternate function

- Select the alternate function of the port by setting the port to the port control mode.

(10) UARTB FIFO status register 1 (UBFIS1)

The UBFIS1 register is valid in the FIFO mode (UBFIC0.UBMOD bit = 1). This register can be used to read the number of empty bytes of transmit FIFO.

This register is read-only in 8-bit units.

Reset sets this register to 10H.

Caution The values of the UBTB4 to UBTB0 bits are reflected after transmit data has been written to the UBTX register and then time of two cycles of the fxx/2 has passed. Therefore, care must be exercised when referencing the UBFIS1 register after transmit data has been written to the UBTX register.

After reset: 10H R Address: FFFFFA4FH

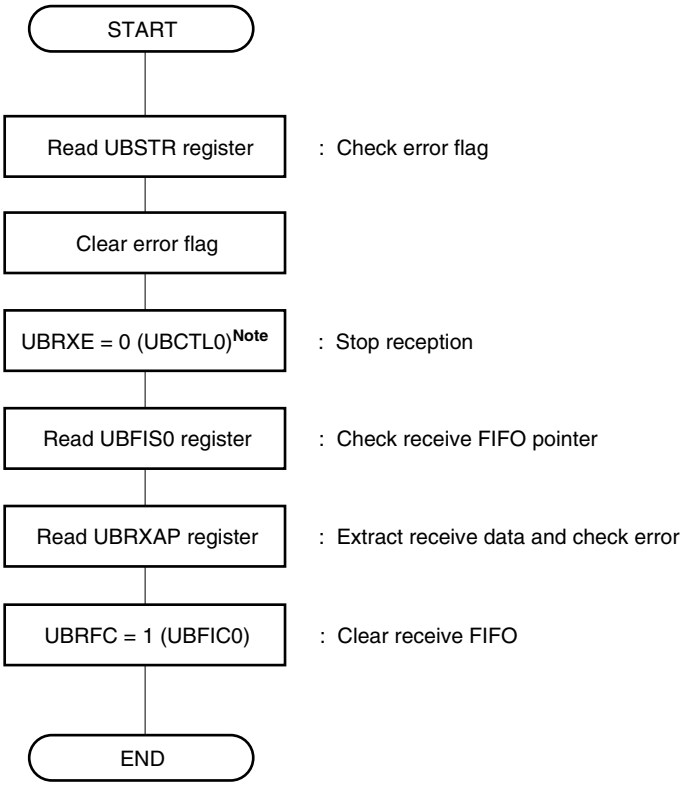
	7	6	5	4	3	2	1	0
UBFIS1	0	0	0	UBTB4	UBTB3	UBTB2	UBTB1	UBTB0

UBTB4	UBTB3	UBTB2	UBTB1	UBTB0	Transmit FIFO pointer
0	0	0	0	0	0 bytes
0	0	0	0	1	1 byte
0	0	0	1	0	2 bytes
0	0	0	1	1	3 bytes
0	0	1	0	0	4 bytes
0	0	1	0	1	5 bytes
0	0	1	1	0	6 bytes
0	0	1	1	1	7 bytes
0	1	0	0	0	8 bytes
0	1	0	0	1	9 bytes
0	1	0	1	0	10 bytes
0	1	0	1	1	11 bytes
0	1	1	0	0	12 bytes
0	1	1	0	1	13 bytes
0	1	1	1	0	14 bytes
0	1	1	1	1	15 bytes
1	0	0	0	0	16 bytes
Setting prohibited					Invalid

Indicates the number of empty bytes of transmit FIFO (bytes that can be written) as a transmit FIFO pointer.

(10) Example of reception error processing flow in FIFO mode (1)

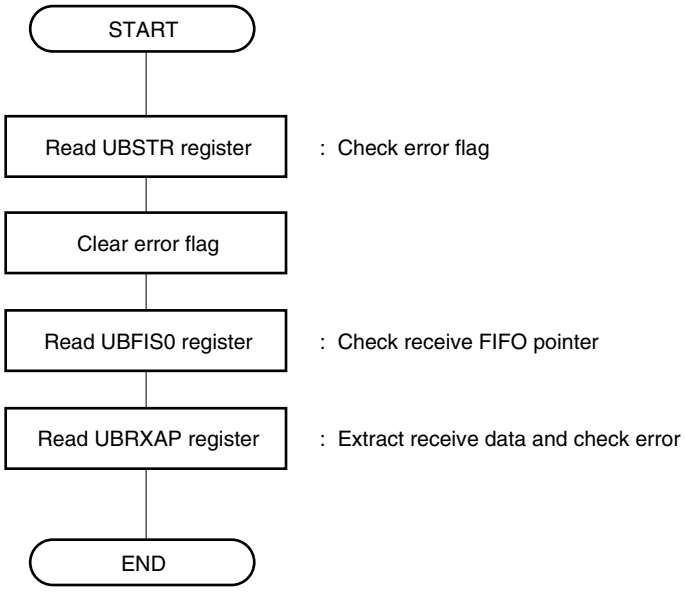
Figure 15-21. Example of Reception Error Processing Flow in FIFO Mode (1)



Note If the error flag is cleared when UBRXE bit = 0, the UBCTL0 register does not have to be set.

(11) Example of reception error processing flow in FIFO mode (2)

Figure 15-22. Example of Reception Error Processing Flow in FIFO Mode (2)



Caution Reception can be continued by completing this control flow before reception of the next data is ended. Extract the receive data and check if a reception error has occurred before receive FIFO becomes empty. Note that this control flow is valid only when a parity error or a framing error occurs. If an overflow error occurs, receive FIFO must be cleared (UBFIC0.UBRFC bit = 1).

If the next data is received before this control flow is ended, a reception error interrupt request signal (INTUBTIRE) may occur even if the data has been received correctly.

16.5.9 Continuous transfer mode (master mode, transmission/reception mode)

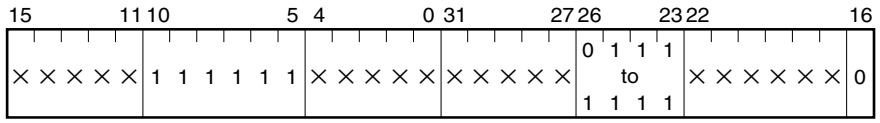
MSB first (CFnCTL0.CFnDIR bit = 0), communication type 1 (CFnCTL1.CFnCKP and CFnCTL1.CFnDAP bits = 00), communication clock (f_{CCLK}) = f_{XX}/4 (CFnCTL1.CFnCKS2 to CFnCTL1.CFnCKS0 bits = 000), transfer data length = 8 bits (CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits = 0000)

19.6 Exception Trap

An exception trap is an interrupt that is requested when the illegal execution of an instruction takes place. In the V850E/IG4 and V850E/IH4, an illegal opcode trap (ILGOP: Illegal Opcode Trap) is used as an exception trap.

19.6.1 Illegal opcode definition

The illegal instruction has an opcode (bits 10 to 5) of 111111B, a sub-opcode (bits 26 to 23) of 0111B to 1111B, and a sub-opcode (bit 16) of 0B. An exception trap occurs when an instruction applicable to this illegal instruction is executed.



×: Arbitrary

Caution Illegal opcodes must not be used because instructions may be newly assigned to these opcodes in the future.

(1) Operation

If an exception trap occurs, the CPU performs the following processing and transfers control to the handler routine.

<1> Saves the current PC to DBPC.
<2> Saves the current PSW to DBPSW.
<3> Sets the PSW.NP, PSW.EP, and PSW.ID bits (1).
<4> Sets the handler address (00000060H) for the exception trap to the PC and transfers control.

The processing of an exception trap is shown below.

After reset: 00H[Note] R/W Address: FFFFF888H

	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LIVRF

WDTRF	Occurrence of reset signal from watchdog timer (WDT)
0	Read: No reset request, Write: Clear
1	Reset request

LIVRF	Occurrence of reset signal from low-voltage detector (LVI)
0	Read: No reset request, Write: Clear
1	Reset request

Note After a reset by $\overline{\text{RESET}}$ pin input or the power-on-clear circuit (POC), or after a forced reset by the on-chip debug function: 00H
After a reset due to a watchdog timer overflow: 10H
After a reset by the low-voltage detector (LVI): 01H

Cautions 1. If setting (occurrence of reset of set source) and clearing (occurrence of system reset or writing 0 to the WDTRF or LVIRF bit) of the RESF register conflict, the priorities are as follows.

<1> A reset by $\overline{\text{RESET}}$ pin input or the power-on-clear circuit (POC), or a forced reset by the on-chip debug function (that clears the RESF register)
<2> A reset by WDT or LVI (that sets the RESF register)
<3> Writing 0 to the WDTRF or LVIRF bit by a bit manipulation or store instruction (that clears the RESF register)

2. Even if reset masking was specified when a flag setting source occurred, the flag is set. (Reset masking does not affect setting the flag.)

26.2.14 Supply voltage application/cutoff timing

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = V_{DD2} = V_{DD3} = 1.35 to 1.65 V, EV_{DD0} = EV_{DD1} = EV_{DD2} = EV_{DD3} = FV_{DD} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 3.5 to 5.5 V, V_{SS0} = V_{SS1} = V_{SS2} = EV_{SS0} = EV_{SS1} = EV_{SS2} = EV_{SS3} = EV_{SS4} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from FV_{DD} rise to EV_{DD} rise	t_{RER}		–50	0	ms
Delay time from FV_{DD} rise to V_{DD} rise	t_{RVR}		–50	0	ms
Delay time from FV_{DD} rise to AV_{DD} rise	t_{RAR}		–50	0	ms
Delay time from FV_{DD} rise to $\overline{\text{RESET}}$ rise	t_{RRR}	When using an external reset	T_{osc} + 0.5		ms
Delay time from FV_{DD} fall to EV_{DD} fall	t_{FEF}		0	50	ms
Delay time from FV_{DD} fall to V_{DD} fall	t_{FVF}		0	50	ms
Delay time from FV_{DD} fall to AV_{DD} fall	t_{FAF}		0	50	ms

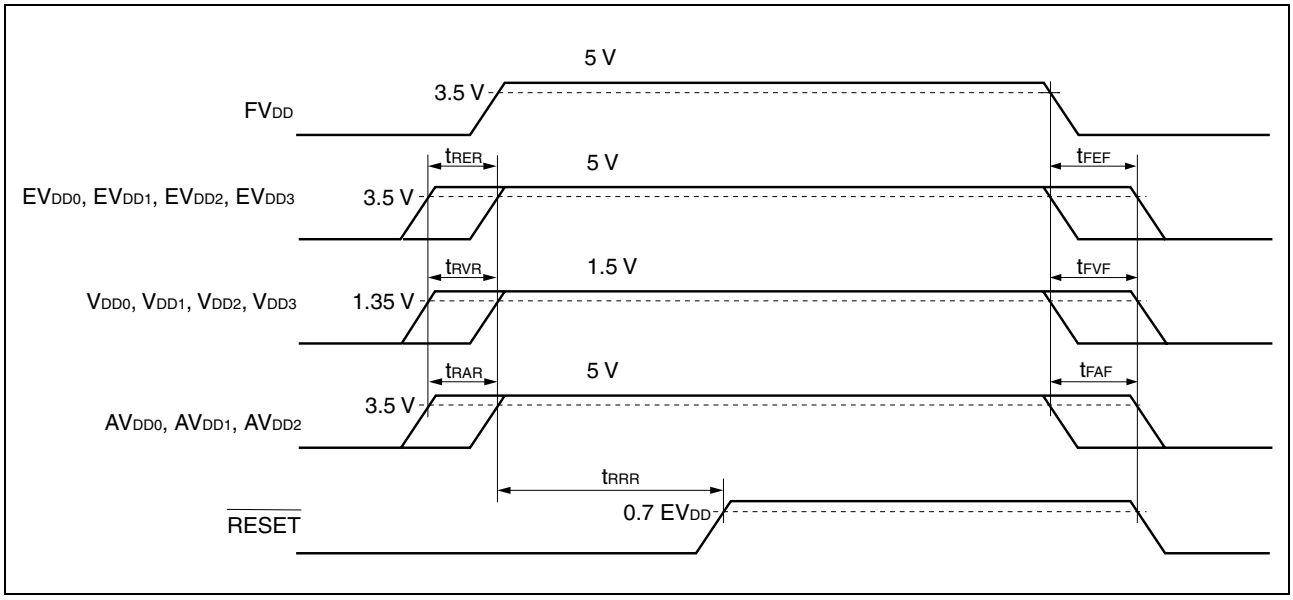
Remark Tosc: Oscillation stabilization time

Supply voltage application/cutoff timing

<R> **Cautions 1. There are no regulations for the voltage level and time of FV_{DD}, EV_{DD0}, EV_{DD1}, EV_{DD2}, EV_{DD3}, V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3}, AV_{DD0}, AV_{DD1}, and AV_{DD2} in the process of natural discharge after power supply cutoff.**

2. Apply all of the FV_{DD}, EV_{DD0}, EV_{DD1}, EV_{DD2}, EV_{DD3}, V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3}, AV_{DD0}, AV_{DD1}, and AV_{DD2} power supplies.
It is prohibited to apply one of these power supplies without supplying them all.

(a) External $\overline{\text{RESET}}$ (recommended conditions)



(3) Register symbols used in operations

Register Symbol	Explanation
←	Input for
GR [ ]	General-purpose register
SR [ ]	System register
zero-extend (n)	Expand n with zeros until word length.
sign-extend (n)	Expand n with signs until word length.
load-memory (a, b)	Read size b data from address a.
store-memory (a, b, c)	Write data b into address a in size c.
load-memory-bit (a, b)	Read bit b of address a.
store-memory-bit (a, b, c)	Write c to bit b of address a.
saturated (n)	Execute saturated processing of n (n is a 2's complement). If, as a result of calculations, n ≥ 7FFFFFFFH, let it be 7FFFFFFFH. n ≤ 80000000H, let it be 80000000H.
result	Reflects the results in a flag.
Byte	Byte (8 bits)
Halfword	Half word (16 bits)
Word	Word (32 bits)
+	Addition
–	Subtraction
ll	Bit concatenation
×	Multiplication
÷	Division
%	Remainder from division results
AND	Logical product
OR	Logical sum
XOR	Exclusive OR
NOT	Logical negation
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

(4) Register symbols used in execution clock

Register Symbol	Explanation
i	If executing another instruction immediately after executing the first instruction (issue).
r	If repeating execution of the same instruction immediately after executing the first instruction (repeat).
l	If using the results of instruction execution in the instruction immediately after the execution (latency).

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 18**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 18, 20**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					

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Edition	Description	Applied to:
2nd	Modification of description in **24.2.4 Cautions**	**CHAPTER 24 ON-CHIP DEBUG FUNCTION**
	Addition of **25.2 Memory Configuration**	**CHAPTER 25 FLASH MEMORY**
	Addition of description to **25.3 Functional Overview**	
	Modification of description in **25.9 Rewriting by Self Programming**	
	Modification of description in **26.1.3 Operating conditions**	**CHAPTER 26 ELECTRICAL SPECIFICATIONS**
	Modification of description in **26.1.4 Clock oscillator characteristics**	
	Modification of description in **26.1.5 DC characteristics**	
	Modification of description in **26.1.7 (5) UARTB timing**	
	Modification of description in **26.1.8 Characteristics of A/D converters 0 and 1**	
	Modification of description in **26.1.9 Characteristics of A/D converter 2**	
	Modification of description in **26.1.11 Comparator characteristics**	
	Modification of description in **26.1.12 Power-on-clear circuit (POC)**	
	Modification of description in **26.1.13 Low-voltage detector (LVI)**	
	Addition of **26.1.14 Supply voltage application/cutoff timing**	
	Modification of description in **26.1.15 Flash memory programming characteristics**	
	Modification of description in **26.2.3 Operating conditions**	
	Modification of description in **26.2.4 Clock oscillator characteristics**	
	Modification of description in **26.2.5 DC characteristics**	
	Modification of description in **26.2.7 (5) UARTB timing**	
	Modification of description in **26.2.8 Characteristics of A/D converters 0, 1**	
	Modification of description in **26.2.9 Characteristics of A/D converter 2**	
	Modification of description in **26.2.11 Comparator characteristics**	
	Modification of description in **26.2.12 Power-on-clear circuit (POC)**	
	Modification of description in **26.2.13 Low-voltage detector (LVI)**	
	Addition of **26.2.14 Supply voltage application/cutoff timing**	
	Modification of description in **26.2.15 Flash memory programming characteristics**	
	Modification of description in **CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**	**CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**
	Addition of **APPENDIX D REVISION HISTORY**	**APPENDIX D REVISION HISTORY**