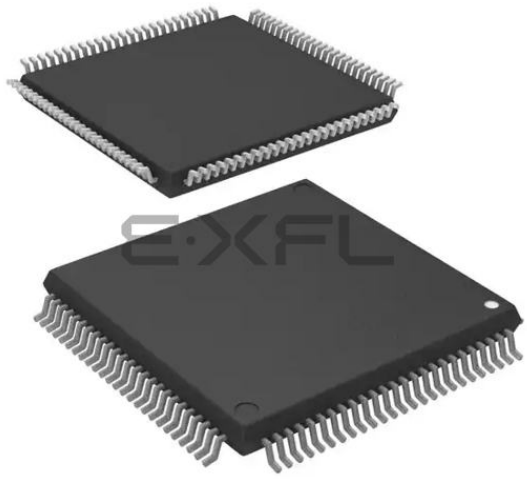

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	480KB (480K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3915gc-r-ueu-ax

4.3.2 Port 1

Port 1 can be set to the input or output mode in 1-bit units.

The number of I/O pins for port 1 differs depending on the product.

Generic Name	Number of I/O Ports
V850E/IG4	7-bit I/O port
V850E/IH4	8-bit I/O port

The pins of port 1 have the following alternate functions.

Table 4-7. Alternate Functions of Port 1

Pin Name	Pin No.			Alternate-Function Pin Name	I/O	Pull-Up[Note 1]
	IG4		IH4			
	GC	GF	GF			
P10	98	26	36	TOB0T1/TIB01/TOB01	I/O	Provided
P11	97	25	35	TOB0B1/TIB02/TOB02	I/O	
P12	96	24	34	TOB0T2/TIB03/TOB03	I/O	
P13	95	23	33	TOB0B2/TIB00	I/O	
P14	94	22	32	TOB0T3/EVTB0	I/O	
P15	93	21	31	TOB0B3/TRGB0	I/O	
P16	92	20	30	TOB00/TOB0OFF/INTP08/ADTRG0/INTADT0	I/O	
P17[Note 2]	–	–	29	–	–	

Notes 1. Software pull-up function

2. V850E/IH4 only

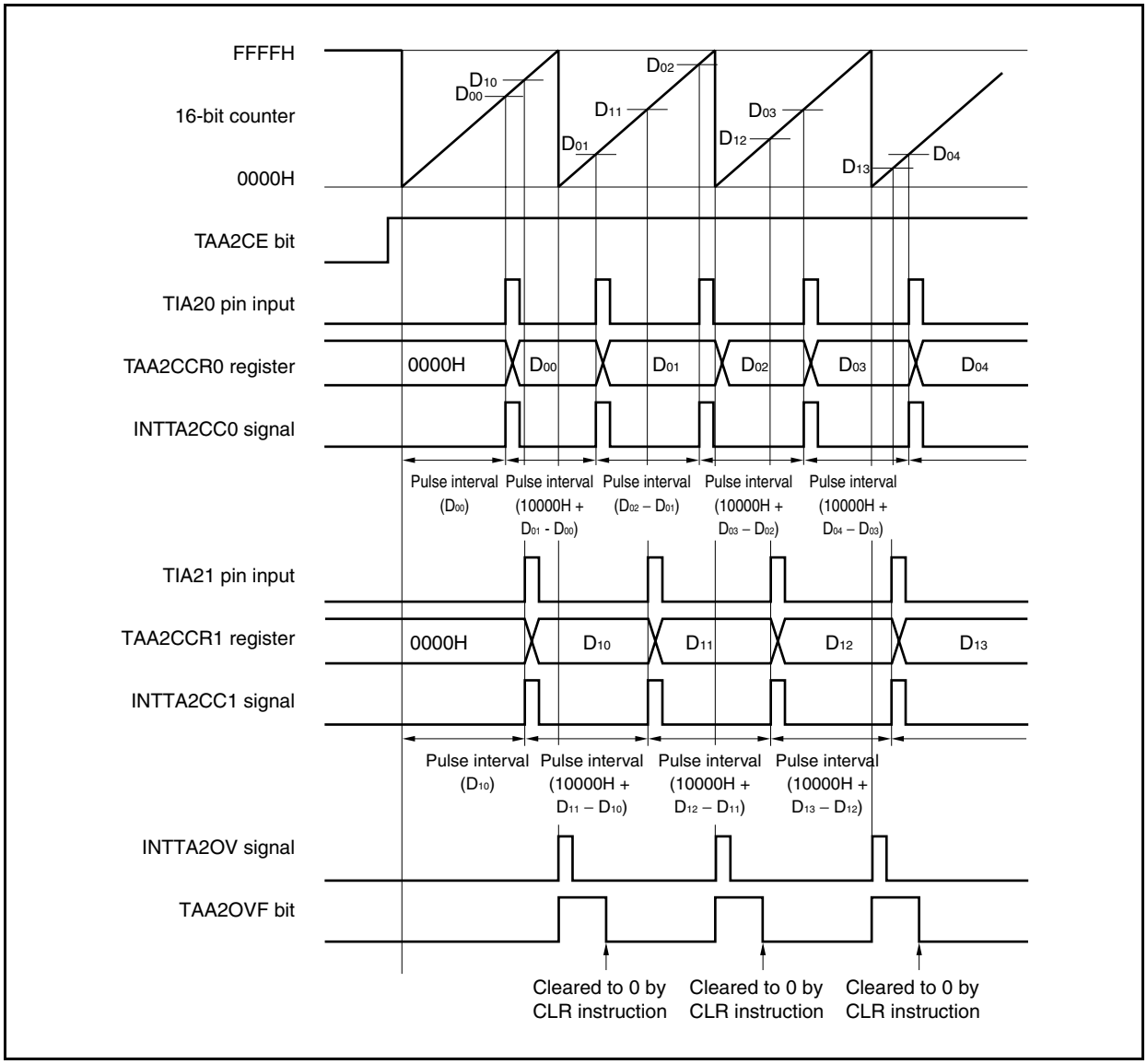
Caution When P10 to P15 are used as TOB0T1 to TOB0T3 and TOB0B1 to TOB0B3, they go into a high-impedance state by inputting the following active signal.

- **Output of high impedance setting signal from high impedance output controller**
- **Output of clock stop detection signal from clock monitor**

Remark IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

(b) Pulse width measurement with capture register

When pulse width measurement is performed with the TAA2CCRa register used as a capture register, software processing is necessary for reading the capture register each time the INTTA2CCa signal has been detected and for calculating an interval.



When executing pulse width measurement in the free-running timer mode, two pulse widths can be measured with one channel.

To measure a pulse width, the pulse width can be calculated by reading the value of the TAA2CCRa register in synchronization with the INTTA2CCa signal, and calculating the difference between the read value and the previously read value.

Remark a = 0, 1

7.3 Configuration

TABn includes the following hardware (n = 0, 1).

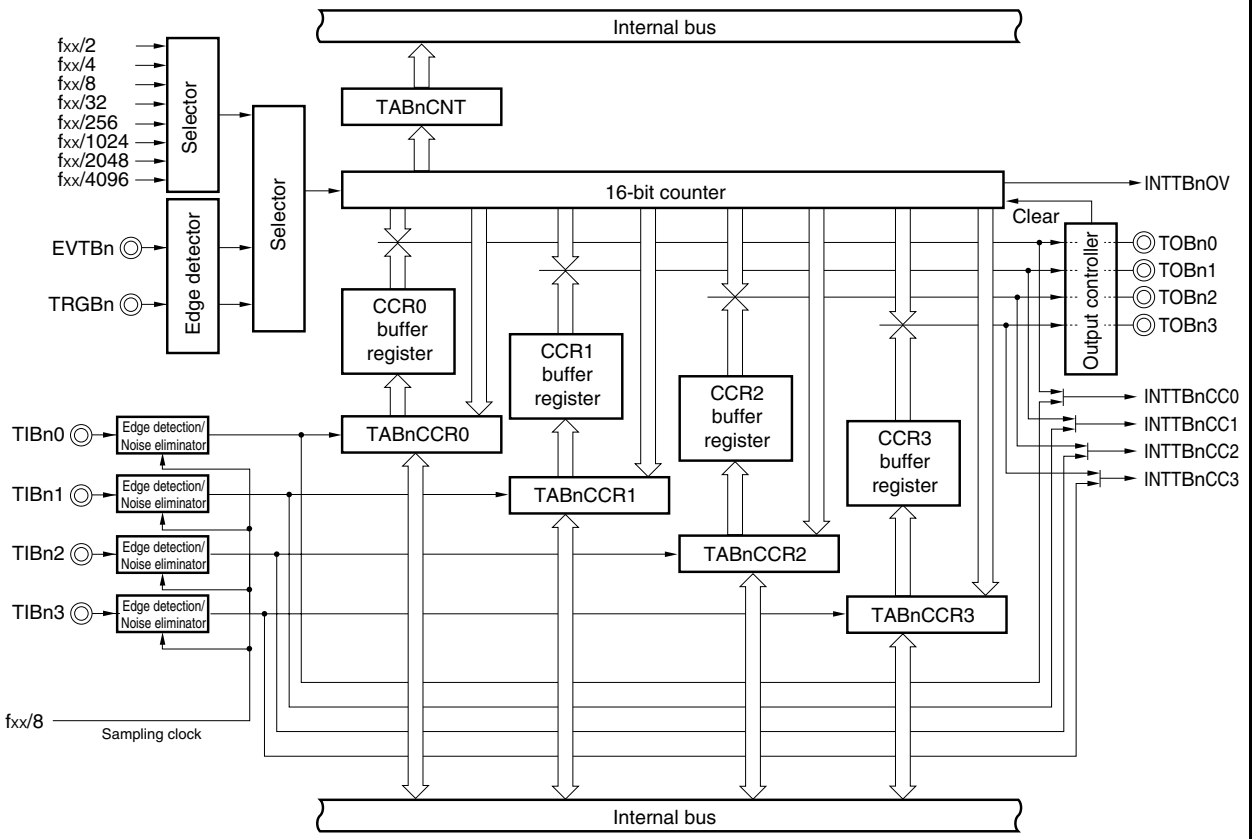
Table 7-1. TABn Configuration

Item	Configuration
Timer register	16-bit counter × 1
Registers	TABn counter read buffer register (TABnCNT) TABn capture/compare registers 0 to 3 (TABnCCR0 to TABnCCR3) CCR0 to CCR3 buffer registers
Timer input	12 in total (TIB00 to TIB03, TIB10 to TIB13, EVTB0, EVTB1, TRGB0, TRGB1 pins)[Note]
Timer output	8 in total (TOB00 to TOB03, TOB10 to TOB13 pins)[Note]
Control registers	TABn control registers 0, 1 (TABnCTL0, TABnCTL1) TABn I/O control registers 0 to 2 (TABnIOC0 to TABnIOC2) TABn option register 0 (TABnOPT0)

Note The TIBn1 to TIBn3 pins function alternately as timer output pins (TOBn1 to TOBn3).

Remark n = 0, 1

Figure 7-1. TABn Block Diagram



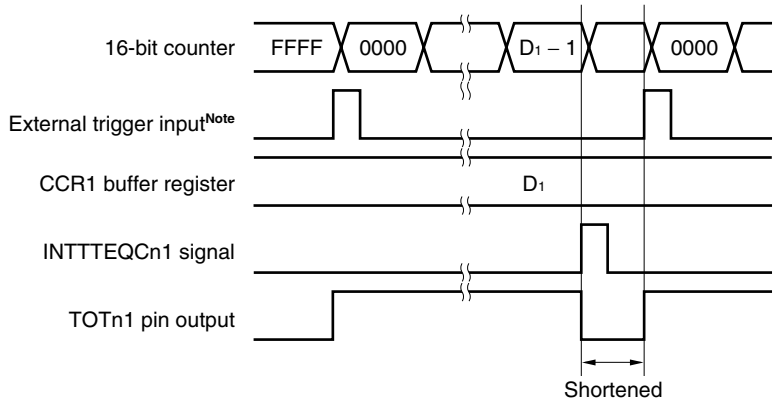
Remarks 1. fxx: Peripheral clock

2. For the noise eliminator, see **4.6 Noise Eliminator**.

3. n = 0, 1

(c) Conflict between trigger detection and match with CCR1 buffer register

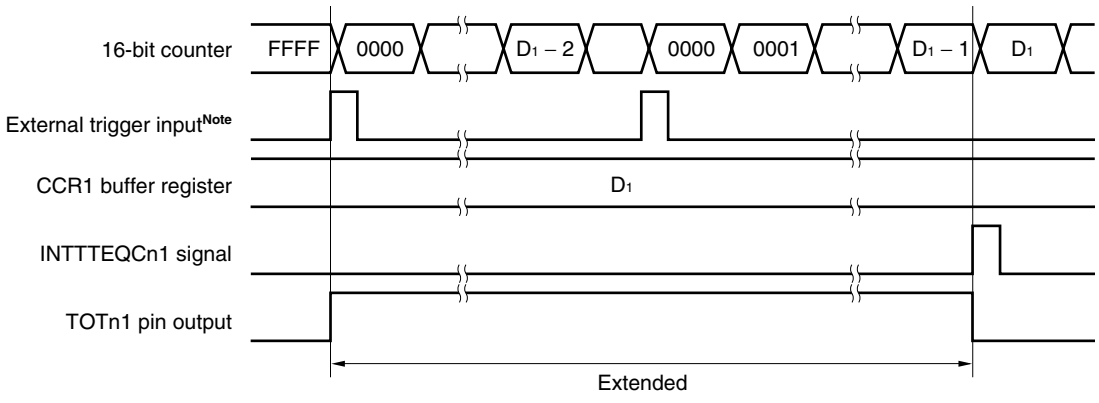
If the trigger is detected immediately after the INTTTEQCn1 signal is generated, the 16-bit counter is immediately cleared to 0000H, the output signal of the TOTn1 pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.



Note TMT0 and TMT1: EVTTm pin input
TMT2 and TMT3: TITk0 pin input

Remark n = 0 to 3
m = 0, 1
k = 2, 3

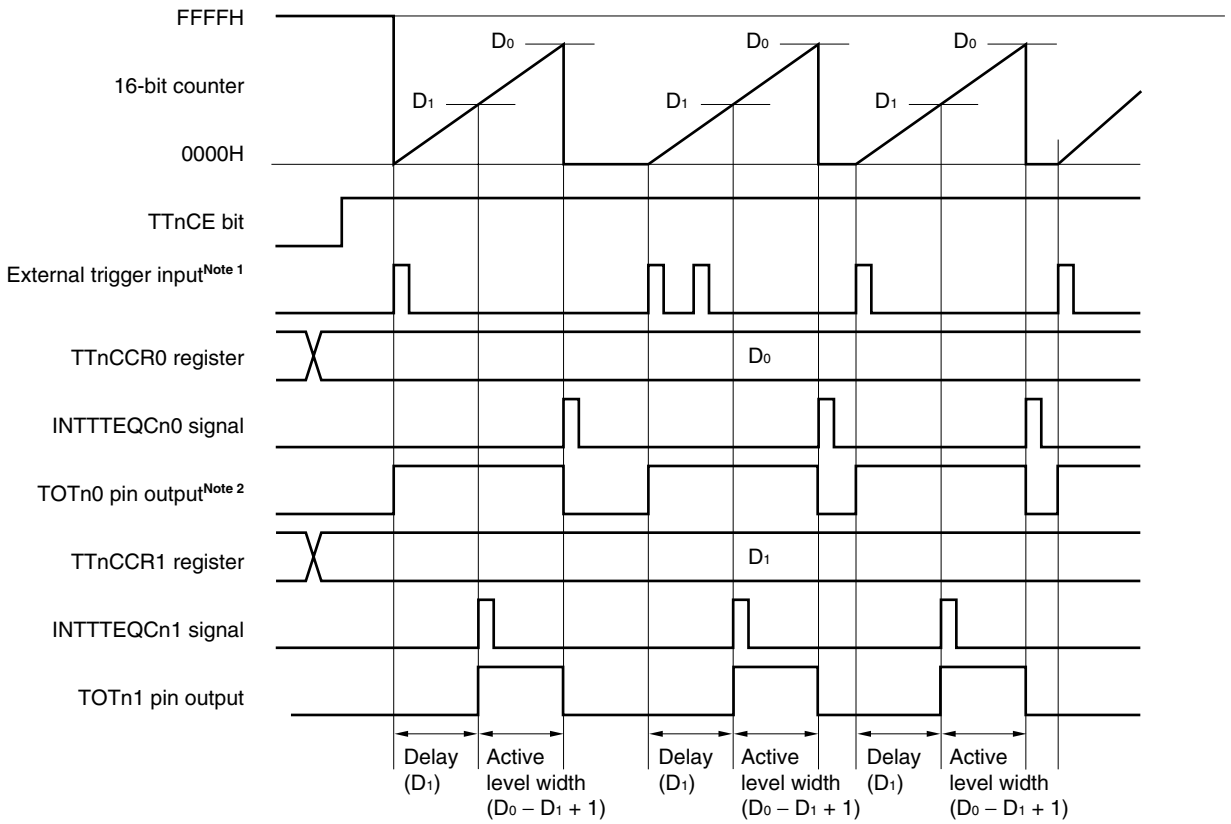
If the trigger is detected immediately before the INTTTEQCn1 signal is generated, the INTTTEQCn1 signal is not generated, and the 16-bit counter is cleared to 0000H and continues counting. The output signal of the TOTn1 pin remains active. Consequently, the active period of the PWM waveform is extended.



Note TMT0 and TMT1: EVTTm pin input
TMT2 and TMT3: TITk0 pin input

Remark n = 0 to 3
m = 0, 1
k = 2, 3

Figure 8-29. Basic Timing in One-Shot Pulse Output Mode



Notes 1. EVTTm pin input in the case of TMT0 and TMT1, and TITk0 pin input in the case of TMT2 and TMT3.

2. In the case of TMT2 and TMT3, this function can only be used by using a software trigger.

When the TTnCE bit is set to 1, 16-bit timer/event counter T waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a one-shot pulse from the TOTn1 pin. After the one-shot pulse is output, the 16-bit counter is cleared to 0000H, stops counting, and waits for a trigger. When the trigger is generated again, the 16-bit counter starts counting from 0000H. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows.

Output delay period = (Set value of TTnCCR1 register) × Count clock cycle

Active level width = (Set value of TTnCCR0 register − Set value of TTnCCR1 register + 1) × Count clock cycle

The compare match interrupt request signal (INTTTEQCn0) is generated when the 16-bit counter counts after its count value matches the value of the CCR0 buffer register. The compare match interrupt request signal (INTTTEQCn1) is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The valid edge of an external trigger input (EVTTm pin in the case of TMT0 and TMT1, and TITk0 pin in the case of TMT2 and TMT3) or setting the software trigger (TTnCTL1.TTnEST bit) to 1 is used as the trigger.

Remark n = 0 to 3
m = 0, 1
k = 2, 3

8.6.10 Encoder compare mode (TTmMD3 to TTmMD0 bits = 1000)

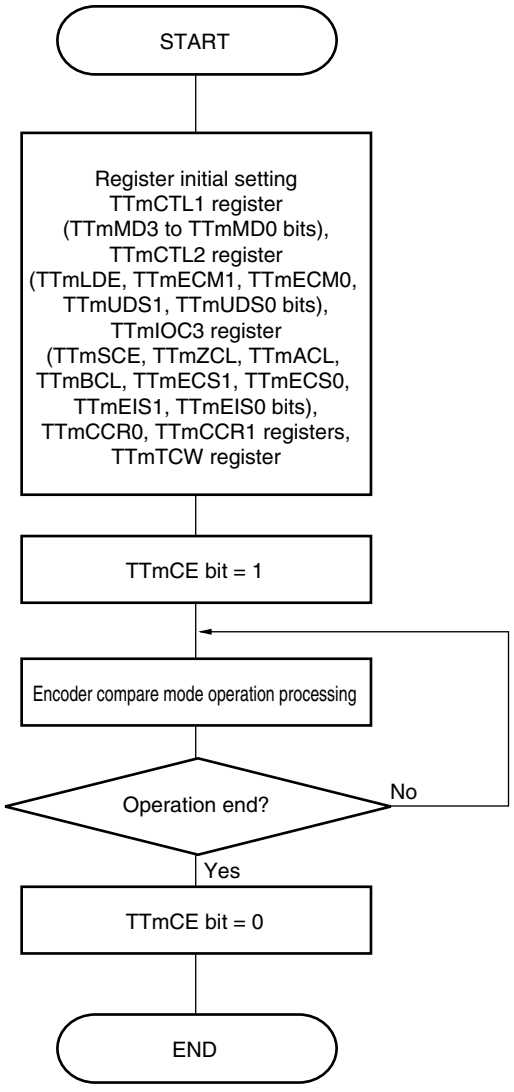
In the encoder compare mode, the encoder is controlled by using both the TTmCCR0 and TTmCCR1 registers as compare registers and the input pins for encoder count function (TENCm0, TENCm1, and TECRm).

In this mode, the 16-bit counter can be cleared to 0000H in three ways: when the count value of the counter matches the value of the CCRa buffer register (compare match interrupt request signal (INTTTEQCma) is generated), when the edge of the encoder clear input (TECRm pin) is detected and cleared, and when the clear level condition of TENCm0, TENCm1, and TECRm pins is detected and cleared.

When the 16-bit counter underflows, the set value of the TTmCCR0 register can be transferred to the counter.

(1) Encoder compare mode operation flow

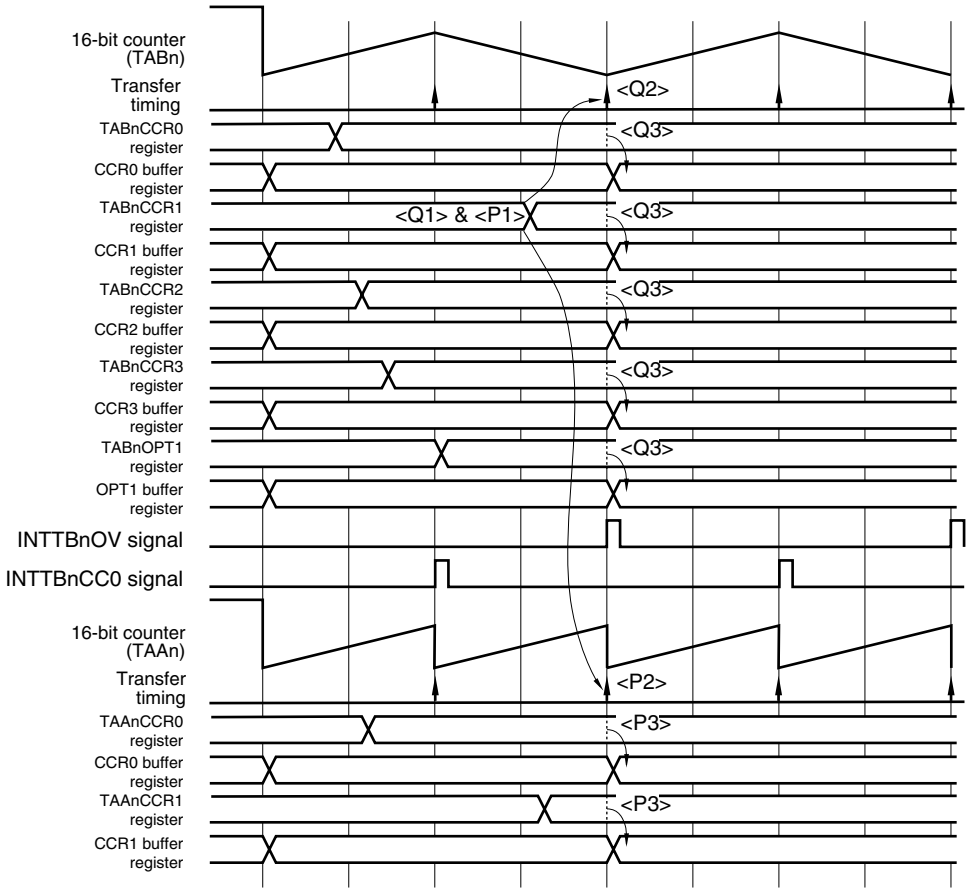
Figure 8-64. Encoder Compare Mode Operation Flow



: See **Figure 8-65 Encoder Compare Mode Operation Processing**.

Remark m = 0, 1

Figure 10-26. Basic Operation in Batch Mode



[Operation of TABn]

<Q1> Write the TABnCCR1 register

<Q2> The target timing is the first transfer timing after a write to the TABnCCR1 register.

<Q3> The values are transferred all at once at the transfer timing.

[Operation of TAAn]

<P1> Write the TABnCCR1 register

<P2> The target timing is the first transfer timing after a write to the TABnCCR1 register.

<P3> The values are transferred all at once at the transfer timing.

11.3 Control Registers

(1) Watchdog timer mode register (WDTM)

The WDTM register sets the overflow time and operation clock of the watchdog timer.

This register can be read or written in 8-bit units. This register can be read any number of times, but can be written only once following reset release; it cannot then be written a second or subsequent time.

Reset sets this register to 67H.

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4	3	2	1	0
WDTM	0	WDM1	WDM0	0	0	WDCS2	WDCS1	WDCS0

WDM1	WDM0	Selection of operation mode of watchdog timer
0	0	Stop operation
0	1	Non-maskable interrupt request mode (generation of INTWDT signal)
1	×	Reset mode (generation of WDTRES signal)

Cautions 1. For details of the WDCS2 to WDCS0 bits, see Table 11-2 Overflow Time.

2. If the WDTM register is rewritten while the watchdog timer is counting, the counter of the watchdog timer is cleared to 0000H.

3. Be sure to clear bits 3, 4, and 7 to "0".

Table 11-2. Overflow Time

WDCS2	WDCS1	WDCS0	Overflow Time	f_{XX} = 100 MHz
0	0	0	$2^{19}/f_{XX}$	5.2 ms
0	0	1	$2^{20}/f_{XX}$	10.5 ms
0	1	0	$2^{21}/f_{XX}$	21.0 ms
0	1	1	$2^{22}/f_{XX}$	41.9 ms
1	0	0	$2^{23}/f_{XX}$	83.9 ms
1	0	1	$2^{24}/f_{XX}$	167.8 ms
1	1	0	$2^{25}/f_{XX}$	335.5 ms
1	1	1	$2^{26}/f_{XX}$	671.1 ms

(7) A/D converter n channel specification register 1 (ADnCH1)

The ADnCH1 register is a register that specifies the analog input pin for selection trigger 1 in the conversion channel specification mode and extension buffer mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: AD0CH1 FFFFF232H, AD1CH1 FFFFF2B2H

	7	6	5	4	3	2	1	0
ADnCH1 (n = 0, 1)	0	ADn TRGCH16	ADn TRGCH15	ADn TRGCH14	0	ADn TRGCH12	ADn TRGCH11	ADn TRGCH10

ADnTRGCH16	ADnTRGCH15	ADnTRGCH14	Specification of analog input pin for selection trigger 1
0	0	0	ANIn0
0	0	1	ANIn1
0	1	0	ANIn2
0	1	1	ANIn3[Note]
1	0	0	Setting prohibited
1	0	1	ANIn5
1	1	0	ANIn6
1	1	1	ANIn7

ADnTRGCH12	ADnTRGCH11	ADnTRGCH10	Specification of analog input pin for selection trigger 1
0	0	0	ANIn0
0	0	1	ANIn1
0	1	0	ANIn2
0	1	1	ANIn3[Note]
1	0	0	Setting prohibited
1	0	1	ANIn5
1	1	0	ANIn6
1	1	1	ANIn7

Note For the V850E/IG4, this can be specified only for A/D converter 0.
Specifying this for A/D converter 1 is prohibited.

Cautions 1. Set the ADnCH1 register when the ADnSCM.ADnCE bit = 0 (conversion operation is stopped) (the same value can be written to the register when the ADnCE bit = 1 (conversion operation is enabled)).

2. Be sure to set bits 3 and 7 to "0".

(15) A/D trigger rising edge, falling edge specification registers (ADTR, ADTF)

The ADTR and ADTF registers are registers that specify the trigger mode of the ADTRG0/INTADT0 and ADTRG1/INTADT1 pins and can specify the valid edge independently for each pin (rising edge, falling edge, or both rising and falling edges).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When the function is changed from the external trigger input of the A/D converter n (alternate function)/external interrupt function (alternate function) to the port mode, an edge may be detected. Therefore, be sure to set the ADTFn and ADTRn bits to 00, and then set the port mode.

After reset: 00H R/W Address: FFFFF2F2H

	7	6	5	4	3	2	1	0
ADTR	0	0	0	0	0	0	ADTR1	ADTR0

After reset: 00H R/W Address: FFFFF2F0H

	7	6	5	4	3	2	1	0
ADTF	0	0	0	0	0	0	ADTF1	ADTF0

Remark For the valid edge specification, see **Table 12-8**.

Table 12-8. Valid Edge Specification of ADTRG0/INTADT0 and ADTRG1/INTADT1 Pins

ADTFn	ADTRn	Valid Edge Specification
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

Caution When not using these pins as the ADTRGn/INTADTn pins, be sure to set the ADTFn and ADTRn bits to 00.

Remark n = 0, 1

12.4.7 A/D trigger mode (normal operation mode)

A/D conversion is started when the ADnSCM.ADnCE bit is set to 1.

When conversion is started, the ADnSCM.ADnCS bit is set to 1 (conversion is in progress).

If the ADnSCM register is written during A/D conversion, the conversion is stopped and started again from the beginning.

(1) Operation of 1-channel conversion

The signal of one analog input pin (ANInk) is converted once and the result is stored in one ADnCRk register. The ANInk pin and ADnCRk register correspond to each other on a one-to-one basis.

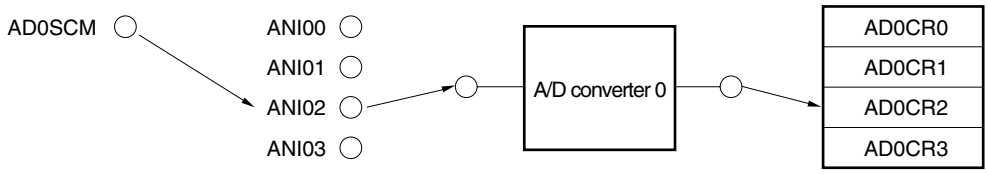
Each time conversion has been completed, an A/Dn conversion end interrupt request signal (INTADn) is generated. After A/D conversion is completed, The A/D converter stops conversion operation with the ADnSCM.ADnCE bit remaining set to 1. The A/D conversion can be restarted by setting the ADnCE bit to 1.

This operation is suitable for an application where the result of A/D conversion should be read each time conversion has been completed once.

Analog Input Pin	A/D Conversion Result Register
ANInk	ADnCRk

Remark A/D converter 0: n = 0
k = 0 to 3, 5 to 7
A/D converter 1: n = 1
V850E/IG4: k = 0 to 2, 5 to 7
V850E/IH4: k = 0 to 3, 5 to 7

Figure 12-14. Example of 1-Channel Conversion Operation (A/D Trigger Mode): A/D Converter 0



(1) AD0CE bit = 1 (enable)
(2) Signal of ANI02 pin is A/D converted
(3) Conversion result is stored in AD0CR2 register
(4) AD0SCM.AD0CS bit = 0
(5) INTAD0 interrupt request signal is generated

Remark This is an operation example when the AD0SCM.AD0PLM, AD0TRG1, and AD0TRG0 bits = 000, AD0CTL0.AD0MD1 and AD0CTL0.AD0MD0 bits = 00, and AD0CHEN register = 0004H.

13.4 Operation

13.4.1 Basic operation

<1> Set the AD2M0.AD2PS bit to 1 to turn on A/D power while the AD2M0.AD2CE bit = 0.
At this time, bits other than the AD2M0.AD2CE bit can be simultaneously set.

<2> Select an operation mode of A/D conversion and A/D conversion time by using the AD2M0, AD2M1, and AD2S registers.

<3> Setting the AD2M0.AD2CE bit to 1 (enable conversion) at least 2 μs after turning on A/D power (AD2M0.AD2PS bit = 0 $\rightarrow$ 1) starts A/D conversion.
If the AD2CE bit is set to 1 before 2 μs passes, the conversion operation is started and ends after A/D conversion time, but the conversion result is undefined.

<4> When A/D conversion is started, the voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<5> When sampling has been performed for a specific time, the sample & hold circuit enters the hold status, and holds the input analog voltage until A/D conversion ends.

<6> Set bit 9 of the successive approximation register (SAR) and changes the level of the voltage tap of the D/A converter to the reference voltage ($1/2AV_{DD2}$).

<7> The voltage generated by the voltage tap of the D/A converter is compared with the analog input voltage by a voltage comparator. If the analog input voltage is found to be greater than ($1/2AV_{DD2}$) as a result of comparison, the MSB of the SAR register remains set. If the analog input voltage is less than ($1/2AV_{DD2}$), the MSB is reset.

<8> Next, bit 8 of the SAR register is automatically set, and the next comparison is started. The voltage tap of the D/A converter is selected according to the value of bit 9, to which the result has been already set as shown below.

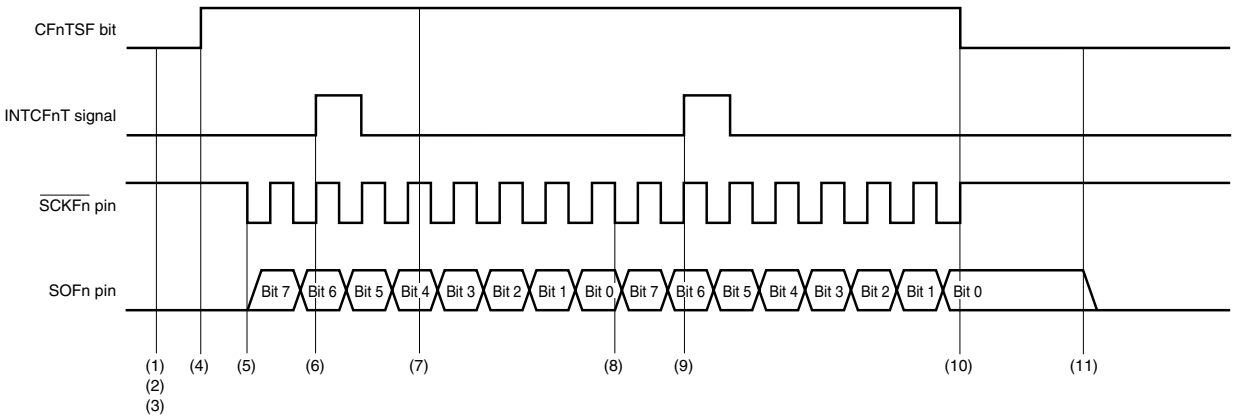
Bit 9 = 1: ($3/4AV_{DD2}$)
Bit 9 = 0: ($1/4AV_{DD2}$)

The voltage tap of the D/A converter and the analog input voltage are compared and bit 8 of the SAR register is manipulated according to the result of the comparison as shown below.

Analog input voltage $\geq$ Voltage tap of D/A converter: Bit 8 = 1
Analog input voltage $\leq$ Voltage tap of D/A converter: Bit 8 = 0

Comparison is continued like this to bit 0 of the SAR register.

(2) Operation timing



(1) Write 07H to the CFnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKFn}$), and slave mode.

(2) Write 00H to the CFnCTL2 register, and set the transfer data length to 8 bits.

(3) Write C3H to the CFnCTL0 register, and select the transmission mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) The CFnSTR.CFnTSF bit is set to 1 by writing the transmit data to the CFnTX register, and the device waits for a serial clock input.

(5) When a serial clock is input, output the transmit data from the SOFn pin in synchronization with the serial clock.

(6) When transfer of the transmit data from the CFnTX register to the shift register is ended and writing to the CFnTX register is enabled, the transmission enable interrupt request signal (INTCFnT) is generated.

(7) To continue transmission, write the transmit data to the CFnTX register again after the INTCFnT signal is generated.

(8) When a serial clock is input following end of the transmission of the transfer data length set with the CFnCTL2 register, continuous transmission is started.

(9) When transfer of the transmit data from the CFnTX register to the shift register is ended and writing to the CFnTX register is enabled, the INTCFnT signal is generated. To end continuous transmission at the current transmission, do not write to the CFnTX register.

(10) When the clock of the transfer data length set with the CFnCTL2 register is input without writing to the CFnTX register, clear the CFnTSF bit to 0 to end transmission.

(11) To release the transmission enable status, write the CFnCTL0.CFnPWR bit = 0 and the CFnCTL0.CFnTXE bit = 0 after checking that the CFnTSF bit = 0.

Caution In continuous transmission mode, the reception end interrupt request signal (INTCFnR) is not generated.

Remark n = 0 to 2

18.3.9 DMA trigger factor register n (DTFRn)

This 16-bit register is used to control DMA transfer start triggers generated by interrupt requests from on-chip peripheral I/O.

The interrupt requests set by using this registers serve as DMA transfer start triggers.

The DTFRn register can be read or written in 16-bit units.

The DTFRnH register is the higher 8 bits of the DTFRn register and the DTFRnL register is the lower 8 bits of the DTFRn register. These registers can be read and written in 8-bit units.

Reset sets these registers to 0000H.

Cautions 1. To change the IFCn0 to IFCn6 bits of the DTFRn register (except for clearing the DFn/DFm bit), disable DMA channel n for which the IFCn0 to IFCn6 bits are to be changed, and all other DMA channels having a priority lower than channel n (clear the DCHC.ENn bit or the DEN.ENnn bit to 0 and the ENm/ENmm bit to 0). To enable the DMA operation after changing the IFCn0 to IFCn6 bits of the DTFRn register (ENn/ENnn/ENm/ENmm bit = 1), be sure to clear the DFn/DFm bit.

Unless these conditions are satisfied, DMA channel m may perform the following operation.

- **DMAm transfer is started even when a DMAm start trigger is not generated.**
- **DMAm transfer is not started even when a DMAm start trigger is generated.**

2. To overwrite the same value to the DTFRn register, disable the operation of DMA channel n corresponding to the DTFRn register to which the same value is to be written (ENn/ENnn bit = 0). The operation of DMA channel m that has a priority lower than DMA channel n does not have to be disabled.

3. If data is written to the DTFRn register, a DMAn start request that is generated while the corresponding DMA channel n is held pending or while data is being written to the register, regardless of whether the DMA operation of DMA channel n is enabled or disabled, and regardless of the value set to the DTFRn register, is cleared.

4. If a DMA transfer start trigger is input while DMA is suspended (when the DCHC.ENn bit or DEN.ENnn bit = 0, or DCHC.STPn bit or DMSTP.STPnn bit = 1), the start trigger is held pending.

The pending start trigger is re-activated when the DMA operation is enabled (ENn/ENnn bit = 1, STPn/STPnn bit = 0) and DMA transfer is started.

5. Do not change the DTFRn register setting from the start of DMA transfer until the end of the specified number of DMA transfers. If this register setting is changed, the operation is not guaranteed.

6. While DMA transfer is pending because the bus mastership has been lost or because the transfer request has a low priority, only one start trigger is pended, even if two or more DMA start triggers have been generated and are waiting.

7. An interrupt request input from on-chip peripheral I/O during standby (IDLE or STOP mode) is held pending as a DMA transfer start trigger. The pending DMA start trigger is executed once the system returns to normal mode.

8. If the same start trigger is specified for multiple DMA channels, that DMA transfer start trigger will be enabled for all the specified channels at the same time. In this case, DMA transfer will be performed in order from the DMA channel with the highest priority.

Remark n = 0 to 6, m = 1 to 6, n < m (the priority of DMAn is higher than DMAm)

(7) Registers that must not be set under certain conditions

The following registers must not be written to when a specific operation is performed. If these registers are written to, the operation cannot be guaranteed.

Status	Register That Must Not Be Set
Stop (ENn/ENnn bit = 0)	None
During operation (ENn/ENnn bit = 1)	DADCn[Note 1], DTFRn
During suspension[Note 2] (STPn/STPnn bit = 1)	DADCn[Note 1], DTFRn

Notes 1. The same value may be written to the register.

2. Setting the register is prohibited when the operation that was suspended is resumed. The register can be set when the operation is stopped (ENn/ENnn bit = 0) after the register is written.

Remark n = 0 to 6

Table 25-6. Wiring Correspondence Between Dedicated Flash Memory Programmer and V850E/IG4, V850E/IH4 (1/2)

Pin No.	Dedicated Flash Memory Programmer (PG-FP4 or PG-FP5)	I/O (PG-FP4 or PG-FP5 Side)	V850E/IG4, V850E/IH4			
			Pin Name	Pin No.		
				IG4		IH4
				GC	GF	GF
1	GND	–	V_{SS0}	38	66	81
			V_{SS1}	64	92	117
			V_{SS2}	91	19	28
			EV_{SS0}	41	69	85
			EV_{SS1}	63	91	116
			EV_{SS2}	100	28	38
			EV_{SS3}	–	–	8
			EV_{SS4}	–	–	74
			AV_{SS0}	5	33	43
			AV_{SS1}	10	38	48
			AV_{SS2}	27	55	66
2	$\overline{\text{RESET}}$	Output	$\overline{\text{RESET}}$	39	67	82
3	SI/RxD	Input	TXDA0	47	75	97
4	V_{DD}	–	EV_{DD0}	40	68	83
			EV_{DD1}	62	90	115
			EV_{DD2}	99	27	37
			EV_{DD3}	–	–	7
			FV_{DD}	–	–	114
			AV_{DD0}	7	35	45
			AV_{DD1}	8	36	46
			AV_{DD2}	26	54	65
			AV_{REFP0}	6	34	44
			AV_{REFP1}	9	37	47
5	SO/TxD	Output	RXDA0	46	74	96
6	V_{PP}	×	NC	–	–	–
7	SCK	×	NC	–	–	–
8	H/S	×	NC	–	–	–
9	CLK[Note]	Output	X1[Note]	36	64	79
10	VDE	×	NC	–	–	–

Note In the V850E/IG4 and V850E/IH4, external clock input is prohibited. Mount the resonator on board.

Remark NC: No Connection
IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

Table 25-7. Wiring Correspondence Between Dedicated Flash Memory Programmer and V850E/IG4, V850E/IH4 (1/2)

Pin No.	Dedicated Flash Memory Programmer (PG-FP4 or PG-FP5)	I/O (PG-FP4 or PG-FP5 Side)	V850E/IG4, V850E/IH4			
			Pin Name	Pin No.		
				IG4		IH4
				GC	GF	GF
1	GND	–	V_{SS0}	38	66	81
			V_{SS1}	64	92	117
			V_{SS2}	91	19	28
			EV_{SS0}	41	69	85
			EV_{SS1}	63	91	116
			EV_{SS2}	100	28	38
			EV_{SS3}	–	–	8
			EV_{SS4}	–	–	74
			AV_{SS0}	5	33	43
			AV_{SS1}	10	38	48
			AV_{SS2}	27	55	66
2	$\overline{\text{RESET}}$	Output	$\overline{\text{RESET}}$	39	67	82
3	SI/RxD	Output	SOF0	47	75	97
4	V_{DD}	–	EV_{DD0}	40	68	83
			EV_{DD1}	62	90	115
			EV_{DD2}	99	27	37
			EV_{DD3}	–	–	7
			FV_{DD}	–	–	114
			AV_{DD0}	7	35	45
			AV_{DD1}	8	36	46
			AV_{DD2}	26	54	65
			AV_{REFP0}	6	34	44
			AV_{REFP1}	9	37	47
5	SO/TxD	Output	SIF0	46	74	96
6	V_{PP}	×	NC	–	–	–
7	SCK	Output	$\overline{\text{SCKF0}}$	48	76	98
8	H/S	×	NC	–	–	–
9	CLK[Note]	Output	X1[Note]	36	64	79
10	VDE	×	NC	–	–	–

Note In the V850E/IG4 and V850E/IH4, external clock input is prohibited. Mount the resonator on board.

Remark NC: No Connection
IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

Table 25-7. Wiring Correspondence Between Dedicated Flash Memory Programmer and V850E/IG4, V850E/IH4 (2/2)

Pin No.	Dedicated Flash Memory Programmer (PG-FP4 or PG-FP5)	I/O (PG-FP4 or PG-FP5 Side)	V850E/IG4, V850E/IH4			
			Pin Name	Pin No.		
				IG4		IH4
				GC	GF	GF
11	V_{DD2}	–	V_{DD0}	35	63	78
			V_{DD1}	65	93	118
			V_{DD2}	90	18	27
			V_{DD3}	–	–	77
12	FLMD1	Output	**Note**	76	4	1
13	RFU-1	×	NC	–	–	–
14	FLMD0	Output	FLMD0	42	70	86
15	Not used	×	NC	–	–	–
16	Not used	×	NC	–	–	–

Note Connect to FLMD1 or GND by way of a resistor.

Remark NC: No Connection
IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 18**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 18, 20**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					

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Edition	Description	Applied to:
2nd	Modification of description in **24.2.4 Cautions**	**CHAPTER 24 ON-CHIP DEBUG FUNCTION**
	Addition of **25.2 Memory Configuration**	**CHAPTER 25 FLASH MEMORY**
	Addition of description to **25.3 Functional Overview**	
	Modification of description in **25.9 Rewriting by Self Programming**	
	Modification of description in **26.1.3 Operating conditions**	**CHAPTER 26 ELECTRICAL SPECIFICATIONS**
	Modification of description in **26.1.4 Clock oscillator characteristics**	
	Modification of description in **26.1.5 DC characteristics**	
	Modification of description in **26.1.7 (5) UARTB timing**	
	Modification of description in **26.1.8 Characteristics of A/D converters 0 and 1**	
	Modification of description in **26.1.9 Characteristics of A/D converter 2**	
	Modification of description in **26.1.11 Comparator characteristics**	
	Modification of description in **26.1.12 Power-on-clear circuit (POC)**	
	Modification of description in **26.1.13 Low-voltage detector (LVI)**	
	Addition of **26.1.14 Supply voltage application/cutoff timing**	
	Modification of description in **26.1.15 Flash memory programming characteristics**	
	Modification of description in **26.2.3 Operating conditions**	
	Modification of description in **26.2.4 Clock oscillator characteristics**	
	Modification of description in **26.2.5 DC characteristics**	
	Modification of description in **26.2.7 (5) UARTB timing**	
	Modification of description in **26.2.8 Characteristics of A/D converters 0, 1**	
	Modification of description in **26.2.9 Characteristics of A/D converter 2**	
	Modification of description in **26.2.11 Comparator characteristics**	
	Modification of description in **26.2.12 Power-on-clear circuit (POC)**	
	Modification of description in **26.2.13 Low-voltage detector (LVI)**	
	Addition of **26.2.14 Supply voltage application/cutoff timing**	
	Modification of description in **26.2.15 Flash memory programming characteristics**	
	Modification of description in **CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**	**CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**
	Addition of **APPENDIX D REVISION HISTORY**	**APPENDIX D REVISION HISTORY**