Renesas Electronics America Inc - UPD70F3916GF(R)-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3916gf-r-gat-ax

1.2 Features

- Minimum instruction execution time:
  10 ns (at internal 100 MHz operation)

- General-purpose registers: 32 bits × 32

- CPU features: Signed multiplication (16 bits × 16 bits → 32 bits or 32 bits × 32 bits → 64 bits): 1 to 2 clocks
  Saturated operation instructions (with overflow/underflow detection function)
  32-bit shift instructions: 1 clock
  Bit manipulation instructions
  Load/store instructions with long/short format
  Signed load instructions

- Internal memory: RAM: 24 KB (See **Table 1-1**)
  Flash memory: 256/384/480 KB (See **Table 1-1**)

- On-chip debug function: Supports MINICUBE®, MINICUBE2.

- Interrupts/exceptions:
  Non-maskable interrupts: 1 source (external: none, internal: 1)
  Maskable interrupts: 103 sources (external: 22, internal: 81)
  Software exceptions: 32 sources
  Exception traps: 2 sources

- DMA controller: 7 channels
  Transfer unit: 8 bits/16 bits/32 bits
  Maximum transfer count: 4096 (2^{12})
  Transfer type: 2-cycle
  Transfer modes: Single/single step
  Transfer targets: On-chip peripheral I/O ↔ Internal RAM
  Transfer request: On-chip peripheral I/O/software
  Next address setting function

- I/O lines: V850E/IG4: Total: 67 (Input ports: 12, I/O ports: 55)
  V850E/IH4: Total: 80 (Input ports: 12, I/O ports: 68)

(9) TAAn counter read buffer register (TAAnCNT)

The TAAnCNT register is a read buffer register that can read the count value of the 16-bit counter.

If this register is read when the TAAnCTL0.TAAnCE bit = 1, the count value of the 16-bit timer can be read.

This register is read-only, in 16-bit units.

The value of the TAAnCNT register is cleared to 0000H when the TAAnCE bit = 0. If the TAAnCNT register is read at this time, the value of the 16-bit counter (FFFFH) is not read, but 0000H is read.

The value of the TAAnCNT register is cleared to 0000H after reset, and the TAAnCE bit is cleared to 0.

After reset: 0000H R Address: TAA0CNT FFFFF66AH, TAA1CNT FFFFF68AH, TAA2CNT FFFFF6AAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAAnCNT																

(n = 0 to 2)

6.5 Timer Output Operations

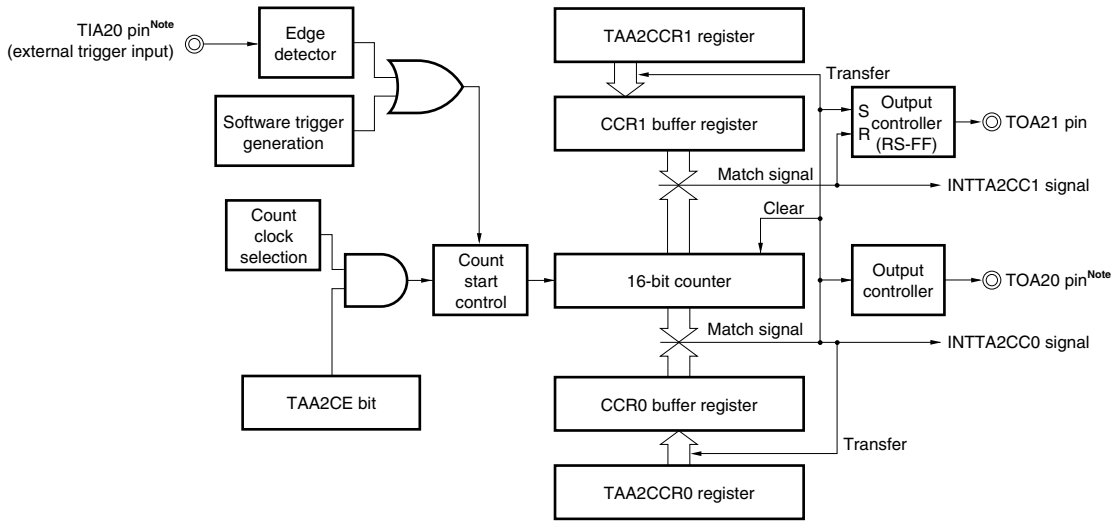
The following table shows the operations and output levels of the TOAn0 and TOAn1 pins.

Table 6-6. Timer Output Control in Each Mode

Operation Mode	TOAn1 Pin	TOAn0 Pin
Interval timer mode	PWM output	
External event count mode	None	
External trigger pulse output mode	External trigger pulse output	PWM output
One-shot pulse output mode	One-shot pulse output	
PWM output mode	PWM output	
Free-running timer mode	PWM output (only when compare function is used)	
Pulse width measurement mode	None	

Remark n = 0 to 2

Figure 6-23. Configuration of TAA2 in External Trigger Pulse Output Mode

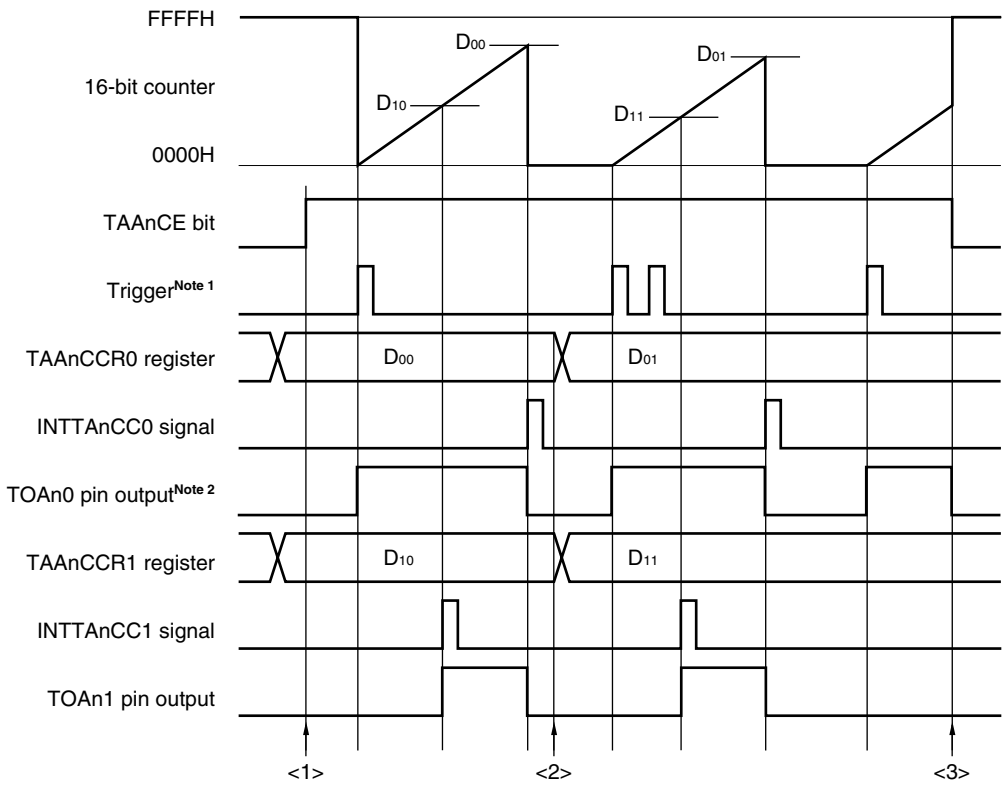


Note Because the external trigger input pin (TIA20) and timer output pin (TOA20) are the same pin, the two functions cannot be used at the same time.

Caution In the external trigger pulse output mode, select the internal clock as the count clock (by clearing the TAA2CTL1.TAA2EEE bit to 0).

(1) Operation flow in one-shot pulse output mode

Figure 6-31. Software Processing Flow in One-Shot Pulse Output Mode (1/2)



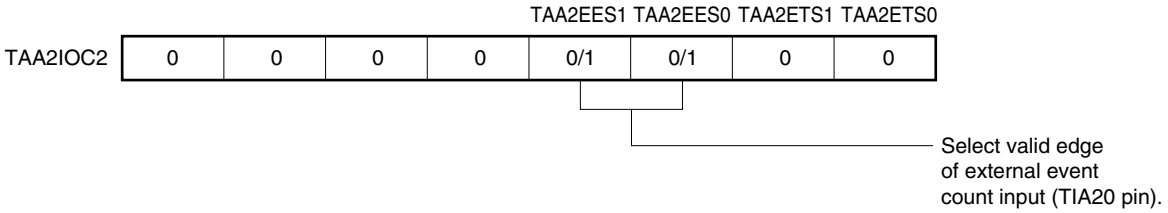
Notes 1. A software trigger for TAA0 and TAA1, and an external trigger input (from the TIA20 pin) for TAA2

2. For TAA2, this function can only be used by using a software trigger.

Remark n = 0 to 2

Figure 6-35. Register Setting in PWM Output Mode (2/2)

(d) TAA2 I/O control register 2 (TAA2IOC2)



(e) TAAn counter read buffer register (TAAnCNT)

The value of the 16-bit counter can be read by reading the TAAnCNT register.

(f) TAAn capture/compare registers 0 and 1 (TAAnCCR0 and TAAnCCR1)

If D_0 is set to the TAAnCCR0 register and D_1 to the TAAnCCR1 register, the cycle and active level of the PWM waveform are as follows.

Cycle = (D_0 + 1) × Count clock cycle

Active level width = D_1 × Count clock cycle

Remarks 1. TAA2 I/O control register 1 (TAA2IOC1) and TAAn option register 0 (TAAnOPT0) are not used in the PWM output mode.

2. n = 0 to 2

a = 0, 1

8.4 Registers

(1) TMTn control register 0 (TTnCTL0)

The TTnCTL0 register is an 8-bit register that controls the operation of TMTn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TTnCTL0 register by software.

After reset: 00H R/W Address: TT0CTL0 FFFFF580H, TT1CTL0 FFFFF5C0H, TT2CTL0 FFFFF780H, TT3CTL0 FFFFF7C0H

	<7>	6	5	4	3	2	1	0
TTnCTL0 (n = 0 to 3)	TTnCE	0	0	0	0	TTnCKS2	TTnCKS1	TTnCKS0

TTnCE	TMTn operation control
0	TMTn operation disabled (TMTn reset asynchronously[Note])
1	TMTn operation enabled. TMTn operation start

TTnCKS2	TTnCKS1	TTnCKS0	Internal count clock selection
0	0	0	$f_{XX}/2$
0	0	1	$f_{XX}/4$
0	1	0	$f_{XX}/8$
0	1	1	$f_{XX}/32$
1	0	0	$f_{XX}/256$
1	0	1	$f_{XX}/1024$
1	1	0	$f_{XX}/2048$
1	1	1	$f_{XX}/4096$

Note The TTnOPT0.TTnOVF bit and the 16-bit counter are reset simultaneously. Moreover, timer outputs (TOTn0 and TOTn1 pins) are reset to the TTnIOC0 register set status at the same time as the 16-bit counter is reset.

Cautions 1. Set the TTnCKS2 to TTnCKS0 bits when the TTnCE bit = 0.
When the value of the TTnCE bit is changed from 0 to 1, the TTnCKS2 to TTnCKS0 bits can be set simultaneously.
2. Be sure to set bits 3 to 6 to "0".

Remark f_{XX}: Peripheral clock

(11) TMTn capture/compare register 0 (TTnCCR0)

The TTnCCR0 register is a 16-bit register that can be used as a capture register or compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TTnOPT0.TTnCCS0 bit. In the pulse width measurement mode, the TTnCCR0 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TTnCCR0 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Remark n = 0 to 3

After reset: 0000H R/W Address: TT0CCR0 FFFFF58AH, TT1CCR0 FFFFF5CAH, TT2CCR0 FFFFF78AH, TT3CCR0 FFFFF7CAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTnCCR0 (n = 0 to 3)																

8.6.7 Pulse width measurement mode (TTnMD3 to TTnMD0 bits = 0110)

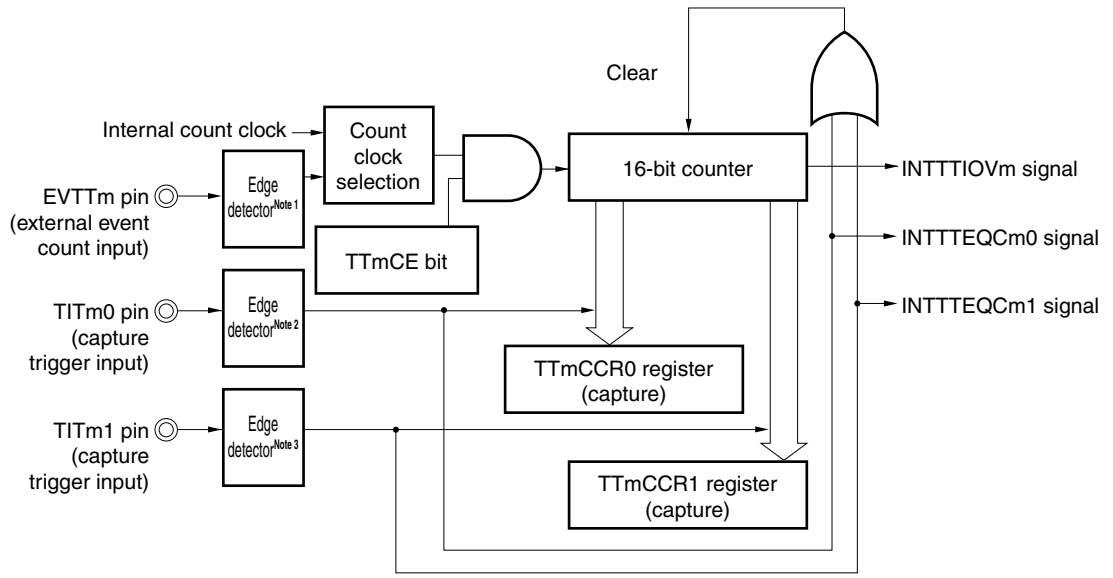
In the pulse width measurement mode, 16-bit timer/event counter T starts counting when the TTnCTL0.TTnCE bit is set to 1. Each time the valid edge input to the TITna pin has been detected, the count value of the 16-bit counter is stored in the TTnCCRa register, and the 16-bit counter is cleared to 0000H.

The interval of the valid edge can be measured by reading the TTnCCRa register after a capture interrupt request signal (INTTTEQCna) occurs.

As shown in Figure 8-46, select either the TITn0 or TITn1 pin as the capture trigger input pin and set the unused pins to “No edge detection” by using the TTnIOC1 register.

Remark n = 0 to 3
a = 0, 1

Figure 8-44. Configuration of TMT0 and TMT1 in Pulse Width Measurement Mode



Notes 1. Set by the TTmIOC2.TTmEES1 and TTmIOC2.TTmEES0 bits.
2. Set by the TTmIOC1.TTmIS1 and TTmIOC1.TTmIS0 bits.
3. Set by the TTmIOC1.TTmIS3 and TTmIOC1.TTmIS2 bits.

Remark m = 0, 1

11.3 Control Registers

(1) Watchdog timer mode register (WDTM)

The WDTM register sets the overflow time and operation clock of the watchdog timer.

This register can be read or written in 8-bit units. This register can be read any number of times, but can be written only once following reset release; it cannot then be written a second or subsequent time.

Reset sets this register to 67H.

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4	3	2	1	0
WDTM	0	WDM1	WDM0	0	0	WDCS2	WDCS1	WDCS0

WDM1	WDM0	Selection of operation mode of watchdog timer
0	0	Stop operation
0	1	Non-maskable interrupt request mode (generation of INTWDT signal)
1	×	Reset mode (generation of WDTRES signal)

Cautions 1. For details of the WDCS2 to WDCS0 bits, see Table 11-2 Overflow Time.

2. If the WDTM register is rewritten while the watchdog timer is counting, the counter of the watchdog timer is cleared to 0000H.

3. Be sure to clear bits 3, 4, and 7 to "0".

Table 11-2. Overflow Time

WDCS2	WDCS1	WDCS0	Overflow Time	f_{XX} = 100 MHz
0	0	0	$2^{19}/f_{XX}$	5.2 ms
0	0	1	$2^{20}/f_{XX}$	10.5 ms
0	1	0	$2^{21}/f_{XX}$	21.0 ms
0	1	1	$2^{22}/f_{XX}$	41.9 ms
1	0	0	$2^{23}/f_{XX}$	83.9 ms
1	0	1	$2^{24}/f_{XX}$	167.8 ms
1	1	0	$2^{25}/f_{XX}$	335.5 ms
1	1	1	$2^{26}/f_{XX}$	671.1 ms

14.2.1 Pin functions of each channel

The input and output pins used by UARTA in the V850E/IG4 and V850E/IH4 are alternately used for other functions as shown in Table 14-2. To use these pins for UARTA, set up the related registers as described in **Table 4-16 Settings When Pins Are Used for Alternate Functions**.

Table 14-2. Pins Used by UARTA

Channel	Pin No.			Port	UARTA Reception Input	UARTA Transmission Output	Other Functions
	IG4		IH4				
	GC	GF	GC				
UARTA0	46	74	96	P40	RXDA0	–	SIF0/DDI/TOA00
	47	75	97	P41	–	TXDA0	SOF0
UARTA1	54	82	106	P30	RXDA1	–	SCL
	55	83	107	P31	–	TXDA1	SDA
UARTA2	56	84	108	P32	RXDA2	–	SIF1
	57	85	109	P33	–	TXDA2	SOF1

Remark IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

16.3 Mode Switching Between CSIF and Other Serial Interface

16.3.1 Mode switching between CSIF0 and UARTA0

In the V850E/IG4 and V850E/IH4, CSIF0 and UARTA0 share a pin, and these functions cannot be used at the same time. To use the pin for the CSIF0 function, set up the PMC4, PFC4, and PFCE4 registers in advance.

Switching the operation mode between CSIF0 and UARTA0, the serial interfaces, is described below.

Caution The operations related to transmission and reception of CSIF0 or UARTA0 are not guaranteed if the operation mode is switched during transmission or reception. Be sure to disable the unit that is not used.

Figure 16-2. Operation Mode Switch Settings of CSIF0 and UARTA0

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	PMC44	PMC43	PMC42	PMC41	PMC40

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	0	0	0	0	PFC43	0	PFC41	PFC40

After reset: 00H R/W Address: FFFFF708H

	7	6	5	4	3	2	1	0
PFCE4	0	0	0	0	0	PFCE42	0	PFCE40

PMC42	PFCE42	Operation mode
0	×	Port I/O mode
1	0	$\overline{\text{SCKF0}}$

PMC4n	PFC4n	Operation mode
0	×	Port I/O mode
1	0	CSIF0 mode
1	1	UARTA0 mode

Remarks 1. n = 0, 1

2. × = 0 or 1

(1) IIC control register 0 (IICC0)

The IICC0 register is used to enable/stop I²C operations, set wait timing, and set other I²C operations.

The IICC0 register can be read or written in 8-bit or 1-bit units. However, set the SPIE0, WTIM0, and ACKE0 bits when the IICE0 bit is 0 or during the wait period. When setting the IICE0 bit from "0" to "1", these bits can also be set at the same time.

Reset sets this register to 00H.

(1/4)

After reset: 00H R/W Address: FFFFFD82H

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I²C operation enable/disable specification
0	Stop operation. Reset the IICS0 register[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit to 1 when the SCL and SDA lines are high level.	
Condition for clearing (IICE0 bit = 0)	Condition for setting (IICE0 bit = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Note 2]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL and SDA lines are set to high impedance. The STT0, SPT0, IICS0.MSTS0, IICS0.EXC0, IICS0.COI0, IICS0.TRC0, IICS0.ACKD0, and IICS0.STD0 bits are cleared to 0.
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 bit = 0)	Condition for setting (LREL0 bit = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICS0 register, and the IICF0.STCF0, IICF0.IICBSY0, IICCL0.CLD0, and IICCL0.DAD0 bits are reset.

2. This flag's signal is invalid when the IICE0 bit = 0.

Caution If the I²C operation is enabled (IICE0 bit = 1) when the SCL line is high level and the SDA line is low level, the start condition is detected immediately. To avoid this, after enabling the I²C operation, immediately set the LREL0 bit to 1 with a bit manipulation instruction.

The following shows an example of the processing of the slave device by an INTIIC interrupt (it is assumed that no extension codes are used here). During an INTIIC interrupt, the status is confirmed and the following steps are executed.

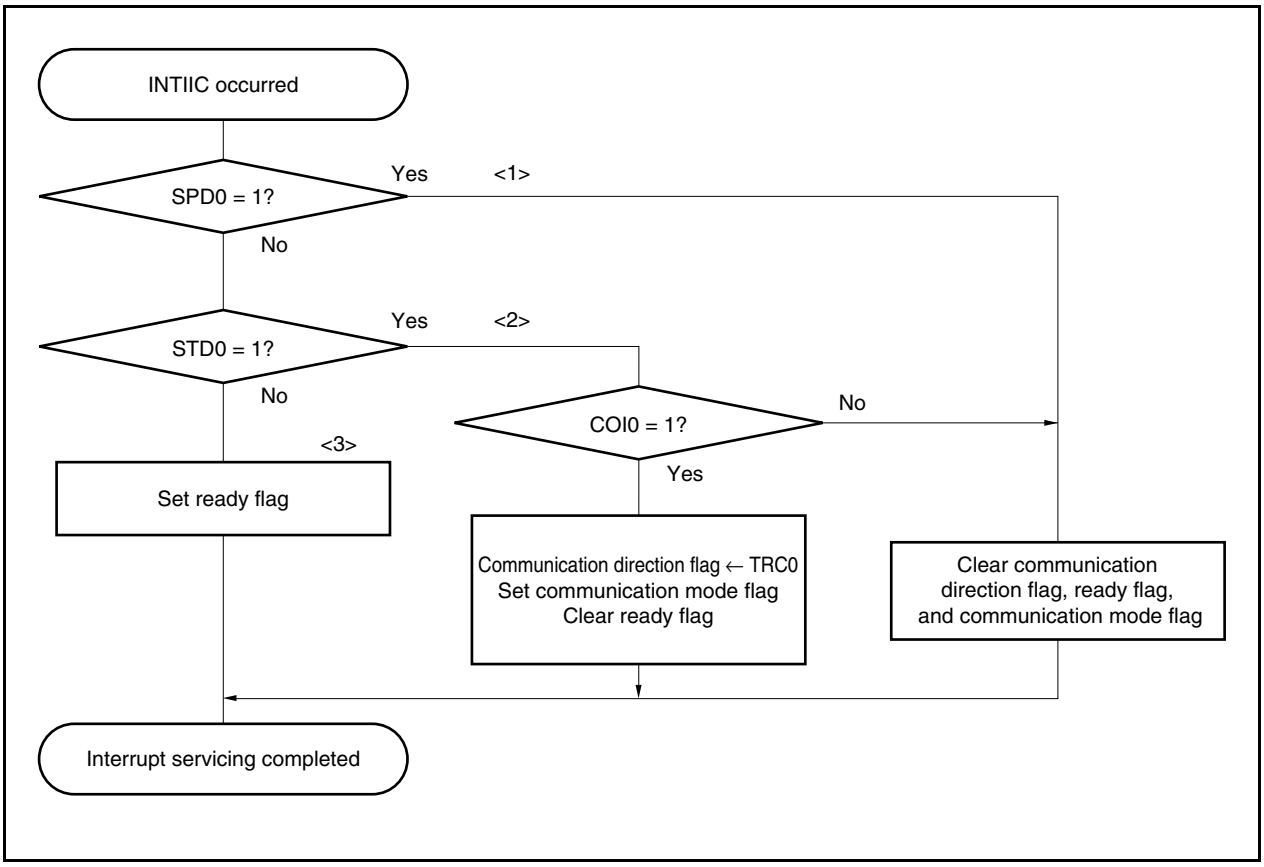
<1> When a stop condition is detected, communication is terminated.

<2> When a start condition is detected, the address is confirmed. If the address does not match, communication is terminated. If the address matches, the communication mode is set and wait is released, and operation returns from the interrupt (the ready flag is cleared).

<3> For data transmission/reception, when the ready flag is set, operation returns from the interrupt while the I²C bus remains in the wait status.

Remark <1> to <3> in the above correspond to <1> to <3> in **Figure 17-20 Slave Operation Flowchart (2)**.

Figure 17-20. Slave Operation Flowchart (2)



17.17 Timing of Data Communication

When using I²C bus mode, the master device generates an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the IICS0.TRC0 bit that specifies the data transfer direction and then starts serial communication with the slave device.

The IIC0 register's shift operation is synchronized with the falling edge of the serial clock (SCL pin). The transmit data is transferred to the SO latch and is output (MSB first) via the SDA pin.

Data input via the SDA pin is captured by the IIC0 register at the rising edge of the SCL pin.

The data communication timing is shown below.

CHAPTER 23 POWER-ON CLEAR CIRCUIT

23.1 Function

Functions of the power-on-clear circuit (POC) are shown below.

- Generates a reset signal (POCRES) upon power application.
- Compares the supply voltage (V850E/IG4: EV_{DD0}, EV_{DD1}, EV_{DD2}, V850E/IH4: FV_{DD}) and detection voltage (V_{POC0}), and generates a reset signal when the supply voltage drops below the detection voltage (detection voltage (V_{POC0}): 3.7 V ±0.2 V).

Remark The V850E/IG4 and V850E/IH4 have the reset source flag register (RESF) that indicates generation of a reset signal (WDTRES) by watchdog timer overflow and a reset signal (LVIRES) by low-voltage detector (LVI).
The RESF register is not cleared to 00H when a reset signal (WDTRES or LVIRES) is generated, and its flag corresponding to the reset source is set to 1.
The RESF register is cleared (00H) when a reset signal (POCRES) by power-on-clear circuit (POC) is generated.
For details of the RESF register, see **CHAPTER 21 RESET FUNCTIONS**.

Table 25-8. Wiring Correspondence Between Dedicated Flash Memory Programmer and V850E/IG4, V850E/IH4 (1/2)

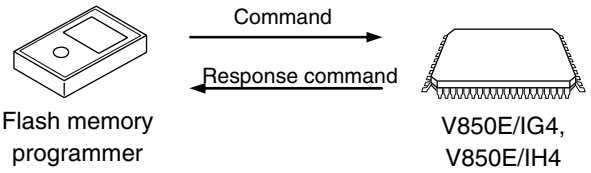
Pin No.	Dedicated Flash Memory Programmer (PG-FP4 or PG-FP5)	I/O (PG-FP4 or PG-FP5 Side)	V850E/IG4, V850E/IH4			
			Pin Name	Pin No.		
				IG4		IH4
				GC	GF	GF
1	GND	–	V_{SS0}	38	66	81
			V_{SS1}	64	92	117
			V_{SS2}	91	19	28
			EV_{SS0}	41	69	85
			EV_{SS1}	63	91	116
			EV_{SS2}	100	28	38
			EV_{SS3}	–	–	8
			EV_{SS4}	–	–	74
			AV_{SS0}	5	33	43
			AV_{SS1}	10	38	48
			AV_{SS2}	27	55	66
2	$\overline{\text{RESET}}$	Output	$\overline{\text{RESET}}$	39	67	82
3	SI/RxD	Input	SOF0	47	75	97
4	V_{DD}	–	EV_{DD0}	40	68	83
			EV_{DD1}	62	90	115
			EV_{DD2}	99	27	37
			EV_{DD3}	–	–	7
			FV_{DD}	–	–	114
			AV_{DD0}	7	35	45
			AV_{DD1}	8	36	46
			AV_{DD2}	26	54	65
			AV_{REFP0}	6	34	44
			AV_{REFP1}	9	37	47
5	SO/TxD	Output	SIF0	46	74	96
6	V_{PP}	×	NC	–	–	–
7	SCK	Output	$\overline{\text{SCKF0}}$	48	76	98
8	H/S	Input	P44	50	78	100
9	CLK[Note]	Output	X1[Note]	36	64	79
10	VDE	×	NC	–	–	–

Note In the V850E/IG4 and V850E/IH4, external clock input is prohibited. Mount the resonator on board.

Remark NC: No Connection
IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

25.8.3 Communication commands

The V850E/IG4 and V850E/IH4 communicate with a flash memory programmer by means of commands. The commands sent from the flash memory programmer to the V850E/IG4 or V850E/IH4 are called “commands”. The response signals sent from the V850E/IG4 or V850E/IH4 to the flash memory programmer are called “response commands”.



The following shows the commands for flash memory control in the V850E/IG4 and V850E/IH4. All of these commands are issued from the dedicated flash memory programmer, and the V850E/IG4 and V850E/IH4 perform the processing corresponding to the commands.

Table 25-10. Flash Memory Control Commands

Classification	Command Name	Support			Function
		UARTA0	CSIF0	**Note**	
Blank check	Block blank check command	√	√	√	Checks if the contents of the memory in the specified block have been correctly erased.
Erase	Chip erase command	√	√	√	Erases the contents of the entire memory.
	Block erase command	√	√	√	Erases the contents of the memory of the specified block.
Write	Program command	√	√	√	Writes the specified address range, and executes a contents verify check.
Verify	Verify command	√	√	√	Compares the contents of memory in the specified address range with data transferred from the flash memory programmer.
	Checksum command	√	√	√	Reads the checksum in the specified address range.
System setting and control	Silicon signature command	√	√	√	Reads silicon signature information.
	Security setting command	√	√	√	Prohibits the chip erase command, block erase command, program command, read command, and boot area rewrite.

Note CSIF0 supporting handshake

The V850E/IG4 and V850E/IH4 send back response commands for the commands issued from the flash memory programmer. The response commands sent from the V850E/IG4 and V850E/IH4 are listed below.

Table 25-11. Response Commands

Response Command Name	Function
ACK (Acknowledge)	Acknowledges command/data, etc.
NAK (Not acknowledge)	Acknowledges illegal frame, etc.
Command number error	Acknowledges illegal command/data, etc.
Parameter error	Acknowledges illegal parameter, etc.
Checksum error	Acknowledges checksum of frame
Protect error	Acknowledges when protection is in effect
During processing (BUSY)	Acknowledges during processing
Other than above	Error

(6) CSIF timing

(a) Master mode

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = V_{DD2} = 1.35 to 1.65 V,
EV_{DD0} = EV_{DD1} = EV_{DD2} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 4.0 to 5.5 V,
V_{SS0} = V_{SS1} = V_{SS2} = EV_{SS0} = EV_{SS1} = EV_{SS2} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKFn}$ cycle	t_{KCYM}	<22>		125		ns
$\overline{SCKFn}$ high-/low-level width	t_{KWHM}, t_{KWLM}	<23>		t_{KCYM}/2 – 10		ns
SIFn setup time (to $\overline{SCKFn}$↑)	t_{SSIM}	<24>		30		ns
SIFn setup time (to $\overline{SCKFn}$↓)				30		ns
SIFn hold time (from $\overline{SCKFn}$↑)	t_{HSIM}	<25>		30		ns
SIFn hold time (from $\overline{SCKFn}$↓)				30		ns
SOFn output delay time (from $\overline{SCKFn}$↓)	t_{DSOM}	<26>			30	ns
SOFn output delay time (from $\overline{SCKFn}$↑)					30	ns
SOFn output hold time (from $\overline{SCKFn}$↑)	t_{HSOM}	<27>		t_{KCYM}/2 – 10		ns
SOFn output hold time (from $\overline{SCKFn}$↓)				t_{KCYM}/2 – 10		ns

Remark n = 0 to 2

(b) Slave mode

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = V_{DD2} =1.35 to 1.65 V,
EV_{DD0} = EV_{DD1} = EV_{DD2} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 4.0 to 5.5 V,
V_{SS0} = V_{SS1} = V_{SS2} = EV_{SS0} = EV_{SS1} = EV_{SS2} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKFn}$ cycle	t_{KCYS}	<28>		125		ns
$\overline{SCKFn}$ high-/low-level width	t_{KWHS}, t_{KWLS}	<29>		t_{KCYS}/2 – 10		ns
SIFn setup time (to $\overline{SCKFn}$↑)	t_{SSIS}	<30>		30		ns
SIFn setup time (to $\overline{SCKFn}$↓)				30		ns
SIFn hold time (from $\overline{SCKFn}$↑)	t_{HSIS}	<31>		30		ns
SIFn hold time (from $\overline{SCKFn}$↓)				30		ns
SOFn output delay time (from $\overline{SCKFn}$↓)	t_{DSOS}	<32>			30	ns
SOFn output delay time (from $\overline{SCKFn}$↑)					30	ns
SOFn output hold time (from $\overline{SCKFn}$↑)	t_{HSOS}	<33>		t_{KCYS}/2 – 10		ns
SOFn output hold time (from $\overline{SCKFn}$↓)				t_{KCYS}/2 – 10		ns

Remark n = 0 to 2

26.1.14 Supply voltage application/cutoff timing

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = V_{DD2} = 1.35 to 1.65 V, EV_{DD0} = EV_{DD1} = EV_{DD2} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 3.5 to 5.5 V, V_{SS0} = V_{SS1} = V_{SS2} = EV_{SS0} = EV_{SS1} = EV_{SS2} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from EV_{DD} rise to V_{DD} rise	t_{RVR}	When using an external reset	–50	50	ms
		When using an internal reset	–50	0	ms
Delay time from EV_{DD} rise to AV_{DD} rise	t_{RAR}	When using an external reset	–50	50	ms
		When using an internal reset	–50	0	ms
Delay time from EV_{DD} rise to $\overline{\text{RESET}}$ rise	t_{RRR}	When using an external reset	T_{osc} + 0.5		ms
Delay time from EV_{DD} fall to V_{DD} fall	t_{FVF}		0	50	ms
Delay time from EV_{DD} fall to AV_{DD} fall	t_{FAF}		0	50	ms

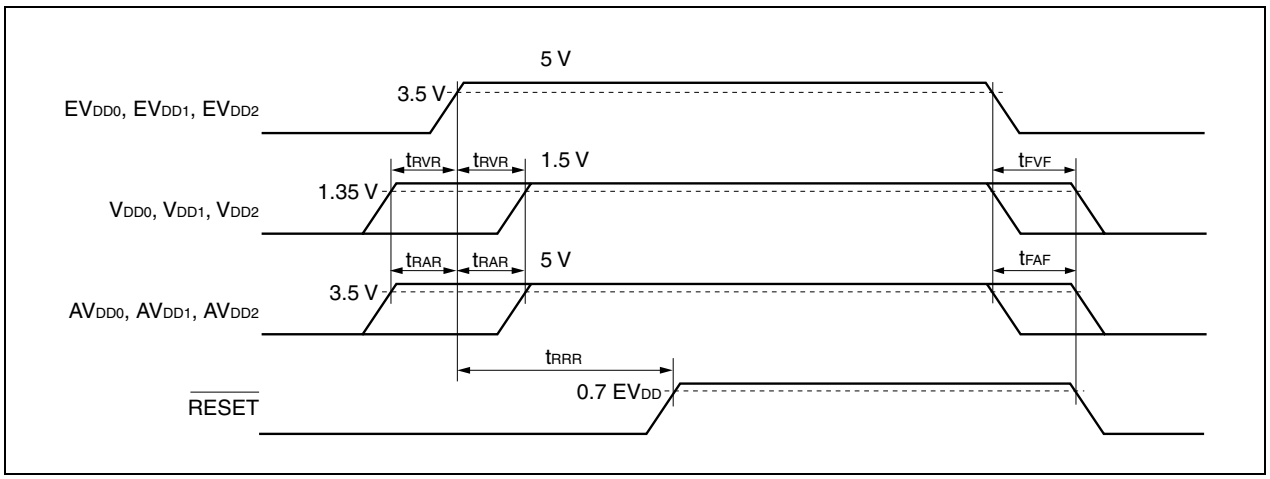
Remark T_{osc}: Oscillation stabilization time

Supply voltage application/cutoff timing

<R> **Cautions 1. There are no regulations for the voltage level and time of EV_{DD0}, EV_{DD1}, EV_{DD2}, V_{DD0}, V_{DD1}, V_{DD2}, AV_{DD0}, AV_{DD1}, and AV_{DD2} in the process of natural discharge after power supply cutoff.**

2. Apply all of the EV_{DD0}, EV_{DD1}, EV_{DD2}, V_{DD0}, V_{DD1}, V_{DD2}, AV_{DD0}, AV_{DD1}, and AV_{DD2} power supplies. It is prohibited to apply one of these power supplies without supplying them all.

(a) External $\overline{\text{RESET}}$ (recommended conditions)



(b) Internal $\overline{\text{RESET}}$ (recommended conditions)