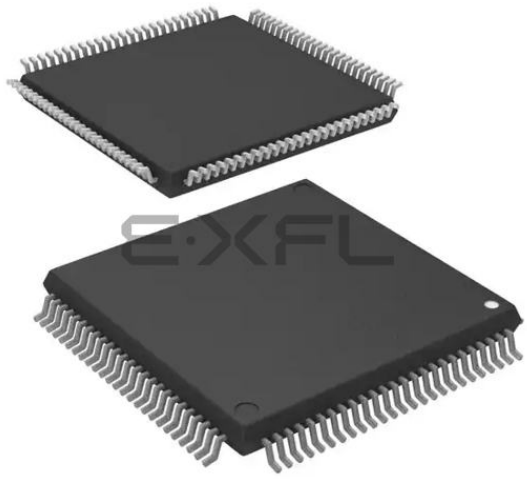

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3917gf-r-gat-ax

(1) Port functions

(1/4)

Function Name	Pin No.			I/O	Function	Alternate Function
	IG4		IH4			
	GC	GF	GF			
P00	89	17	26	I/O	Port 0 (See **4.3.1**.) 8-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected when the pins are in the port mode and input mode, and when the pins function as input pins of the alternate function, and when TOT21 and TOT31 pins go into a high-impedance state).	TECR0/TIT00/TOT00/INTP00
P01	88	16	25			TENC00/EVTT0/INTP01
P02	87	15	24			TENC01/TIT01/TOT01/INTP02
P03	86	14	23			TOT20/TIT20/TOT2OFF/INTP03
P04	85	13	22			TOT21/TIT21/INTP04
P05	84	12	21			TOT30/TIT30/TOT3OFF/INTP05
P06	83	11	20			TOT31/TIT31/INTP06
P07	82	10	19			TOB01OFF/INTP07
P10	98	26	36	I/O	Port 1 (See **4.3.2**.) V850E/IG4: 7-bit I/O port V850E/IH4: 8-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected when the pins are in the port mode and input mode, and when the pins function as input pins of the alternate function, and when TOB0B1 to TOB0B3 and TOB0T1 to TOB0T3 pins (output pins of the alternate function) go into a high-impedance state).	TOB0T1/TIB01/TOB01
P11	97	25	35			TOB0B1/TIB02/TOB02
P12	96	24	34			TOB0T2/TIB03/TOB03
P13	95	23	33			TOB0B2/TIB00
P14	94	22	32			TOB0T3/EVTB0
P15	93	21	31			TOB0B3/TRGB0
P16	92	20	30			TOB00/TOB0OFF/INTP08/ADTRG0/ INTADT0
P17[Note]	–	–	29			–
P20	28	56	67	I/O	Port 2 (See **4.3.3**.) 8-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected when the pins are in the port mode and input mode, and when the pins function as input pins of the alternate function, and when TOB1B1 to TOB1B3 and TOB1T1 to TOB1T3 pins (output pins of the alternate function) go into a high-impedance state).	TOB1T1/TIB11/TOB11
P21	29	57	68			TOB1B1/TIB12/TOB12
P22	30	58	69			TOB1T2/TIB13/TOB13
P23	31	59	70			TOB1B2/TIB10
P24	32	60	71			TOB1T3/EVTB1
P25	33	61	72			TOB1B3/TRGB1
P26	34	62	73			TOB10/TOB1OFF/INTP10/ADTRG1/ INTADT1
P27	43	71	87			INTP09/TOA01

Note V850E/IH4 only

Remark IG4: V850E/IG4
IH4: V850E/IH4
GC (V850E/IG4): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG4): 100-pin plastic LQFP (14 × 20)
GF (V850E/IH4): 128-pin plastic LQFP (fine pitch) (14 × 20)

CHAPTER 3 CPU FUNCTION

The CPU of the V850E/IG4 and V850E/IH4 is based on RISC architecture and executes almost all the instructions in one clock cycle using 5-stage pipeline control.

3.1 Features

- Minimum instruction execution time: 10 ns (at 100 MHz internal operation)
- Thirty-two 32-bit general-purpose registers
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- One-clock 32-bit shift instruction
- Load/store instruction with long/short instruction format
- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

(1) Registers

(a) Port 7 register H, port 7 register L (P7H, P7L)

After reset: Undefined R Address: R7L FFFFFBB0H, R7H FFFFFBB1H

	7	6	5	4	3	2	1	0
P7H	0	0	0	0	P711	P710	P79	P78
P7L	P77	P76	P75	P74	P73	P72	P71	P70

P7n	Control of input data
0	Input low level.
1	Input high level.

Caution When using a port input pin and analog input pin (ANI2n) together, be sure to set the bit (PMC7n) of the PMC7 register to be used as the ANI2n pin to 1.

Remark n = 0 to 11

(b) Port 7 mode control register H, port 7 mode control register L (PMC7H, PMC7L)

After reset: 00H R/W Address: PMC7L FFFFFBB8H, PMC7H FFFFFBB9H

	7	6	5	4	3	2	1	0
PMC7H	0	0	0	0	PMC711	PMC710	PMC79	PMC78
PMC7L	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70

PMC7n	Specification of operating mode of P7n pin
0	Input port (reading P7n enabled. Input buffer is on when this bit is read)
1	ANI2n input (reading P7n disabled. Input buffer is off when this bit is read)

Cautions 1. Do not change to the port mode using A/D converter 2 during A/D conversion.

2. The PMC7H and PMC7L registers enable or disable reading of the P7H and P7L registers, respectively. When the PMC7n bit is 1, the input buffer does not turn on even when the P7H and P7L registers are read. In this case, the read value of the P7n bit is fixed to the low level. This is to prevent through-current that may flow when the ANI2n input (intermediate level) is read.

Remark n = 0 to 11

Table 4-15. Output Data and Port Read Value for Each Setting (1/10)

Port Name	Function	PMCmn	PFCEmn	PFCmn	PMmn	Output Data	Pmn Read Value	Remark
P00, P02	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TECR0, TIT00, TENC01, TIT01	1	0	0	0	–	Port latch	Alternate input (timer input)
					1		Pin level	
	TOT00, TOT01	1	0	1	0	Alternate output (timer output)	Port latch	
					1		Pin level	
	INTP00, INTP02	1	1	0	0	–	Port latch	Alternate input (external interrupt input (necessary to specify valid edge))
					1		Pin level	
P01	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TENC00	1	0	0	0	–	Port latch	Alternate input (timer input)
					1		Pin level	
	EVTT0	1	0	1	0	–	Port latch	Alternate input (timer input)
					1		Pin level	
	INTP01	1	1	0	0	–	Port latch	Alternate input (external interrupt input (necessary to specify valid edge))
					1		Pin level	
P03 to P06	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TOT20, TOT21, TOT30, TOT31	1	0	0	0	Alternate output (timer output)	Port latch	
					1		Pin level	
	TIT20, TIT21, TIT30, TIT31	1	0	1	0	–	Port latch	Alternate input (timer input)
					1		Pin level	

Remark ×: 0 or 1

Table 4-16. Settings When Pins Are Used for Alternate Functions (5/8)

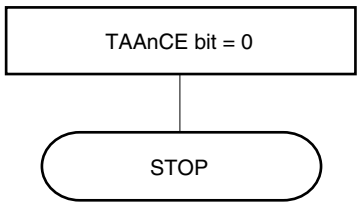
Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bit (Register)
	Name	I/O						
P40	SIF0	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	PMCE40 = 0	PFC40 = 0	
	RXDA0	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	PMCE40 = 0	PFC40 = 1	
	DDI[Note]	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = Setting not required	PFCE40 = Setting not required	PFC40 = Setting not required	
	TOA00	Output	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	PFCE40 = 1	PFC40 = 1	
P41	SOF0	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 0	
	TXDA0	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 1	
P42	$\overline{\text{SCKF0}}$	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	PFCE42 = 0	–	
	DCK[Note]	Input	P42 = Setting not required	PM42 = Setting not required	PMC42 = Setting not required	PFCE42 = Setting not required	–	
	TOA10	Output	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	PFCE42 = 1	–	
P43	INTP13	Input	P43 = Setting not required	PM43 = Setting not required	PMC43 = 1	–	PFC43 = 0	INTF13 (INTF1), INTR13 (INTR1)
	DMS[Note]	Input	P43 = Setting not required	PM43 = Setting not required	PMC43 = Setting not required	–	PFC43 = Setting not required	
	TOA11	Output	P43 = Setting not required	PM43 = Setting not required	PMC43 = 1	–	PFC43 = 1	
P44	INTP14	Input	P44 = Setting not required	PM44 = Setting not required	PMC44 = 1	–	–	INTF14 (INTF1), INTR14 (INTR1)

Note The P40, P42, and P43 pins are also used for on-chip debugging. Switching between the on-chip debug function and port function (including the alternate function) can be done by using the $\overline{\text{DRST}}$ pin level. The following shows the setting method.

Port 4 Functions	
Low-Level Input to $\overline{\text{DRST}}$ Pin	High-Level Input to $\overline{\text{DRST}}$ Pin
P40/SIF0/RXDA0/TOA00	DDI
P42/$\overline{\text{SCKF0}}$/TOA10	DCK
P43/INTP13/TOA11	DMS

Figure 6-11. Software Processing Flow in Interval Timer Mode (2/2)

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TAAnCE bit to 0. The output level of the TOAn0 pin is as specified by the TAAnIOC0 register.

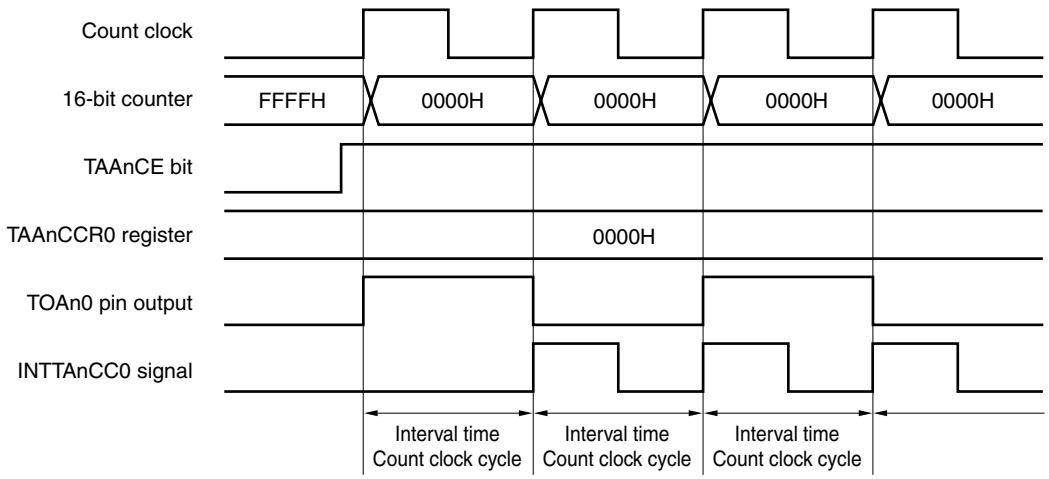
Remark n = 0 to 2

(2) Interval timer mode operation timing

(a) Operation if TAAnCCR0 register is set to 0000H

If the TAAnCCR0 register is set to 0000H, the INTTAnCC0 signal is generated at each count clock, and the output of the TOAn0 pin is inverted.

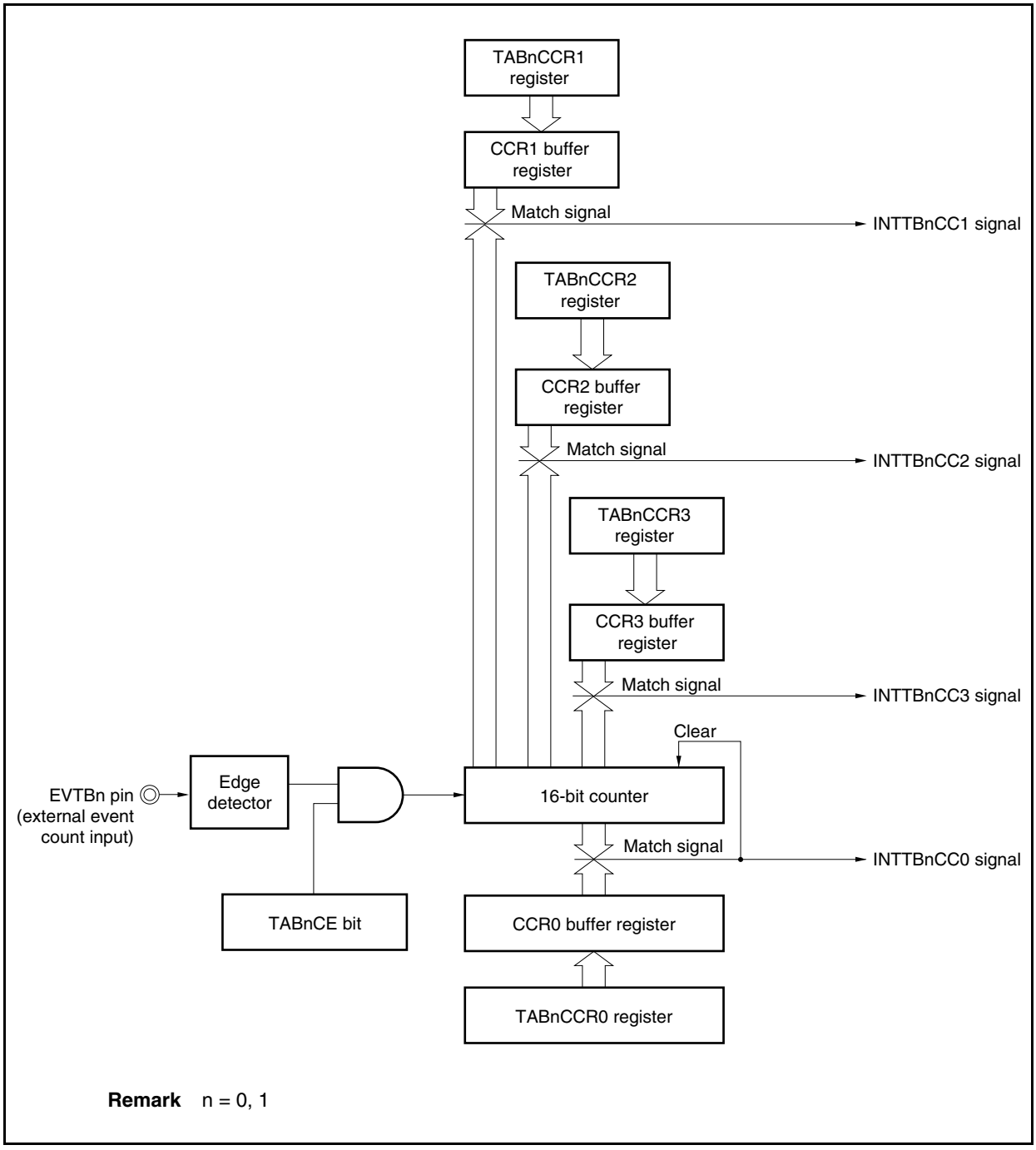
The value of the 16-bit counter is always 0000H.



Remark n = 0 to 2

(e) Operation of TABnCCR1 to TABnCCR3 registers

Figure 7-17. Configuration of TABnCCR1 to TABnCCR3 Registers



Remark n = 0, 1

(2) Operation timing in pulse width measurement mode

(a) Clearing overflow flag

The overflow flag can be cleared to 0 by clearing the TABnOVF bit to 0 with the CLR instruction after reading the TABnOVF bit when it is 1 and by writing 8-bit data (bit 0 is 0) to the TABnOPT0 register after reading the TABnOVF bit when it is 1.

8.3.2 TMT2 and TMT3

TMT2 and TMT3 include the following hardware.

Table 8-2. Configuration of TMT2 and TMT3

Item	Configuration
Timer register	16-bit counter × 1
Registers	TMTk capture/compare registers 0, 1 (TTkCCR0, TTkCCR1) TMTk counter read buffer register (TTkCNT) CCR0 and CCR1 buffer registers
Timer input	2 in total (TITk0 and TITk1 pins)[Note]
Timer output	2 in total (TOTk0 and TOTk1 pins)[Note]
Control registers	TMTk control registers 0, 1 (TTkCTL0, TTkCTL1) TMTk I/O control registers 0 to 2 (TTkIOC0 to TTkIOC2) TMTk option register 0 (TTkOPT0)

Note The TITk0 pin is also used for the capture trigger input signal, the external event count input signal, the external trigger input signal, and as the timer output pin (TOTk0).
The TITk1 pin is also used for the capture trigger input signal and as the timer output pin (TOTk1).

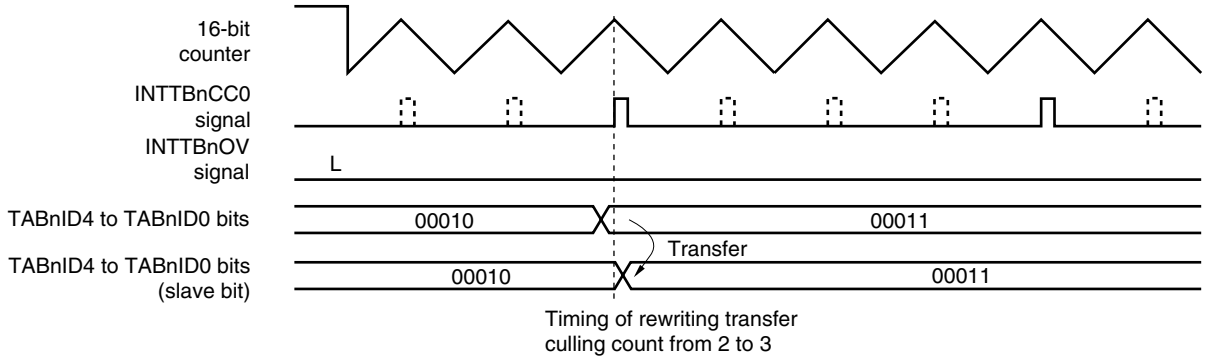
Remark k = 2, 3

(3) To output only crest interrupt (INTTBnCC0)

Set the TABnOPT1.TABnICE bit to 1 and set the TABnOPT1.TABnIOE bit to 0.

Figure 10-19. Crest Interrupt Output

(a) TABnOPT0.TABnCMS bit = 0, TABnOPT2.TABnRDE bit = 1 (with transfer culling control)

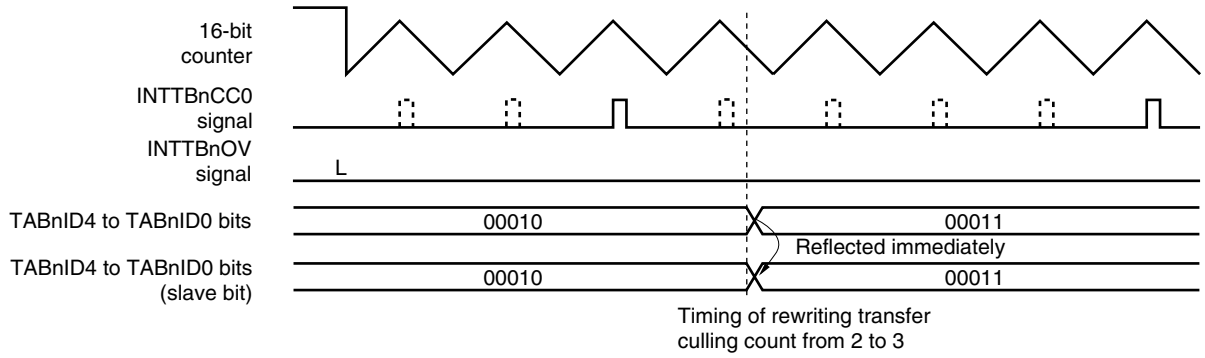


Remarks 1. Transfer is performed when the culled interrupt is output. The other transfer timing is ignored.

2. : Culled interrupt

3. n = 0, 1

(b) TABnOPT0.TABnCMS bit = 1, TABnOPT0.TABnRDE bit = 0 or 1 (without transfer control)



Remarks 1. Rewriting is reflected immediately. The transfer timing is ignored.

2. : Culled interrupt

3. n = 0, 1

14.2 Configuration

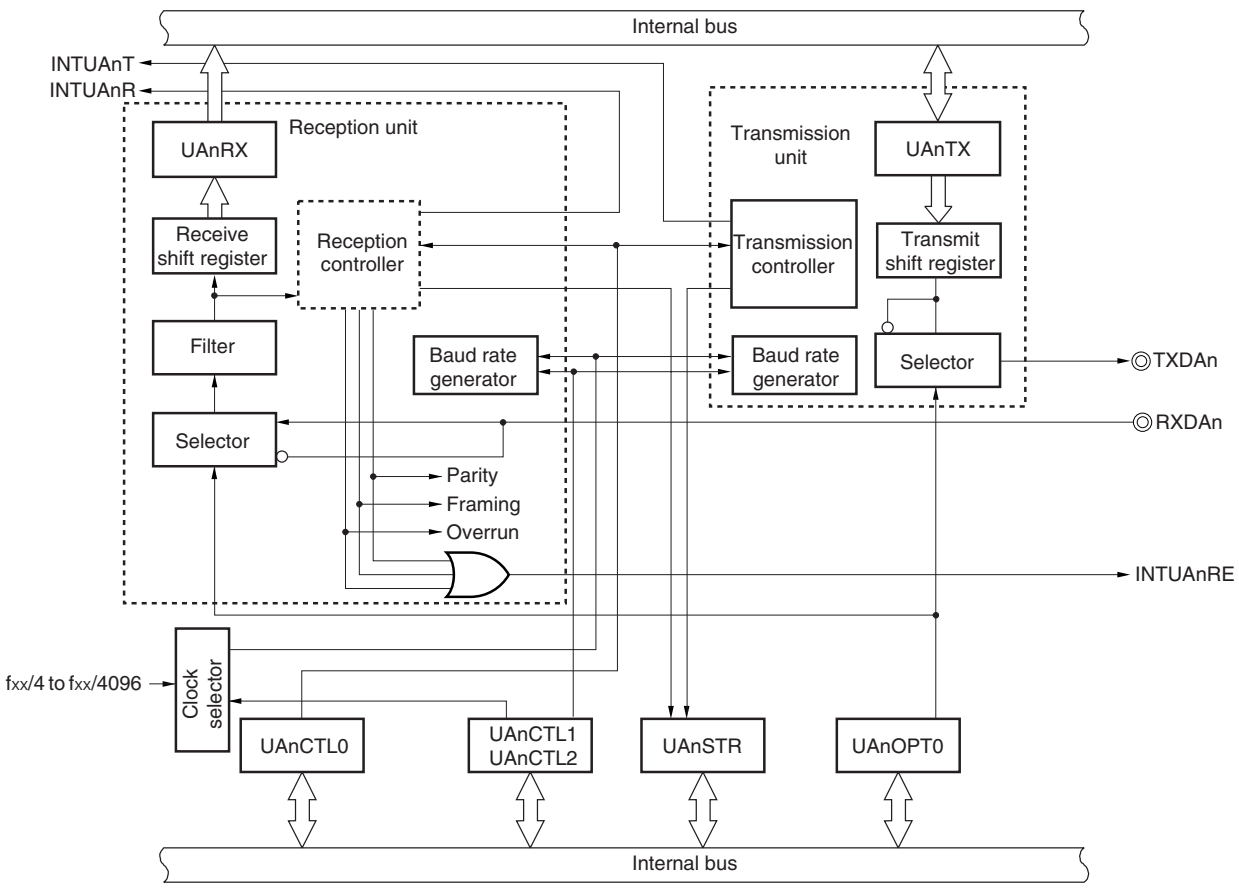
UARTAn consists of the following hardware units.

Table 14-1. Configuration of UARTAn

Item	Configuration
Registers	UARTAn control register 0 (UAnCTL0) UARTAn control register 1 (UAnCTL1) UARTAn control register 2 (UAnCTL2) UARTAn option control register 0 (UAnOPT0) UARTAn status register (UAnSTR) UARTAn receive shift register UARTAn receive data register (UAnRX) UARTAn transmit shift register UARTAn transmit data register (UAnTX)

The block diagram of the UARTAn is shown below.

Figure 14-1. Block Diagram of UARTAn



Remarks 1. n = 0 to 2

2. For the configuration of the baud rate generator, see **Figure 14-12**.

(2/2)

UBDIR	Specification of transfer direction mode (MSB/LSB)
0	MSB transfer first
1	LSB transfer first
• Clear the UBPWR bit or UBTXE and UBRXE bits to 0 before changing the setting of the UBDIR bit.	

UBPS1	UBPS0	Parity selection during transmission	Parity selection during reception
0	0	Do not output a parity bit	Receive with no parity
0	1	Output 0 parity	Receive as 0 parity
1	0	Output odd parity	Judge as odd parity
1	1	Output even parity	Judge as even parity
• Clear the UBTXE and UBRXE bits to 0 before overwriting the UBPS1 and UBPS0 bits. • If “0 parity” is selected for reception, no parity judgment is made. Therefore, no error interrupt is generated because the UBSTR.UBPE bit is not set to 1.			

UBCL	Specification of data character length of 1-frame transmit/receive data
0	7 bits
1	8 bits
Clear the UBTXE and UBRXE bits to 0 before overwriting the UBCL bit.	

UBSL	Specification of stop bit length of transmit data
0	1 bit
1	2 bits
• Clear the UBTXE bit to 0 before overwriting the UBSL bit. • Since reception always operates by using a single stop bit length, the UBSL bit setting does not affect receive operations.	

Remark For details of parity, see **15.7.6 Parity types and corresponding operation**.

(9) UARTB FIFO status register 0 (UBFIS0)

The UBFIS0 register is valid in the FIFO mode (UBFIC0.UBMOD bit = 1). It is used to read the number of bytes of the data stored in receive FIFO.

This register is read-only in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R Address: FFFFFA4EH

	7	6	5	4	3	2	1	0
UBFIS0	0	0	0	UBRB4	UBRB3	UBRB2	UBRB1	UBRB0

UBRB4	UBRB3	UBRB2	UBRB1	UBRB0	Receive FIFO pointer
0	0	0	0	0	0 bytes
0	0	0	0	1	1 byte
0	0	0	1	0	2 bytes
0	0	0	1	1	3 bytes
0	0	1	0	0	4 bytes
0	0	1	0	1	5 bytes
0	0	1	1	0	6 bytes
0	0	1	1	1	7 bytes
0	1	0	0	0	8 bytes
0	1	0	0	1	9 bytes
0	1	0	1	0	10 bytes
0	1	0	1	1	11 bytes
0	1	1	0	0	12 bytes
0	1	1	0	1	13 bytes
0	1	1	1	0	14 bytes
0	1	1	1	1	15 bytes
1	0	0	0	0	16 bytes
Other than above					Invalid

Indicates the number of bytes (readable bytes) of the data stored in receive FIFO as a receive FIFO pointer.

16.3.3 Mode switching between CSIF2 and UARTB

In the V850E/IG4 and V850E/IH4, CSIF2 and UARTB share a pin, and these functions cannot be used at the same time. To use the pin for the CSIF2 function, set up the PMC3 and PFC3 registers in advance.

Switching the operation mode between CSIF2 and UARTB, the serial interfaces, is described below.

Caution The operations related to transmission and reception of CSIF2 or UARTB are not guaranteed if the operation mode is switched during transmission or reception. Be sure to disable the unit that is not used.

Figure 16-4. Operation Mode Switch Settings of CSIF2 and UARTB

After reset: 00H R/W Address: FFFFF446H

	7	6	5	4	3	2	1	0
PMC3	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30

PMC37	PFC37	Operation mode
0	×	I/O port
1	0	$\overline{\text{SCKF2}}$

PMC3n	PFC3n	Operation mode
0	×	I/O port
1	0	CSIF2 mode
1	1	UARTB mode

Remarks 1. n = 5, 6

2. × = 0 or 1

16.5.12 Continuous transfer mode (slave mode, transmission/reception mode)

MSB first (CFnCTL0.CFnDIR bit = 0), communication type 1 (CFnCTL1.CFnCKP and CFnCTL1.CFnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKFn}$) (CFnCTL1.CFnCKS2 to CFnCTL1.CFnCKS0 bits = 111), transfer data length = 8 bits (CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits = 0000)

(3/3)

ACKD0	Detection of $\overline{ACK}$
0	$\overline{ACK}$ was not detected.
1	$\overline{ACK}$ was detected.

Condition for clearing (ACKD0 bit = 0)	Condition for setting (ACKD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• After the SDA pin is set to low level at the rising edge of the SCL pin's ninth clock

STD0	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect

Condition for clearing (STD0 bit = 0)	Condition for setting (STD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD0 bit = 0)	Condition for setting (SPD0 bit = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2					▲3		Δ4

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 00000110B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3				▲4		Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010XX00B

▲4: IICS0 register = 00000110B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

24.3.4 Cautions

(1) Handling of device that was used for debugging

Do not mount a device that was used for debugging on a mass-produced product, because the flash memory was rewritten during debugging and the number of rewrites of the flash memory cannot be guaranteed. Moreover, do not embed the debug monitor program into mass-produced products.

(2) When breaks cannot be executed

Forced breaks cannot be executed if one of the following conditions is satisfied.

- Interrupts are disabled (DI)
- Interrupts issued for the serial interface, which is used for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4, are masked
- Standby mode is entered while standby release by a maskable interrupt is prohibited
- Mode for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4 is UARTA0, and the peripheral clock has been stopped

(3) When pseudo real-time RAM monitor (RRM) function and DMM function do not operate

The pseudo RRM function and DMM function do not operate if one of the following conditions is satisfied.

- Interrupts are disabled (DI)
- Interrupts issued for the serial interface, which is used for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4, are masked
- Standby mode is entered while standby release by a maskable interrupt is prohibited
- Mode for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4 is UARTA0, and the peripheral clock has been stopped
- Mode for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4 is UARTA0, and a clock different from the one specified in the debugger is used for communication

(4) Standby release with pseudo RRM and DMM functions enabled

The standby mode is released by the pseudo RRM function and DMM function if one of the following conditions is satisfied.

- Mode for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4 is CSIF0
- Mode for communication between MINICUBE2 and the V850E/IG4 or V850E/IH4 is UARTA0, and the peripheral clock has not stopped.

(5) Writing to peripheral I/O registers that requires a specific sequence, using DMM function

Peripheral I/O registers that requires a specific sequence cannot be written with the DMM function.

(6) Flash self programming

If a space where the debug monitor program is allocated is rewritten by flash self programming, the debugger can no longer operate normally.

26.2 V850E/IH4

26.2.1 Absolute maximum ratings

(T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.5 to +2.0	V
	V_{SS}	V_{SSa} = EV_{SSb} = AV_{SSk}		−0.5 to +0.5	V
	EV_{DD}			−0.5 to +6.5	V
	EV_{SS}	V_{SSa} = EV_{SSb} = AV_{SSk}		−0.5 to +0.5	V
	FV_{DD}			−0.5 to +6.5	V
	AV_{DD}			−0.5 to +6.5	V
	AV_{SS}	V_{SSa} = EV_{SSb} = AV_{SSk}		−0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1**		−0.5 to EV_{DD} + 0.5[Note 2]	V
	V_{I2}	X1, X2		−0.5 to V_{DD} + 0.35	V
Output current, low	I_{OL}	All pins	Per pin	4	mA
			Total of all pins	63	mA
Output current, high	I_{OH}	All pins	Per pin	−4	mA
			Total of all pins	−63	mA
Analog input voltage	V_{IAN}	**Note 3**		−0.5 to AV_{DD} + 0.5[Note 2]	V
Analog reference input voltage	V_{IREF}	AV_{REFP0}, AV_{REFP1}		−0.5 to AV_{DD} + 0.5[Note 2]	V
Operating ambient temperature	T_A	In normal operating mode		−40 to +85	°C
		In flash memory programming mode		−40 to +85	°C
Storage temperature	T_{stg}			−40 to +125	°C

Notes 1. P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P44, P50 to P56, P70 to P711, P90 to P97, PDL0 to PDL15, $\overline{\text{RESET}}$, FLMD0, $\overline{\text{DRST}}$

2. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

3. P70/ANI20 to P711/ANI211, ANI00/ANI05 to ANI02/ANI07, ANI03, ANI10/ANI15 to ANI12/ANI17, ANI13

Cautions 1. Do not directly connect the output pins (or I/O pins in the output state) of IC products to other output pins (including I/O pins in the output state), power supply pins such as V_{DD} and EV_{DD}, or GND pin. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark a = 0 to 2
b = 0 to 4
k = 0 to 2

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Symbol	Name	Unit	Page
AD2CR6H	A/D2 conversion result register 6H	ADC2	710
AD2CR7	A/D2 conversion result register 7	ADC2	710
AD2CR7H	A/D2 conversion result register 7H	ADC2	710
AD2CR8	A/D2 conversion result register 8	ADC2	710
AD2CR8H	A/D2 conversion result register 8H	ADC2	710
AD2CR9	A/D2 conversion result register 9	ADC2	710
AD2CR9H	A/D2 conversion result register 9H	ADC2	710
AD2CR10	A/D2 conversion result register 10	ADC2	710
AD2CR10H	A/D2 conversion result register 10H	ADC2	710
AD2CR11	A/D2 conversion result register 11	ADC2	710
AD2CR11H	A/D2 conversion result register 11H	ADC2	710
AD2IC	Interrupt control register	INTC	999
AD2M0	A/D converter 2 mode register 0	ADC2	707
AD2M1	A/D converter 2 mode register 1	ADC2	708
AD2S	A/D converter 2 channel specification register	ADC2	709
ADLTS1	A/DLDTRG1 input select register	ADC0, ADC1	659
ADLTS2	A/DLDTRG2 input select register	ADC0, ADC1	659
ADT0IC	Interrupt control register	INTC	999
ADT1IC	Interrupt control register	INTC	999
ADTF	A/D trigger falling edge specification register	ADC0, ADC1	661, 1014
ADTR	A/D trigger rising edge specification register	ADC0, ADC1	661, 1014
CF0CTL0	CSIF0 control register 0	CSIF	829
CF0CTL1	CSIF0 control register 1	CSIF	832
CF0CTL2	CSIF0 control register 2	CSIF	833
CF0REIC	Interrupt control register	INTC	999
CF0RIC	Interrupt control register	INTC	999
CF0RX	CSIF0 receive data register	CSIF	827
CF0RXL	CSIF0 receive data register L	CSIF	827
CF0STR	CSIF0 status register	CSIF	835
CF0TIC	Interrupt control register	INTC	999
CF0TX	CSIF0 transmit data register	CSIF	828
CF0TXL	CSIF0 transmit data register L	CSIF	828
CF1CTL0	CSIF1 control register 0	CSIF	829
CF1CTL1	CSIF1 control register 1	CSIF	832
CF1CTL2	CSIF1 control register 2	CSIF	833
CF1REIC	Interrupt control register	INTC	999
CF1RIC	Interrupt control register	INTC	999
CF1RX	CSIF1 receive data register	CSIF	827
CF1RXL	CSIF1 receive data register L	CSIF	827
CF1STR	CSIF1 status register	CSIF	835
CF1TIC	Interrupt control register	INTC	999
CF1TX	CSIF1 transmit data register	CSIF	828
CF1TXL	CSIF1 transmit data register L	CSIF	828
CF2CTL0	CSIF2 control register 0	CSIF	829