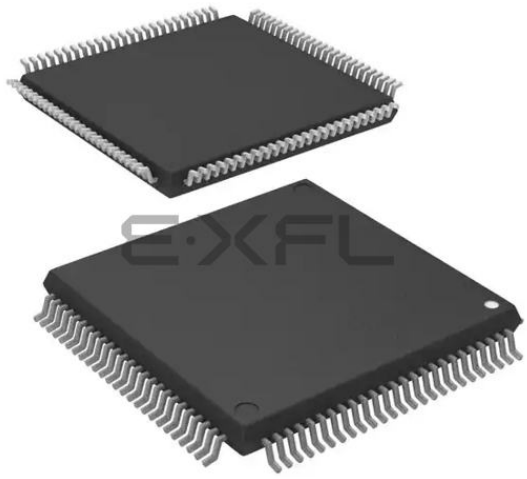
Renesas Electronics America Inc - UPD70F3918GF(R)-GAT-AX Datasheet



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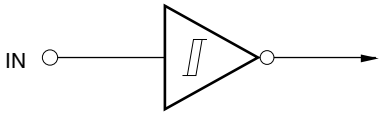
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850E1
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	480KB (480K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3918gf-r-gat-ax

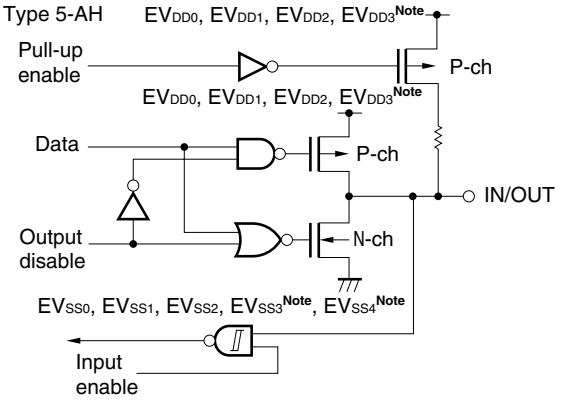
2.3 Pin I/O Circuits

Type 2

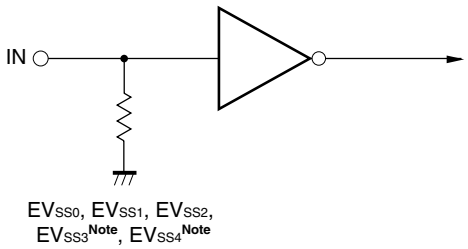


Schmitt-triggered input with hysteresis characteristics

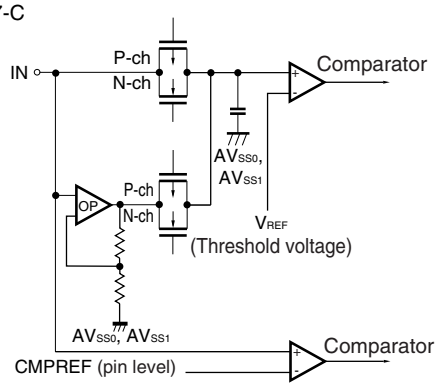
Type 5-AH



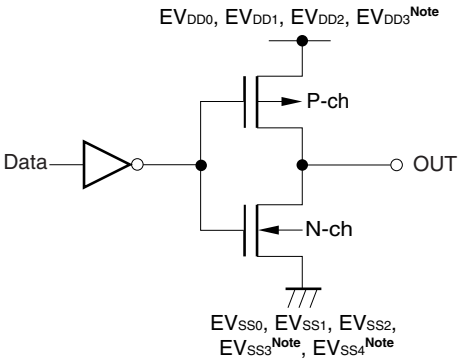
Type 2-M



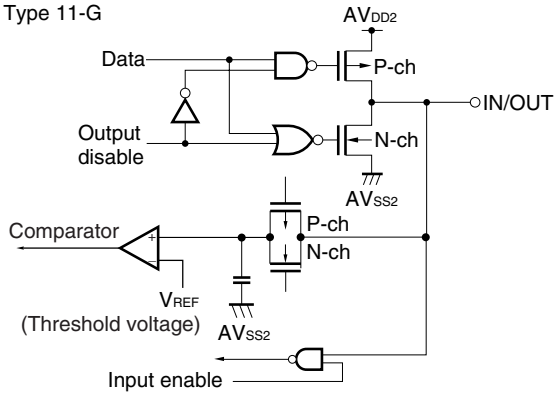
Type 7-C



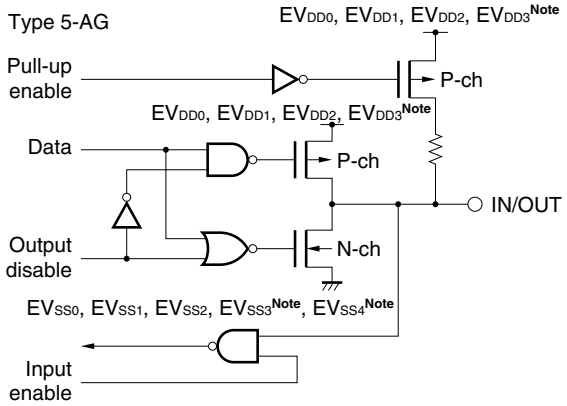
Type 3-C



Type 11-G



Type 5-AG



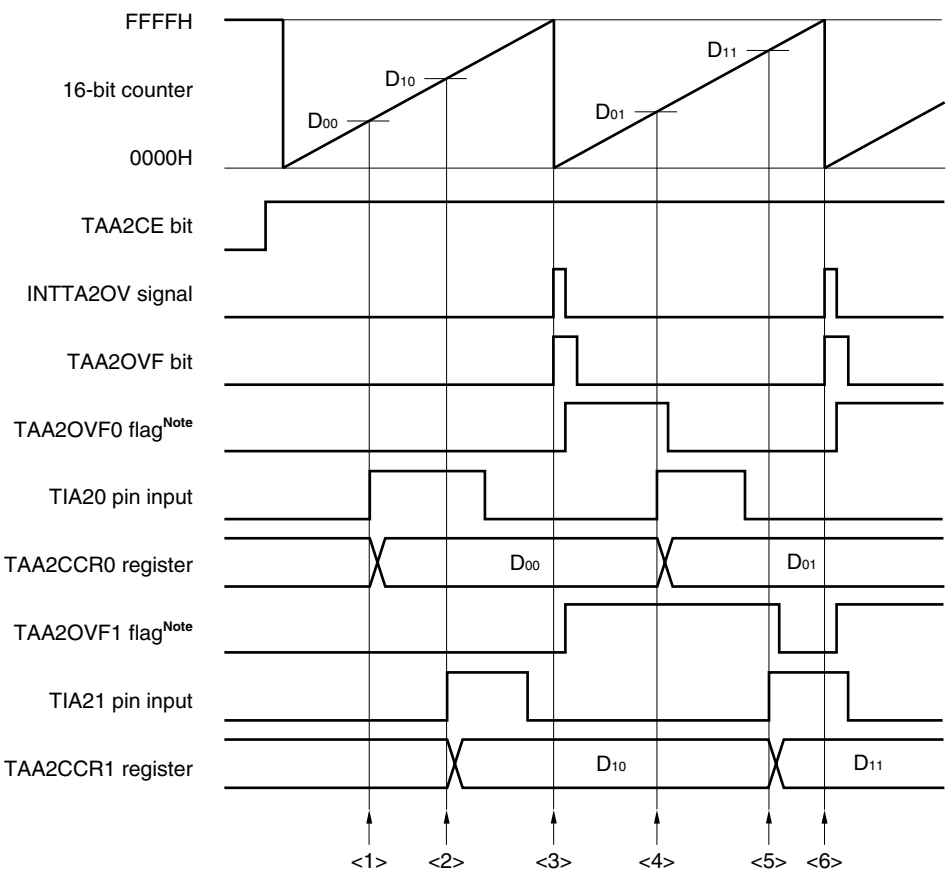
Note V850E/IH4 only

(2/18)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1	8	16	32	
FFFFF0A0H	DMA trigger factor register 2	DTFR2	R/W			√		0000H
FFFFF0A0H	DMA trigger factor register 2L	DTFR2L			√			00H
FFFFF0A1H	DMA trigger factor register 2H	DTFR2H			√			00H
FFFFF0A2H	DMA addressing control register 2	DADC2				√		0000H
FFFFF0A4H	DMA transfer count specification register 2	DTCR2				√		Undefined
FFFFF0A6H	DMA transfer destination address specification register 2	DDAR2					√	Undefined
FFFFF0A6H	DMA transfer destination address specification register 2L	DDAR2L				√		Undefined
FFFFF0A8H	DMA transfer destination address specification register 2H	DDAR2H				√		Undefined
FFFFF0AAH	DMA transfer source address specification register 2	DSAR2					√	Undefined
FFFFF0AAH	DMA transfer source address specification register 2L	DSAR2L				√		Undefined
FFFFF0ACH	DMA transfer source address specification register 2H	DSAR2H				√		Undefined
FFFFF0AEH	DMA channel control register 2	DCHC2				√		0000H
FFFFF0B0H	DMA trigger factor register 3	DTFR3				√		0000H
FFFFF0B0H	DMA trigger factor register 3L	DTFR3L			√			00H
FFFFF0B1H	DMA trigger factor register 3H	DTFR3H			√			00H
FFFFF0B2H	DMA addressing control register 3	DADC3				√		0000H
FFFFF0B4H	DMA transfer count specification register 3	DTCR3				√		Undefined
FFFFF0B6H	DMA transfer destination address specification register 3	DDAR3					√	Undefined
FFFFF0B6H	DMA transfer destination address specification register 3L	DDAR3L				√		Undefined
FFFFF0B8H	DMA transfer destination address specification register 3H	DDAR3H				√		Undefined
FFFFF0BAH	DMA transfer source address specification register 3	DSAR3					√	Undefined
FFFFF0BAH	DMA transfer source address specification register 3L	DSAR3L				√		Undefined
FFFFF0BCH	DMA transfer source address specification register 3H	DSAR3H				√		Undefined
FFFFF0BEH	DMA channel control register 3	DCHC3				√		0000H
FFFFF0C0H	DMA trigger factor register 4	DTFR4				√		0000H
FFFFF0C0H	DMA trigger factor register 4L	DTFR4L			√			00H
FFFFF0C1H	DMA trigger factor register 4H	DTFR4H			√			00H
FFFFF0C2H	DMA addressing control register 4	DADC4				√		0000H
FFFFF0C4H	DMA transfer count specification register 4	DTCR4				√		Undefined
FFFFF0C6H	DMA transfer destination address specification register 4	DDAR4					√	Undefined
FFFFF0C6H	DMA transfer destination address specification register 4L	DDAR4L				√		Undefined
FFFFF0C8H	DMA transfer destination address specification register 4H	DDAR4H				√		Undefined

(1/2)

Example when two capture registers are used (using overflow interrupt)



Note The TAA2OVF0 and TAA2OVF1 flags are set on the internal RAM by software.

<1> Read the TAA2CCR0 register (setting of the default value of the TIA20 pin input).

<2> Read the TAA2CCR1 register (setting of the default value of the TIA21 pin input).

<3> An overflow occurs. Set the TAA2OVF0 and TAA2OVF1 flags to 1 in the overflow interrupt servicing, and clear the overflow flag to 0.

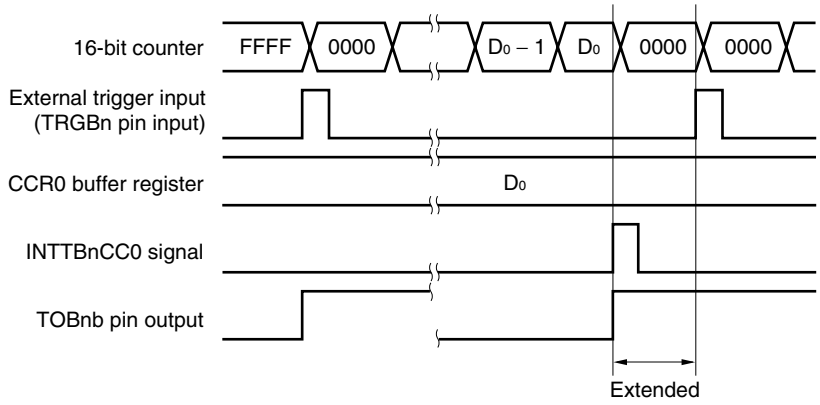
<4> Read the TAA2CCR0 register.
Read the TAA2OVF0 flag. If the TAA2OVF0 flag is 1, clear it to 0.
Because the TAA2OVF0 flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).

<5> Read the TAA2CCR1 register.
Read the TAA2OVF1 flag. If the TAA2OVF1 flag is 1, clear it to 0 (the TAA2OVF0 flag is cleared in <4>, and the TAA2OVF1 flag remains 1).
Because the TAA2OVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} − D_{10}) (correct).

<6> Same as <3>

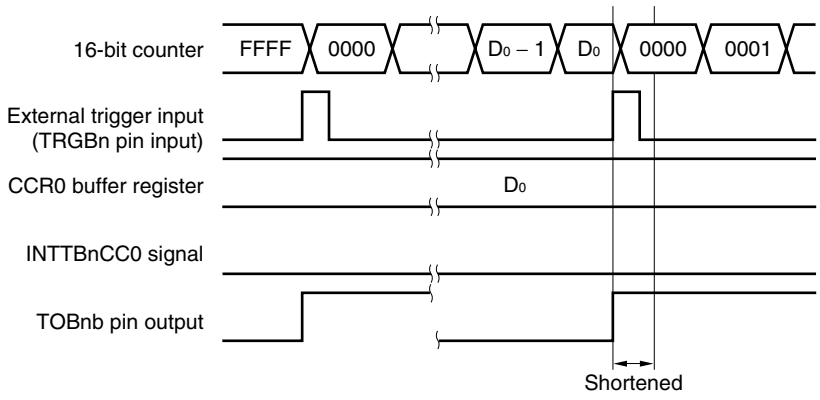
(d) Conflict between trigger detection and match with CCR0 buffer register

If the trigger is detected immediately after the INTTBnCC0 signal is generated, the 16-bit counter is cleared to 0000H and continues counting up. Therefore, the active period of the TOBnb pin is extended by time from generation of the INTTBnCC0 signal to trigger detection.



Remark n = 0, 1
b = 1 to 3

If the trigger is detected immediately before the INTTBnCC0 signal is generated, the INTTBnCC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOBnb pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.



Remark n = 0, 1
b = 1 to 3

Figure 7-26. Register Setting in One-Shot Pulse Output Mode (2/3)

(c) TABn I/O control register 0 (TABnIOC0)

	TABnOL3	TABnOE3	TABnOL2	TABnOE2	TABnOL1	TABnOE1	TABnOL0	TABnOE0
TABnIOC0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

0: Disable TOBn0 pin output
1: Enable TOBn0 pin output

Setting of TOBn0 pin output level while waiting for external trigger
0: Low level
1: High level

0: Disable TOBn1 pin output
1: Enable TOBn1 pin output

Setting of TOBn1 pin output level while waiting for external trigger
0: Low level
1: High level

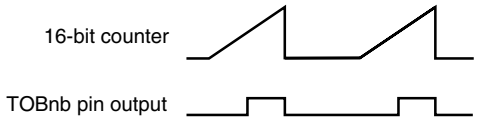
0: Disable TOBn2 pin output
1: Enable TOBn2 pin output

Setting of TOBn2 pin output level while waiting for external trigger
0: Low level
1: High level

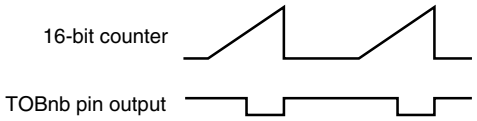
0: Disable TOBn3 pin output
1: Enable TOBn3 pin output

Setting of TOBn3 pin output level while waiting for external trigger
0: Low level
1: High level

• When TABnOLb bit = 0



• When TABnOLb bit = 1



(d) TABn I/O control register 2 (TABnIOC2)

	TABnEES1	TABnEES0	TABnETS1	TABnETS0				
TABnIOC2	0	0	0	0	0/1	0/1	0/1	0/1

Select valid edge of external trigger input (TRGBn pin)

Select valid edge of external event count input (EVTBn pin)

(e) TABn counter read buffer register (TABnCNT)

The value of the 16-bit counter can be read by reading the TABnCNT register.

(11) TMTn capture/compare register 0 (TTnCCR0)

The TTnCCR0 register is a 16-bit register that can be used as a capture register or compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TTnOPT0.TTnCCS0 bit. In the pulse width measurement mode, the TTnCCR0 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TTnCCR0 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Remark n = 0 to 3

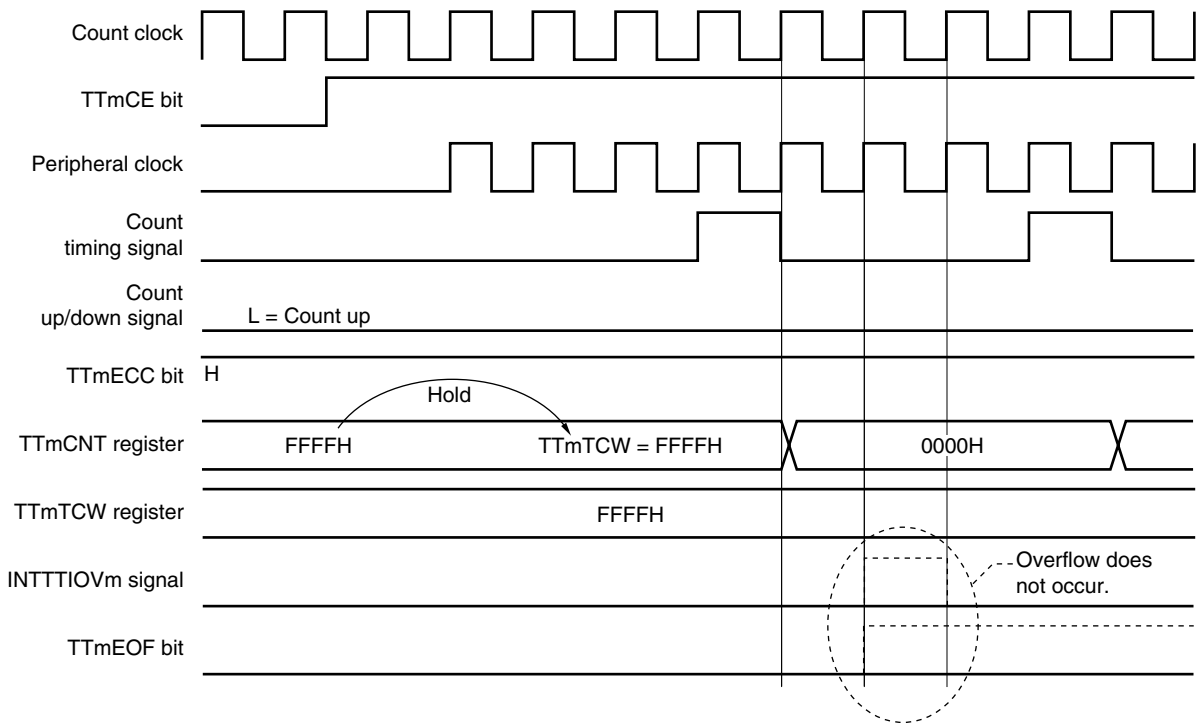
After reset: 0000H R/W Address: TT0CCR0 FFFFF58AH, TT1CCR0 FFFFF5CAH, TT2CCR0 FFFFF78AH, TT3CCR0 FFFFF7CAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTnCCR0 (n = 0 to 3)																

(b) If overflow does not occur immediately after start of operation

If the count operation is resumed when the TTmCTL2.TTmECC bit = 1, the 16-bit counter does not overflow if its count value that has been held is FFFFH and if the next count operation is counting up.

After the counter starts operating and counts up from a count value (value of TTmTCW register = FFFFH), the counter overflows from FFFFH to 0000H. However, detection of the overflow is masked, the overflow flag (TTmEOF) is not set, and the overflow interrupt request signal (INTTTIOVm) is not generated.



Remark m = 0, 1

(2/3)

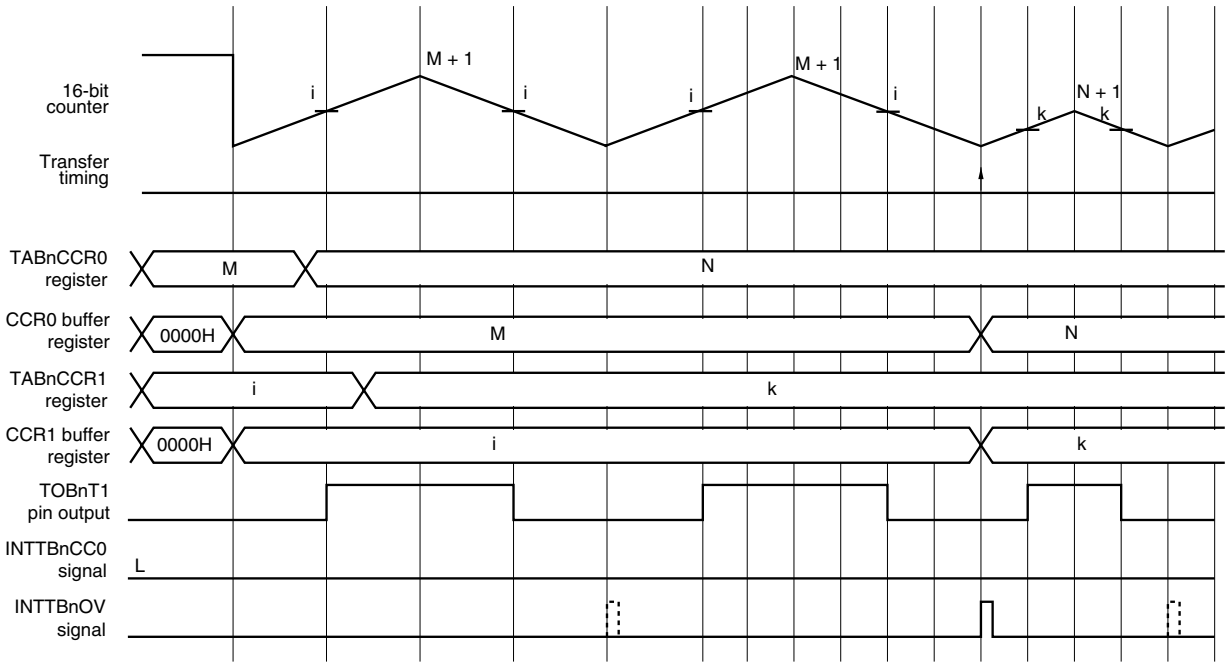
HZAyDCNn	HZAyDCPn	External pin[Note 1] input edge specification
0	0	No valid edge (setting the HZAyDCFn bit by external pin[Note 1] input is prohibited).
0	1	Rising edge of the external pin[Note 1] input is valid (abnormality is detected by rising edge input)[Note 2].
1	0	Falling edge of the external pin[Note 1] input is valid (abnormality is detected by falling edge input)[Note 2].
1	1	Setting prohibited

- Rewrite the HZAyDCNn and HZAyDCPn bits when the HZAyDCEn bit is 0.
- For the edge specification of the INTP03, INTP05, INTP07, INTP08, and INTP10 pins, see **19.4.2 (1) External interrupt rising edge specification register 0 (INTR0, INTF0)**.
- The edge of the external pins must be specified starting from the TOB0OFF, TOB1OFF, TOB01OFF, TOT2OFF, and TOT3OFF pins. Then the edge of the external pins other than the TOB0OFF, TOB1OFF, TOB01OFF, TOT2OFF, and TOT3OFF pins must be specified.
  Otherwise, the undefined edge may be detected when edges of the TOB0OFF, TOB1OFF, TOB01OFF, TOT2OFF, and TOT3OFF pins are specified.
- High-impedance output control is performed when the valid edge is input after the operation is enabled (by setting HZAyDCEn bit to 1). If the external pin[Note 1] is at the active level when the operation is enabled, therefore, high-impedance output control is not performed.

Notes 1. HZA0CTL0, HZA5CTL0, HZA9CTL0: TOB0OFF pin
HZA1CTL0, HZA5CTL1, HZA9CTL1: TOB1OFF pin
HZA4CTL0, HZA4CTL1, HZA8CTL0,
HZA8CTL1, HZA12CTL0, HZA12CTL1: TOB01OFF pin
HZA0CTL1: TOT2OFF pin
HZA1CTL1: TOT3OFF pin
HZA2CTL0, HZA6CTL0, HZA10CTL0: ANI00/ANI05 to ANI02/ANI07 pins
HZA2CTL1, HZA6CTL1, HZA10CTL1: ANI00/ANI05 to ANI02/ANI07 pins
HZA3CTL0, HZA7CTL0, HZA11CTL0: ANI10/ANI15 to ANI12/ANI17 pins
HZA3CTL1, HZA7CTL1, HZA11CTL1: ANI10/ANI15 to ANI12/ANI17 pins

2. To detect the voltage of a comparator exceeding the reference voltage, set the rising edge input. To detect the voltage of a comparator that has not reached the reference voltage, set the falling edge input.

Figure 10-33. Rewriting TABnCCR0 Register (When Valley Interrupt Is Set)



The transfer timing is generated when the valley interrupt occurs, the cycle of up counting and down counting becomes identical, and a symmetrical triangular wave is output.

Remarks 1. This is an example of the operation when the TABnOPT1.TABnICE bit = 0, TABnOPT1.TABnIOE bit = 1, TABnOPT1.TABnID4 to TABnOPT1.TABnID0 bits = 00001.

2. : Culled interrupt

3. n = 0, 1

15.7.5 Reception error

In the single mode (UBFIC0.UBMOD bit = 0), the three types of errors that can occur during a receive operation are a parity error, framing error, and overrun error. In the FIFO mode (UBFIC0.UBMOD bit = 1), the three types of errors that can occur during a receive operation are a parity error, framing error, and overflow error.

As a result of data reception, the UBSTR.UBPE, UBSTR.UBFE, or UBSTR.UBOVE bit is set to 1 if a parity error, framing error, or overrun error occurs in the single mode. The UBSTR.UBOVF bit is set to 1 if an overflow error occurs in the FIFO mode. The UBRXAP.UBPEF or UBRXAP.UBFEF bit is set to 1 if a parity error or framing error occurs in the FIFO mode. At the same time, a reception error interrupt request signal (INTUBTIRE) occurs. The contents of the error can be detected by reading the contents of the UBSTR or UBRXAP register.

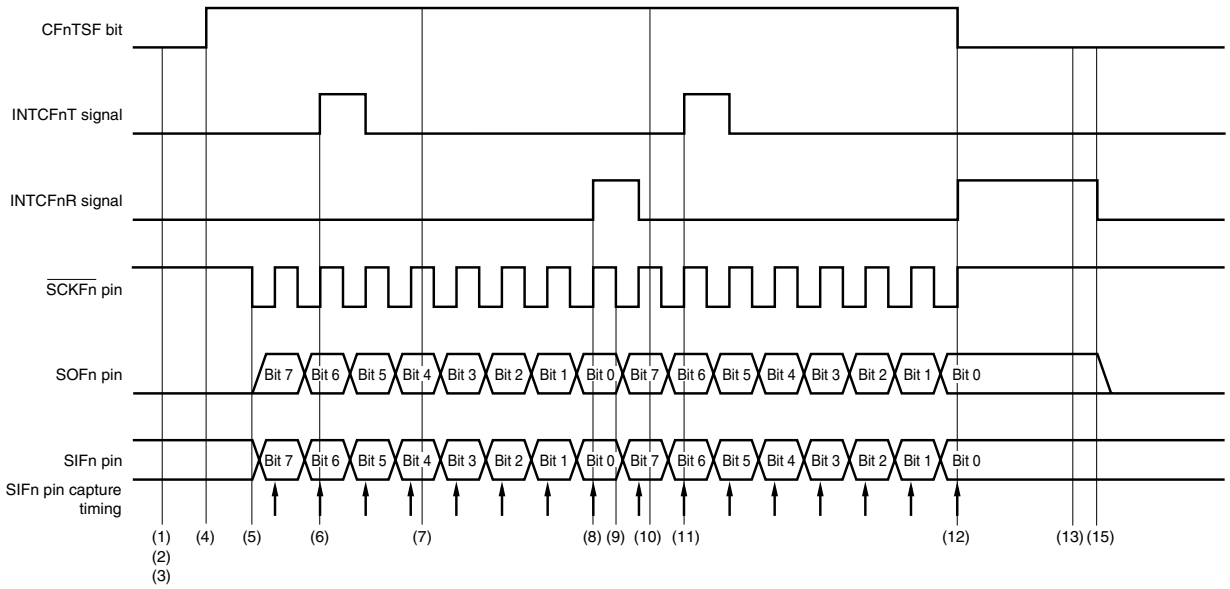
The contents of the UBSTR register are reset when 0 is written to the UBOVF, UBPE, UBFE, or UBOVE bit, or the UBCTL0.UBPWR or UBCTL0.UBRXE bit. The contents of the UBRXAP register are reset when 0 is written to the UBCTL0.UBPWR bit.

Table 15-5. Reception Error Causes

Error Flag	Valid Operation Mode	Error Flag	Reception Error	Cause
UBPE	Single mode	UBPE	Parity error	The parity specification during transmission does not match the parity of the receive data
UBFE		UBFE	Framing error	No stop bit detected
UBOVE		UBOVE	Overrun error	The reception of the next data is ended before data is read from the UBRX register
UBOVF	FIFO mode	UBOVF	Overflow error	The reception of the next data is ended while receive FIFO is full and before data is read.
UBPEF		UBPEF	Parity error	The parity specification during transmission does not match the parity of the data to be received.
UBFEF		UBFEF	Framing error	The stop bit is not detected when the target data is loaded.

(2) Operation timing

(1/2)



(1) Write 00H to the CFnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = f_{XX}/4, and master mode.

(2) Write 00H to the CFnCTL2 register, and set the transfer data length to 8 bits.

(3) Write E3H to the CFnCTL0 register, and select the transmission/reception mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) The CFnSTR.CFnTSF bit is set to 1 by writing the transmit data to the CFnTX register, and transmission/reception is started.

(5) When transmission/reception is started, output the serial clock to the $\overline{\text{SCKFn}}$ pin, output the transmit data to the SOFn pin in synchronization with the serial clock, and capture the receive data of the SIFn pin.

(6) When transfer of the transmit data from the CFnTX register to the shift register is ended and writing to the CFnTX register is enabled, the transmission enable interrupt request signal (INTCFnT) is generated.

(7) To continue transmission/reception, write the transmit data to the CFnTX register again after the INTCFnT signal is generated.

(8) When one transmission/reception is ended, the reception end interrupt request signal (INTCFnR) is generated, and reading of the CFnRX register is enabled.

(9) When a new transmit data is written to the CFnTX register before communication end, the next communication is started following communication end.

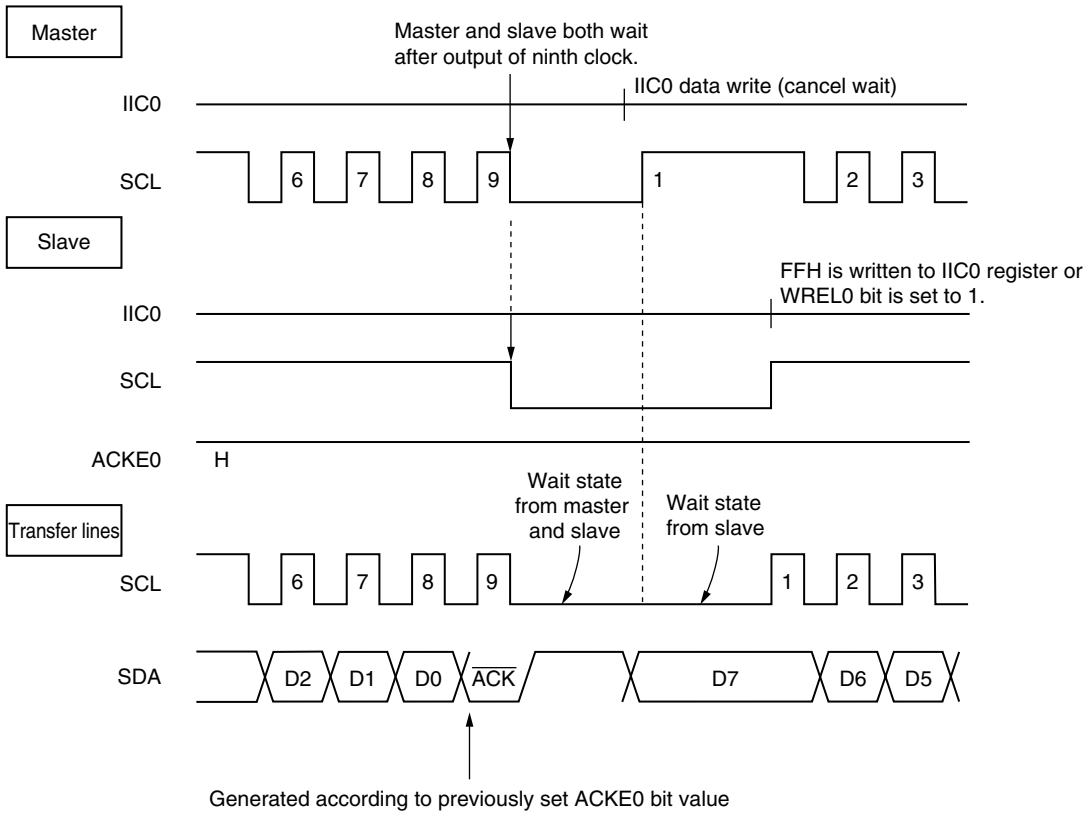
(10) Read the CFnRX register.

Remark n = 0 to 2

Figure 17-11. Wait State (2/2)

(b) When master and slave devices both have a nine-clock wait

(master: transmission, slave: reception, and ACKE0 = 1)



A wait state is automatically generated after a start condition is generated. Moreover, a wait state is automatically generated depending on the setting of the IICC0.WTIM0 bit.

Normally, when the IICC0.WREL0 bit is set to 1 or when FFH is written to the IIC0 register, the wait status is canceled and the transmitting side writes data to the IIC0 register to cancel the wait status.

The master device can also cancel the wait status via either of the following methods.

- By setting the IICC0.STT0 bit to 1
- By setting the IICC0.SPT0 bit to 1

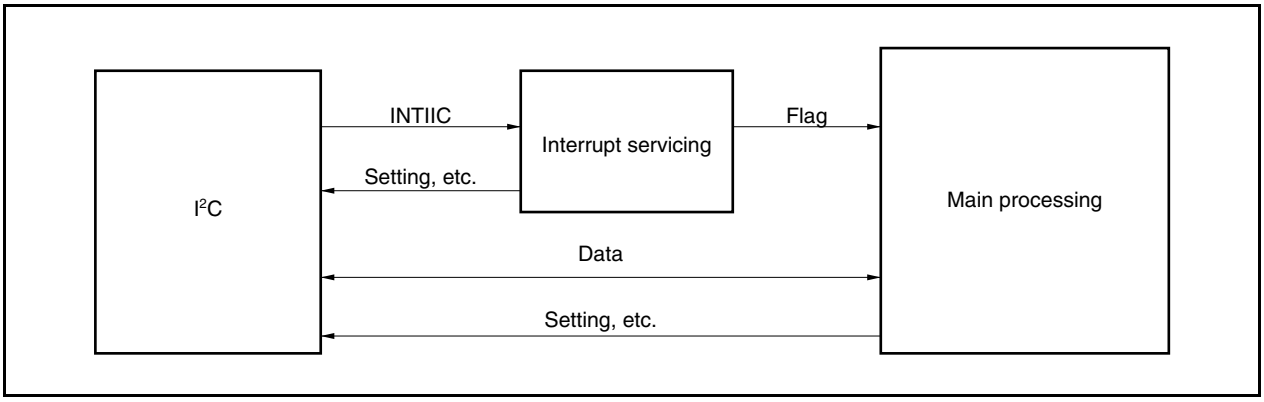
17.16.3 Slave operation

The following shows the processing procedure of the slave operation.

Basically, the operation of the slave device is event-driven. Therefore, processing by an INTIIC interrupt (processing requiring a significant change of the operation status, such as stop condition detection during communication) is necessary.

The following description assumes that data communication does not support extension codes. Also, it is assumed that the INTIIC interrupt servicing performs only status change processing and that the actual data communication is performed during the main processing.

Figure 17-18. Software Outline During Slave Operation



Therefore, the following three flags are prepared so that the data transfer processing can be performed by transmitting these flags to the main processing instead of the INTIIC signal.

(1) Communication mode flag

This flag indicates the following communication statuses.

Clear mode: Data communication not in progress

Communication mode: Data communication in progress (valid address detection stop condition detection, $\overline{\text{ACK}}$ from master not detected, address mismatch)

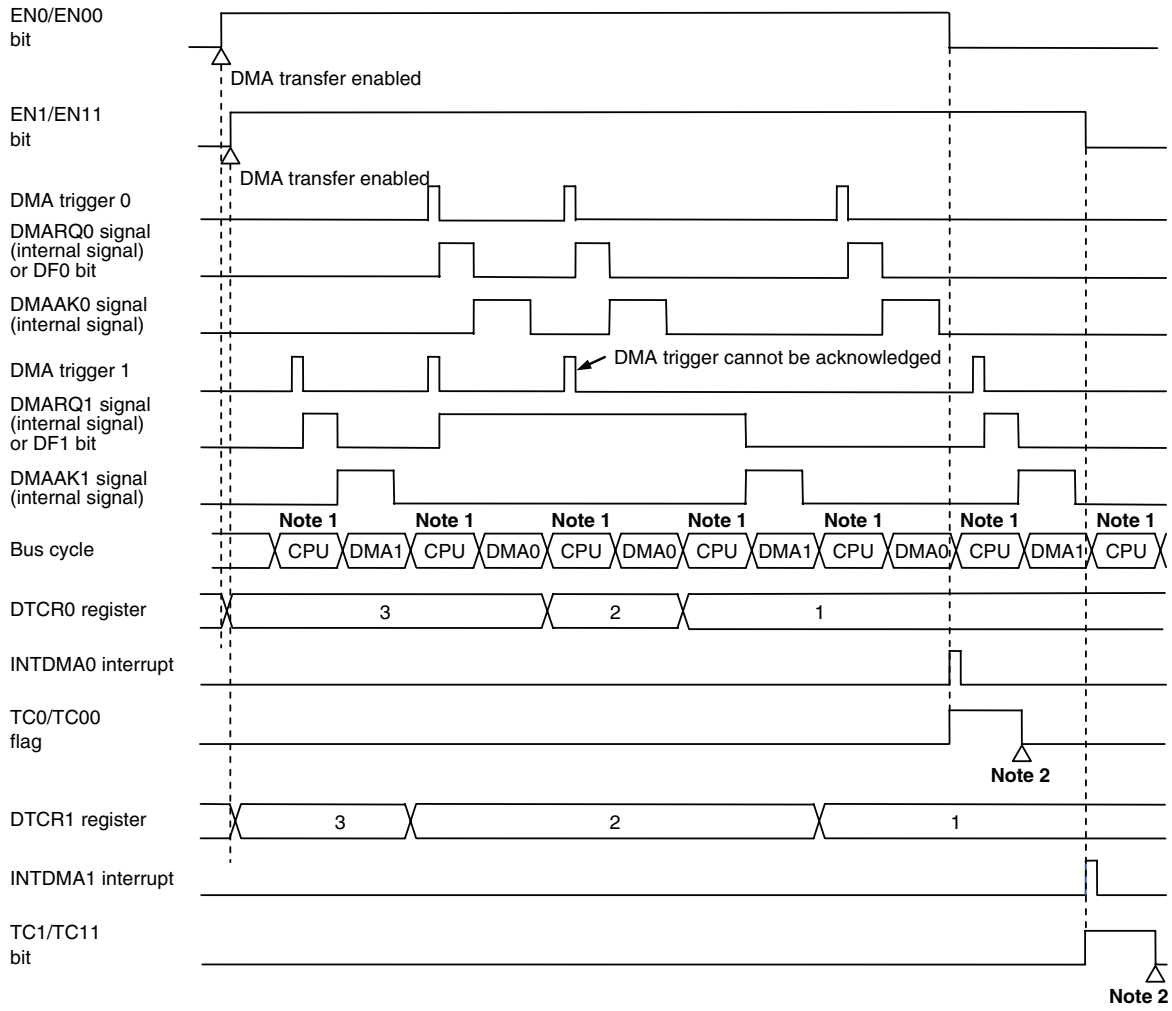
(2) Ready flag

This flag indicates that data communication is enabled. This is the same status as an INTIIC interrupt during normal data transfer. This flag is set in the interrupt processing block and cleared in the main processing block. The ready flag for the first data for transmission is not set in the interrupt processing block, so the first data is transmitted without clearance processing (the address match is regarded as a request for the next data).

(3) Communication direction flag

This flag indicates the direction of communication and is the same as the value of the IICS0.TRC0 bit.

Figure 18-3. Single Transfer Example 2



Notes 1. The bus is always released.

2. The DCHCn register is read or writing “0” to the DMAS.TCnn bit

Caution During the period from DMA trigger generation to the falling edge of the DMAAK0 and DMAAK1 signals (internal signals), DMA triggers for the same channel cannot be acknowledged.

Remark When the active level of the DMAAK0 and DMAAK1 signals (internal signals) is the high level.

(7) Registers that must not be set under certain conditions

The following registers must not be written to when a specific operation is performed. If these registers are written to, the operation cannot be guaranteed.

Status	Register That Must Not Be Set
Stop (ENn/ENnn bit = 0)	None
During operation (ENn/ENnn bit = 1)	DADCn[Note 1], DTFRn
During suspension[Note 2] (STPn/STPnn bit = 1)	DADCn[Note 1], DTFRn

Notes 1. The same value may be written to the register.

2. Setting the register is prohibited when the operation that was suspended is resumed. The register can be set when the operation is stopped (ENn/ENnn bit = 0) after the register is written.

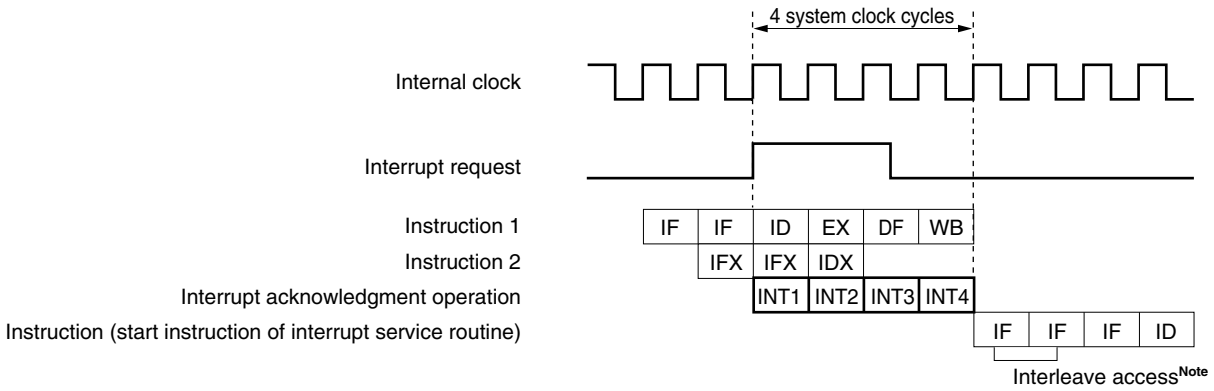
Remark n = 0 to 6

19.8 Interrupt Response Time of CPU

Except for the following cases, the interrupt response time of the CPU is at least 4 clock cycles. To input interrupt request signals successively, input the next interrupt request signal at least 4 clock cycles after the preceding interrupt.

- In IDLE/STOP mode
- When interrupt request non-sample instructions are successively executed (see **19.9 Periods in Which CPU Does Not Acknowledge Interrupts**.)
- When an on-chip peripheral I/O register is accessed

Figure 19-14. Pipeline Operation When Interrupt Request Signal Is Acknowledged (Outline)



Note For interleave accesses, refer to **8.1.2 2-clock branch** in **V850E1 Architecture User's Manual (U14559E)**.

Remark INT1 to INT4: Interrupt acknowledgment processing
IFX: Invalid instruction fetch
IDX: Invalid instruction decode

Interrupt response time (internal system clock cycles)				Conditions
	Internal interrupt	External interrupt		
		INTP00 to INTP19, INTADT0, INTADT1	INTP00 to INTP02, INTP17 to INTP19	
Minimum	4	4 + Analog filter time	4 + **Note 2** + Digital noise filter	The following cases are exceptions. • In IDLE/STOP mode • When two or more interrupt request non-sample instructions are executed in succession • When an on-chip peripheral I/O register is accessed
Maximum	7 Note 1	7 + Analog filter time	7 + **Note 2** + Digital noise filter	

Notes 1. When the LD instruction is executed on internal ROM (during align access)

2. For the number of internal system clocks, see **4.6 (1) Digital noise elimination 0 control register n (INTNFCn)**.

Remark a = 00 to 02, 17 to 19

24.2.2 Interface signals

The interface signals on the V850E/IG4 or V850E/IH4 side are described below.

(1) $\overline{\text{DRST}}$

This is a reset input signal for the on-chip debug unit. It is a negative-logic signal that asynchronously initializes the debug control unit (DCU).

MINICUBE changes the level of the $\overline{\text{DRST}}$ signal from low to high for output and starts the on-chip debug unit of the V850E/IG4 and V850E/IH4 when it detects VDD of the target system after the integrated debugger is started. If VDD is not detected from the target system, the output signals ($\overline{\text{DRST}}$, DCK, DMS, DDI, and FLMD0 pins) from the MINICUBE go into a high-impedance state.

When the $\overline{\text{DRST}}$ signal goes high, a reset signal is also generated in the V850E/IG4 and V850E/IH4.

When starting debugging by starting the integrated debugger, a reset signal is always generated.

(2) DCK

This is a clock input signal. It supplies a 20 MHz clock from MINICUBE. In the on-chip debug unit, the DMS and DDI signals are sampled at the rising edge of the DCK signal, and the data DDO is output at its falling edge.

(3) DMS

This is a transfer mode select signal. The transfer status in the debug unit changes depending on the level of the DMS signal.

(4) DDI

This is a data input signal. It is sampled in the on-chip debug unit at the rising edge of DCK.

(5) DDO

This is a data output signal. It is output from the on-chip debug unit at the falling edge of the DCK signal.

(6) FLMD0

The flash self programming function is used for the function to download data to the flash memory via the integrated debugger. During flash self programming, the FLMD0 pin must be kept high. In addition, connect a pull-down resistor to the FLMD0 pin.

The FLMD0 pin can be controlled in either of the following two ways.

<1> To control from MINICUBE

Connect the FLMD0 signal of MINICUBE to the FLMD0 pin of the V850E/IG4 and V850E/IH4.

In the normal mode, nothing is driven by MINICUBE (high impedance).

During a break, MINICUBE raises the FLMD0 pin to the high level when the download function of the integrated debugger is executed.

<2> To control from port

Connect any port of the device to the FLMD0 pin of the V850E/IG4 and V850E/IH4.

The same port as the one used by the user program to realize the flash self programming function may be used.

On the console of the integrated debugger, make a setting to raise the port pin to high level before executing the download function, or lower the port pin after executing the download function.

For details, refer to the **ID850QB Ver. 3.40 Integrated Debugger Operation User's Manual (U18604E)**.

25.9.6 Internal resources used

The following table lists the internal resources used for self programming. These internal resources can also be used freely for purposes other than self programming.

Table 25-13. Internal Resources Used

Resource Name	Description
Stack area	An extension of the stack used by the user is used by the library (can be used in both the internal RAM and external RAM).
Flash macro service area[Note]	A 9 KB internal RAM area (3FFCC00H to 3FFEFFFH)
Library code[Note]	Program entity of library (can be used anywhere other than the flash memory block to be manipulated).
Application program	Executed as user application. Calls flash functions.
Maskable interrupt	Can be used in the user application execution status or self-programming status. To use this interrupt in the self-programming status, since the processing transits to the address of the internal RAM start address + 4 addresses, allocate the jump instruction that transits the processing to the user interrupt servicing at the address of the internal RAM start address + 4 addresses in advance.
NMI interrupt	Can be used in the user application execution status or self-programming status. To use this interrupt in the self-programming status, since the processing transits to the address of the internal RAM start address, allocate the jump instruction that transits the processing to the user interrupt servicing at the internal RAM start address in advance.

Note About resources used, refer to the **Flash Memory Self-Programming Library User's Manual**.

26.1.9 Characteristics of A/D converter 2

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = V_{DD2} = 1.35 to 1.65 V,
EV_{DD0} = EV_{DD1} = EV_{DD2} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 4.0 to 5.5 V,
V_{SS0} = V_{SS1} = V_{SS2} = EV_{SS0} = EV_{SS1} = EV_{SS2} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]					±4.0	LSB
Conversion time	t_{CONV}		3.00		10.00	μs
Zero scale error[Note 1]					±4.0	LSB
Full-scale error[Note 1]					±4.0	LSB
Integral linearity error[Note 1]					±4.0	LSB
Differential linearity error[Note 1]					±2.0	LSB
Analog reference voltage	AV_{REF}		4.0		5.5	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
AV_{DD} supply current	AI_{DD}	During operation		3.5	7	mA
	AI_{DDS}	In STOP mode[Note 2]		1	10	μA

Notes 1. Excludes quantization error (±0.5 LSB).

2. Stop A/D converter 2 (AD2M0.AD2CE bit = 0) before setting STOP mode.

Remark LSB: Least Significant Bit