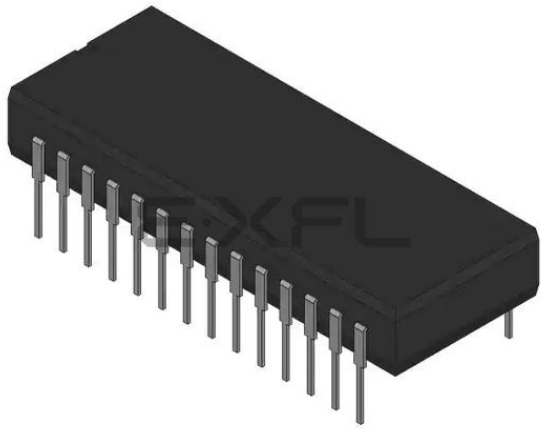

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Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08rd16dwe

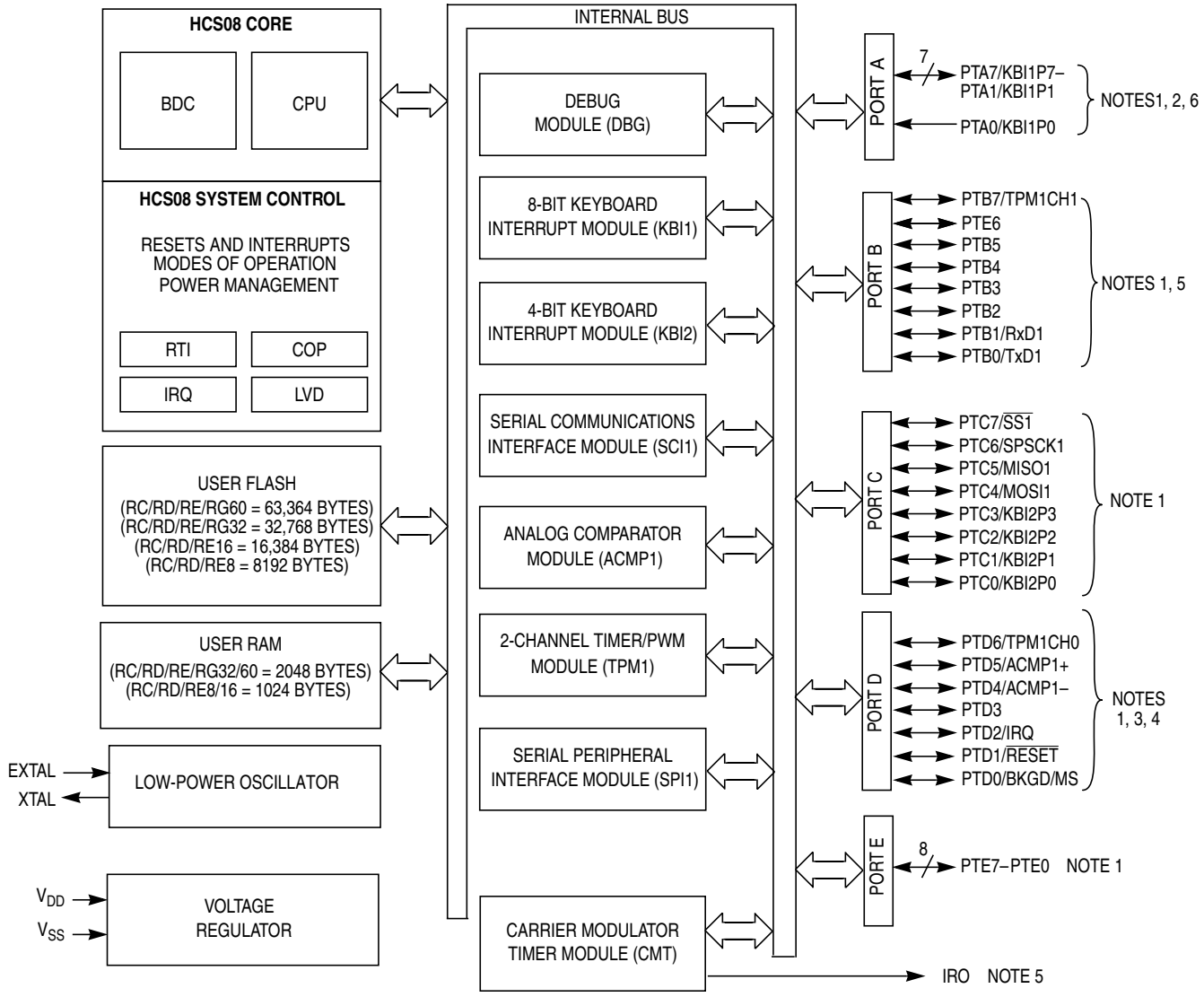
Chapter 11
Serial Communications Interface (S08SCIV1)

Chapter 12
Serial Communications Interface (S08SCIV1)

Chapter 13
Serial Peripheral Interface (S08SPIV3)

1.3 MCU Block Diagram

This block diagram shows the structure of the MC9S08RC/RD/RE/RG MCUs

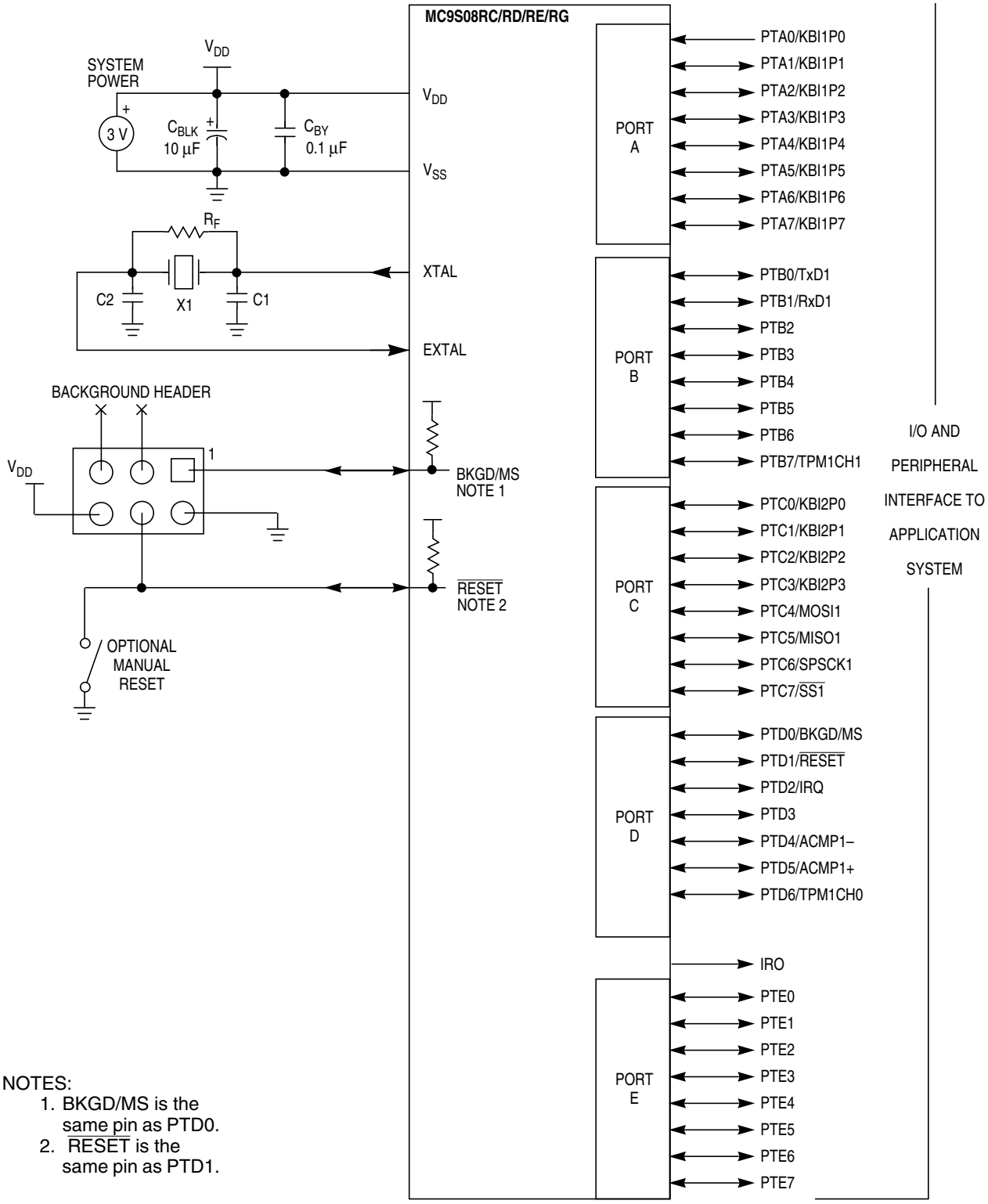


NOTES:

1. Port pins are software configurable with pullup device if input port
2. PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}. Also, PTA0 does not pullup to V_{DD} when internal pullup is enabled.
3. IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)
4. The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 1-1. MC9S08RC/RD/RE/RG Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.



NOTES:
1. BKGD/MS is the same pin as PTD0.
2. RESET is the same pin as PTD1.

Figure 2-5. Basic System Connections

Table 4-1. Direct-Page Register Summary (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$002A	IRQSC	0	0	IRQEDG	IRQPE	IRQF	IRQACK	IRQIE	IRQMOD
$002B	ACMP1SC[2]	ACME	ACBGS	ACF	ACIE	ACO	—	ACMOD1	ACMOD0
$002C–$002F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
$0030	TPM1SC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
$0031	TPM1CNTH	Bit 15	14	13	12	11	10	9	Bit 8
$0032	TPM1CNTL	Bit 7	6	5	4	3	2	1	Bit 0
$0033	TPM1MODH	Bit 15	14	13	12	11	10	9	Bit 8
$0034	TPM1MODL	Bit 7	6	5	4	3	2	1	Bit 0
$0035	TPM1C0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
$0036	TPM1C0VH	Bit 15	14	13	12	11	10	9	Bit 8
$0037	TPM1C0VL	Bit 7	6	5	4	3	2	1	Bit 0
$0038	TPM1C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
$0039	TPM1C1VH	Bit 15	14	13	12	11	10	9	Bit 8
$003A	TPM1C1VL	Bit 7	6	5	4	3	2	1	Bit 0
$003B–$003F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
$0040	**SPI1C1**[3]	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
$0041	SPI1C2[3]	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
$0042	**SPI1BR**[3]	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
$0043	**SPI1S**[3]	SPRF	0	SPTEF	MODF	0	0	0	0
$0044	Reserved	—	—	—	—	—	—	—	—
$0045	**SPI1D**[3]	Bit 7	6	5	4	3	2	1	Bit 0

1. The SCI module is not included on the MC9S08RC devices. This is a reserved location for those devices.
2. The analog comparator (ACMP) module is not included on the MC9S08RD devices. This is a reserved location for those devices.
3. The SPI module is not included on the MC9S08RC/RD/RE devices. These are reserved locations on the 32K and 60K versions of these devices. The address range $0040–$004F are RAM locations on the 16K and 8K devices. There are no MC9S08RG8/16 devices.

High-page registers, shown in Table 4-2, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at $1800.

Table 4-2. High-Page Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$1800	SRS	POR	PIN	COP	ILOP	ILAD[1]	0	LVD	0
$1801	SBDFR	0	0	0	0	0	0	0	BDFR
$1802	SOPT	7	COPT	STOPE	—	0	0	BKGDPE	RSTPE
$1803–$1804	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
$1805	Reserved	0	0	0	0	0	0	0	0
$1806	SDIDH	REV3	REV2	REV1	REV0	ID11	ID10	ID9	ID8
$1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
$1808	SRTISC	RTIF	RTIACK	RTICLKS	RTIE	0	RTIS2	RTIS1	RTIS0

program time provided that the conditions above are met. In the case where the next sequential address is the beginning of a new row, the program time for that byte will be the standard time instead of the burst time. This is because the high voltage to the array must be disabled and then enabled again. If a new burst command has not been queued before the current command completes, then the charge pump will be disabled and high voltage removed from the array.

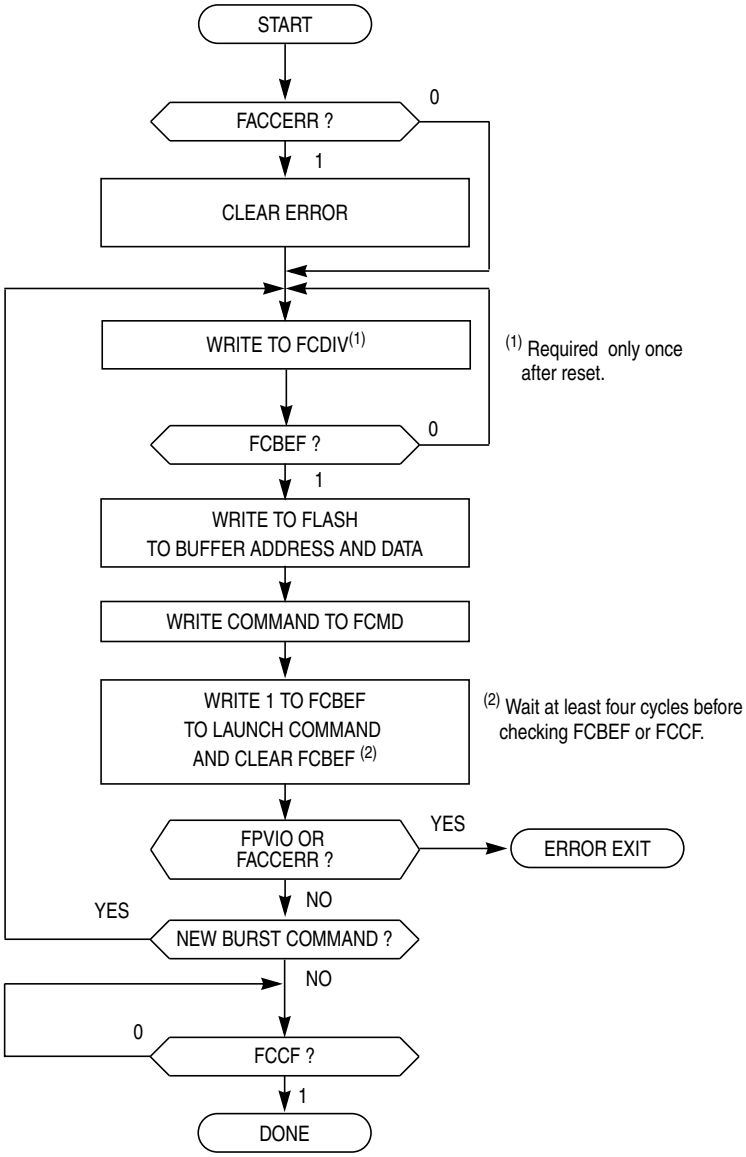


Figure 4-4. FLASH Burst Program Flowchart

4.4.5 Access Errors

An access error occurs whenever the command execution protocol is violated.

Any of the following specific actions will cause the access error flag (FACCERR) in FSTAT to be set. FACCERR must be cleared by writing a 1 to FACCERR in FSTAT before any command can be processed:

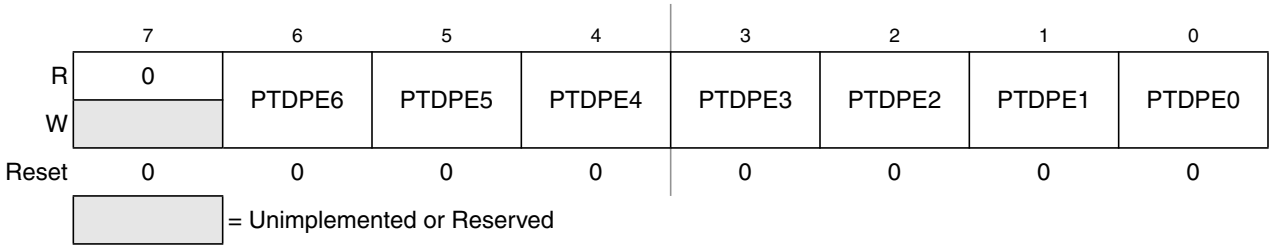


Figure 6-16. Pullup Enable for Port D (PTDPE)

Table 6-11. PTDPE Field Descriptions

Field	Description
6:0 PTDPE[6:0]	**Pullup Enable for Port D Bits** — For port D pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled. For port D pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled. 0 Internal pullup device disabled. 1 Internal pullup device enabled.

Figure 6-17. Data Direction for Port D (PTDDD)

Table 6-12. PTDDD Field Descriptions

Field	Description
6:0 PTDDD[6:0]	**Data Direction for Port D Bits** — These read/write bits control the direction of port D pins and what is read for PTDD reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port D bit n and PTDD reads return the contents of PTDDn.

	7	6	5	4	3	2	1	0
R W	PTEDD7	PTEDD6	PTEDD5	PTEDD4	PTEDD3	PTEDD2	PTEDD1	PTEDD0
Reset	0	0	0	0	0	0	0	0

Figure 6-20. Data Direction for Port E (PTEDD)

Table 6-15. PTEDD Field Descriptions

Field	Description
7:0 PTEDD[7:0]	**Data Direction for Port E Bits** — These read/write bits control the direction of port E pins and what is read for PTED reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port E bit n and PTED reads return the contents of PTEDn.

generation of 100 percent duty cycle is not necessary). This is not a significant limitation because the resulting period is much longer than required for normal applications.

TPM1MODH:TPM1MODL = $0000 is a special case that should not be used with center-aligned PWM mode. When CPWMS = 0, this case corresponds to the counter running free from $0000 through $FFFF, but when CPWMS = 1 the counter needs a valid match to the modulus register somewhere other than at $0000 in order to change directions from up-counting to down-counting.

Figure 10-4 shows the output compare value in the TPM channel registers (multiplied by 2), which determines the pulse width (duty cycle) of the CPWM signal. If ELSnA = 0, the compare match while counting up forces the CPWM output signal low and a compare match while counting down forces the output high. The counter counts up until it reaches the modulo setting in TPM1MODH:TPM1MODL, then counts down until it reaches zero. This sets the period equal to two times TPM1MODH:TPM1MODL.

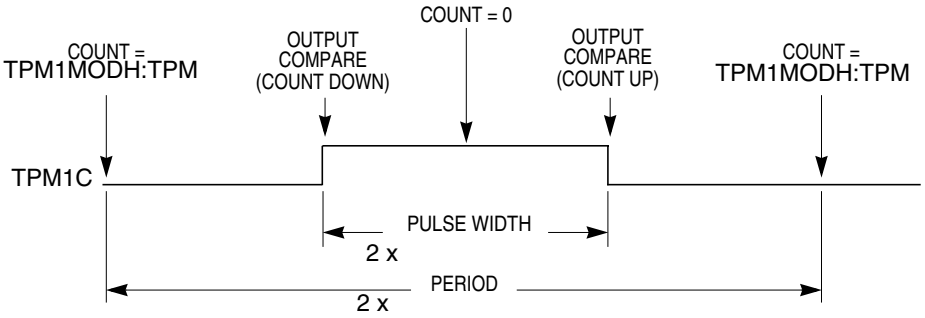


Figure 10-4. CPWM Period and Pulse Width (ELSnA = 0)

Center-aligned PWM outputs typically produce less noise than edge-aligned PWMs because fewer I/O pin transitions are lined up at the same system clock edge. This type of PWM is also required for some types of motor drives.

Because the HCS08 is a family of 8-bit MCUs, the settings in the timer channel registers are buffered to ensure coherent 16-bit updates and to avoid unexpected PWM pulse widths. Writes to any of the registers, TPM1MODH, TPM1MODL, TPM1CnVH, and TPM1CnVL, actually write to buffer registers. Values are transferred to the corresponding timer channel registers only after both 8-bit bytes of a 16-bit register have been written and the timer counter overflows (reverses direction from up-counting to down-counting at the end of the terminal count in the modulus register). This TPM1CNT overflow requirement only applies to PWM channels, not output compares.

Optionally, when TPM1CNTH:TPM1CNTL = TPM1MODH:TPM1MODL, the TPM can generate a TOF interrupt at the end of this count. The user can choose to reload any number of the PWM buffers, and they will all update simultaneously at the start of a new period.

Writing to TPM1SC cancels any values written to TPM1MODH and/or TPM1MODL and resets the coherency mechanism for the modulo registers. Writing to TPM1CnSC cancels any values written to the channel value registers and resets the coherency mechanism for TPM1CnVH:TPM1CnVL.

10.7.1 Timer Status and Control Register (TPM1SC)

TPM1SC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.

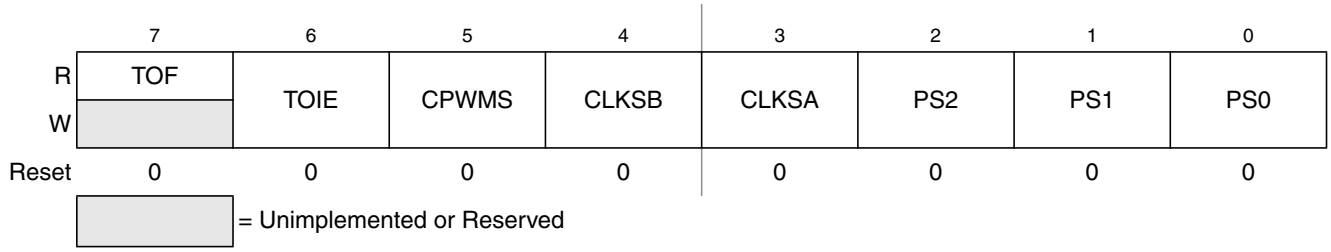


Figure 10-5. Timer Status and Control Register (TPM1SC)

Table 10-1. TPM1SC Register Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — This flag is set when the TPM counter changes to $0000 after reaching the modulo value programmed in the TPM counter modulo registers. When the TPM is configured for CPWM, TOF is set after the counter has reached the value in the modulo register, at the transition to the next lower count value. Clear TOF by reading the TPM status and control register when TOF is set and then writing a 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. Reset clears TOF. Writing a 1 to TOF has no effect. 0 TPM counter has not reached modulo value or overflow 1 TPM counter has overflowed
6 TOIE	**Timer Overflow Interrupt Enable** — This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals 1. Reset clears TOIE. 0 TOF interrupts inhibited (use software polling) 1 TOF interrupts enabled
5 CPWMS	**Center-Aligned PWM Select** — This read/write bit selects CPWM operating mode. Reset clears this bit so the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up-/down-counting mode for CPWM functions. Reset clears CPWMS. 0 All TPM1 channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register 1 All TPM1 channels operate in center-aligned PWM mode
4:3 CLKS[B:A]	**Clock Source Select** — As shown in Table 10-2, this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The external source and the XCLK are synchronized to the bus clock by an on-chip synchronization circuit.
2:0 PS[2:0]	**Prescale Divisor Select** — This 3-bit field selects one of eight divisors for the TPM clock input as shown in Table 10-3. This prescaler is located after any clock source synchronization or clock source selection, so it affects whatever clock source is selected to drive the TPM system.

has one full character time after RDRF is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCI1D. The RDRF flag is cleared automatically by a 2-step sequence which is normally satisfied in the course of the user's program that handles receive data. Refer to Section 12.3.4, "Interrupts and Status Flags," for more details about flag clearing.

12.3.3.1 Data Sampling Technique

The SCI receiver uses a 16× baud rate clock for sampling. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD1 serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock is used to divide the bit time into 16 segments labeled RT1 through RT16. When a falling edge is located, three more samples are taken at RT3, RT5, and RT7 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at RT8, RT9, and RT10 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at RT3, RT5, and RT7 are 0 even if one or all of the samples taken at RT8, RT9, and RT10 are 1s. If any sample in any bit time (including the start and stop bits) in a character frame fails to agree with the logic level for that bit, the noise flag (NF) will be set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges, and if an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if FE is still set.

12.3.3.2 Receiver Wakeup Operation

Receiver wakeup is a hardware mechanism that allows an SCI receiver to ignore the characters in a message that is intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up (RWU) control bit in SCI1C2. When RWU = 1, it inhibits setting of the status flags associated with the receiver, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.

13.2.3 SPI Baud Rate Generation

As shown in Figure 13-4, the clock source for the SPI baud rate generator is the bus clock. The three prescale bits (SPPR2:SPPR1:SPPR0) choose a prescale divisor of 1, 2, 3, 4, 5, 6, 7, or 8. The three rate select bits (SPR2:SPR1:SPR0) divide the output of the prescaler stage by 2, 4, 8, 16, 32, 64, 128, or 256 to get the internal SPI master mode bit-rate clock.

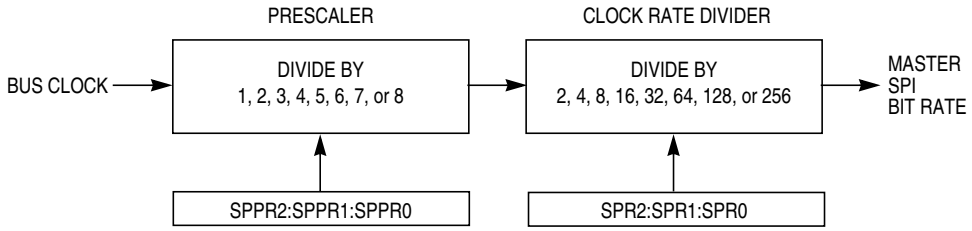


Figure 13-4. SPI Baud Rate Generation

13.3 Functional Description

An SPI transfer is initiated by checking for the SPI transmit buffer empty flag (SPTEF = 1) and then writing a byte of data to the SPI data register (SPI1D) in the master SPI device. When the SPI shift register is available, this byte of data is moved from the transmit data buffer to the shifter, SPTEF is set to indicate there is room in the buffer to queue another transmit character if desired, and the SPI serial transfer starts.

During the SPI transfer, data is sampled (read) on the MISO1 pin at one SPSCK edge and shifted, changing the bit value on the MOSI1 pin, one-half SPSCK cycle later. After eight SPSCK cycles, the data that was in the shift register of the master has been shifted out the MOSI1 pin to the slave while eight bits of data were shifted in the MISO1 pin into the master's shift register. At the end of this transfer, the received data byte is moved from the shifter into the receive data buffer and SPRF is set to indicate the data can be read by reading SPI1D. If another byte of data is waiting in the transmit buffer at the end of a transfer, it is moved into the shifter, SPTEF is set, and a new transfer is started.

Normally, SPI data is transferred most significant bit (MSB) first. If the least significant bit first enable (LSBFE) bit is set, SPI data is shifted LSB first.

When the SPI is configured as a slave, its $\overline{SS1}$ pin must be driven low before a transfer starts and $\overline{SS1}$ must stay low throughout the transfer. If a clock format where CPHA = 0 is selected, $\overline{SS1}$ must be driven to a logic 1 between successive transfers. If CPHA = 1, $\overline{SS1}$ may remain low between successive transfers. See Section 13.3.1, "SPI Clock Formats," for more details.

Because the transmitter and receiver are double buffered, a second byte, in addition to the byte currently being shifted out, can be queued into the transmit data buffer, and a previously received character can be in the receive data buffer while a new character is being shifted in. The SPTEF flag indicates when the transmit buffer has room for a new character. The SPRF flag indicates when a received character is available in the receive data buffer. The received character must be read out of the receive buffer (read SPI1D) before the next transfer is finished or a receive overrun error results.

In the case of a receive overrun, the new data is lost because the receive buffer still held the previous character and was not ready to accept the new data. There is no indication for such an overrun condition so the application system designer must ensure that previous data has been read from the receive buffer before a new transfer is initiated.

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS1}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CHPA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers.

Figure 13-6 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected ($\overline{SS}$ IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

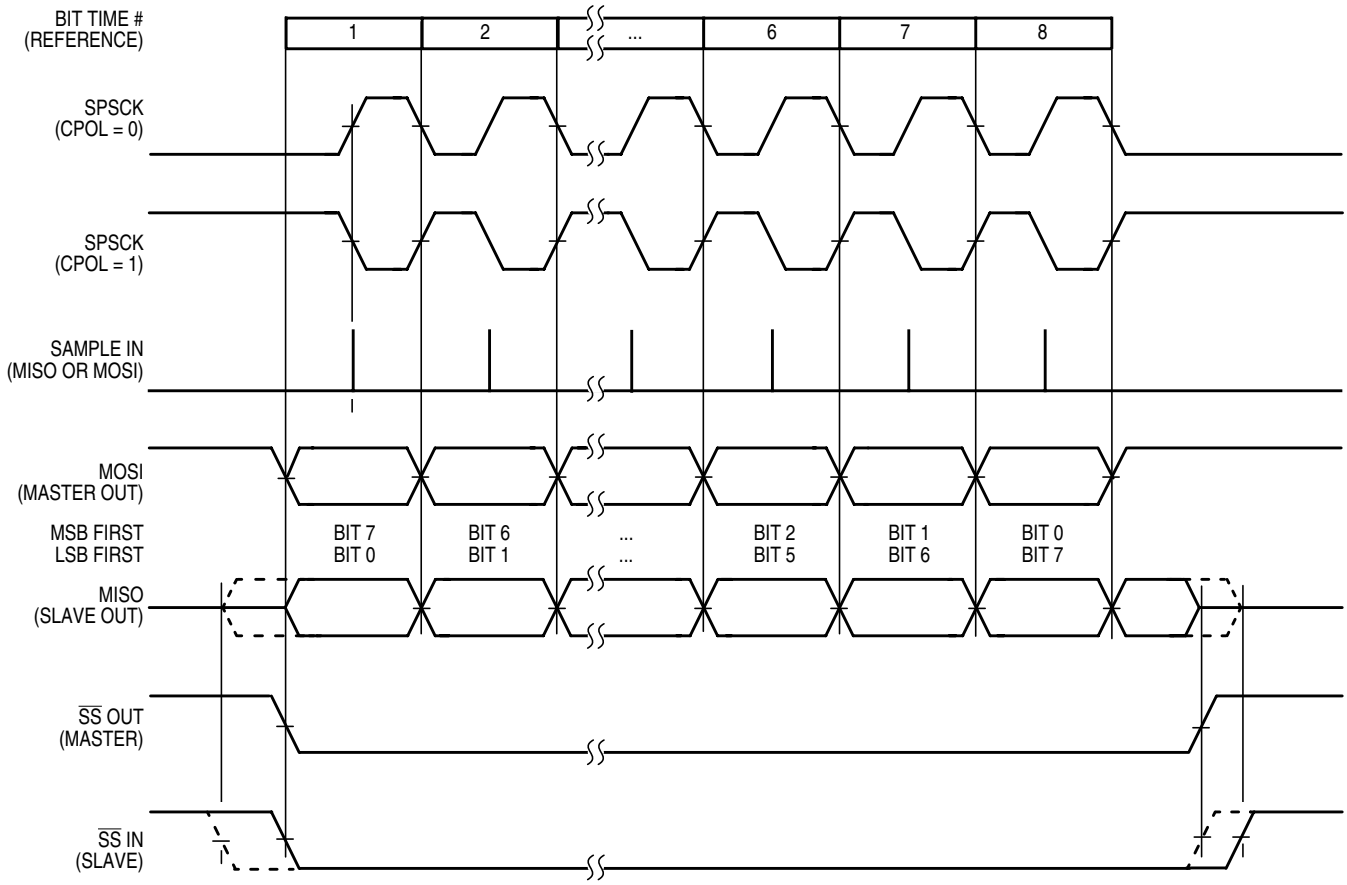


Figure 13-6. SPI Clock Formats (CPHA = 0)

When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when $\overline{SS1}$ goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's $\overline{SS}$ input must go to its inactive high level between transfers.

13.3.2 SPI Pin Controls

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to being general-purpose port I/O pins that are not controlled by the SPI.

13.3.2.1 SPSCK1 — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

13.3.2.2 MOSI1 — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data input. If SPC0 = 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and slave mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

13.3.2.3 MISO1 — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data output. If SPC0 = 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO) and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and master mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

13.3.2.4 $\overline{SS1}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN = 0), this pin is not used by the SPI and reverts to being a general-purpose port I/O pin. When the SPI is enabled as a master and MODFEN = 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE = 0) or as the slave select output (SSOE = 1).

SSOE — Slave Select Output Enable

This bit is used in combination with the mode fault enable (MODFEN) bit in SPCR2 and the master/slave (MSTR) control bit to determine the function of the $\overline{SS1}$ pin as shown in Table 13-1.

Table 13-1. $\overline{SS1}$ Pin Function

MODFEN	SSOE	Master Mode	Slave Mode
0	0	General-purpose I/O (not SPI)	Slave select input
0	1	General-purpose I/O (not SPI)	Slave select input
1	0	$\overline{SS}$ input for mode fault	Slave select input
1	1	Automatic $\overline{SS}$ output	Slave select input

LSBFE — LSB First (Shifter Direction)

1 = SPI serial data transfers start with least significant bit.
0 = SPI serial data transfers start with most significant bit.

13.4.2 SPI Control Register 2 (SPI1C2)

This read/write register is used to control optional features of the SPI system. Bits 7, 6, 5, and 2 are not implemented and always read 0.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	<st-blue> MODFEN	<st-blue> BIDIROE	0	<st-blue> SPISWAI	<st-blue> SPC0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-8. SPI Control Register 2 (SPI1C2)

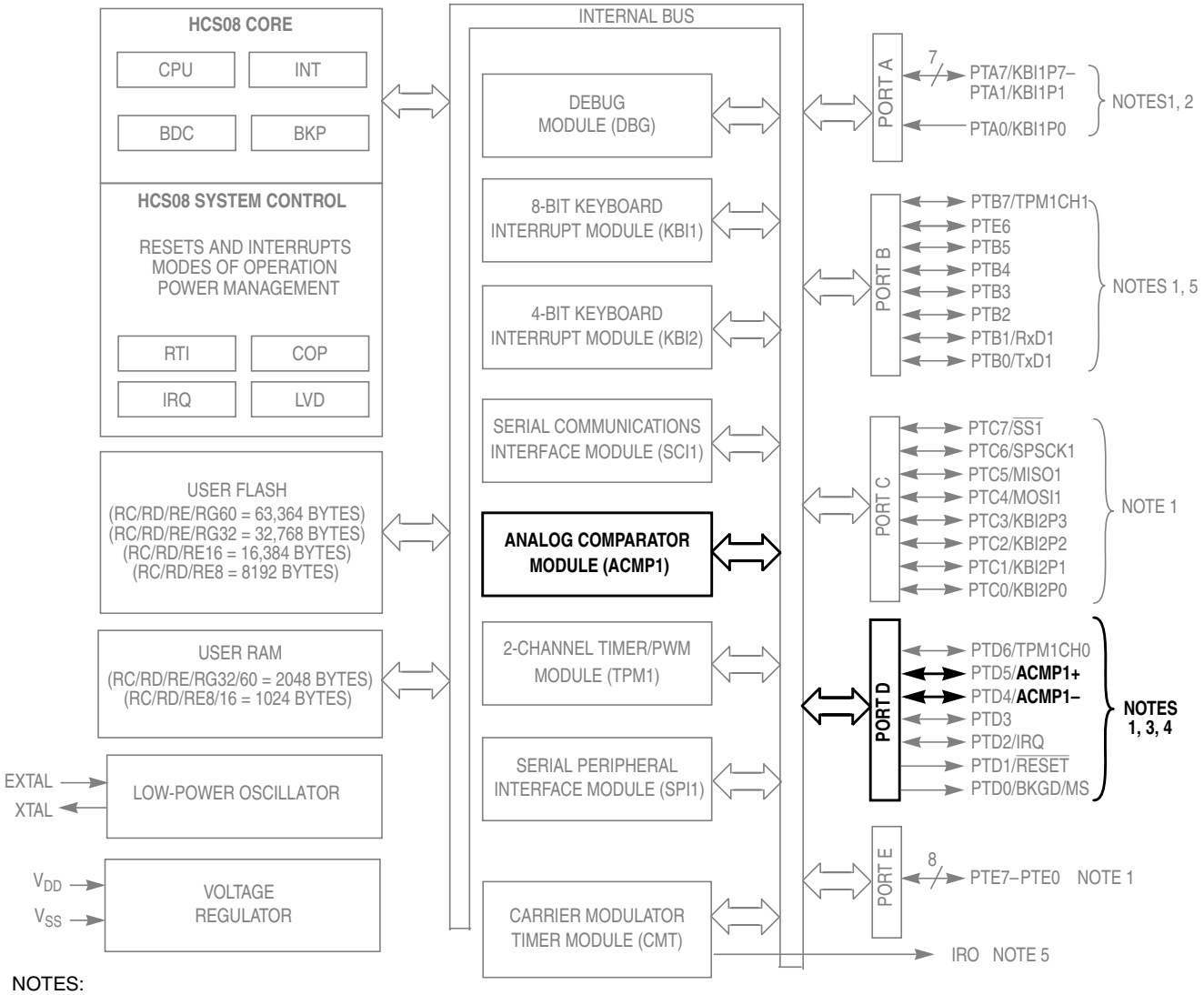
MODFEN — Master Mode-Fault Function Enable

When the SPI is configured for slave mode, this bit has no meaning or effect. (The $\overline{SS1}$ pin is the slave select input.) In master mode, this bit determines how the $\overline{SS1}$ pin is used (refer to Table 13-1 for more details).

1 = Mode fault function enabled, master $\overline{SS1}$ pin acts as the mode fault input or the slave select output.
0 = Mode fault function disabled, master $\overline{SS1}$ pin reverts to general-purpose I/O not controlled by SPI.

Chapter 14
Analog Comparator (S08ACMPV1)

The 32-, 44-, and 46-pin packages of the MC9S08RCxx, MC9S08RExx, and MC9S08RGxx devices include an analog comparator. This comparator has two inputs or can optionally use an internal bandgap reference. The comparator inputs are shared with PTD4 and PTD5 port I/O pins.



NOTES:

19.Port pins are software configurable with pullup device if input port

20.PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}. Also, PTA0 does not pullup to V_{DD} when internal pullup is enabled.

21.IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)

22.The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)

23.High current drive

24.Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 14-1. MC9S08RC/RD/RE/RG Block Diagram Highlighting ACMP Block and Pins

A.8 Oscillator Characteristics

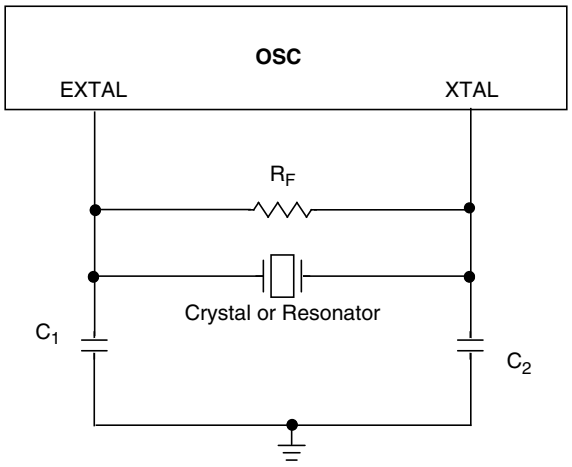


Table A-8. OSC Electrical Specifications (Temperature Range = -40 to 85°C Ambient)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Frequency	f_{OSC}	1	—	16	MHz
Load Capacitors	C_1 C_2	Note(2)			
Feedback resistor	R_F		1		MΩ

1. Data in typical column was characterized at 3.0 V, 25°C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.

A.9 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

A.9.1 Control Timing

Table A-9. Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	8	MHz
Real time interrupt internal oscillator period	t_{RTI}	400		1600	µs
External reset pulse width(1)	t_{extrst}	1.5 t_{cyc}		—	ns
Reset low drive(2)	t_{rstdrv}	34 t_{cyc}		—	ns
Active background debug mode latch setup time	t_{MSSU}	25		—	ns
Active background debug mode latch hold time	t_{MSH}	25		—	ns
IRQ pulse width(3)	t_{ILIH}	1.5 t_{cyc}		—	ns
Port rise and fall time (load = 50 pF)(4)	t_{Rise}, t_{Fall}	—	3		ns

1. This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

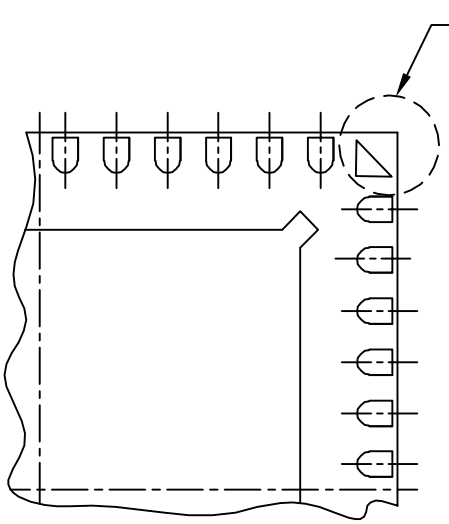
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

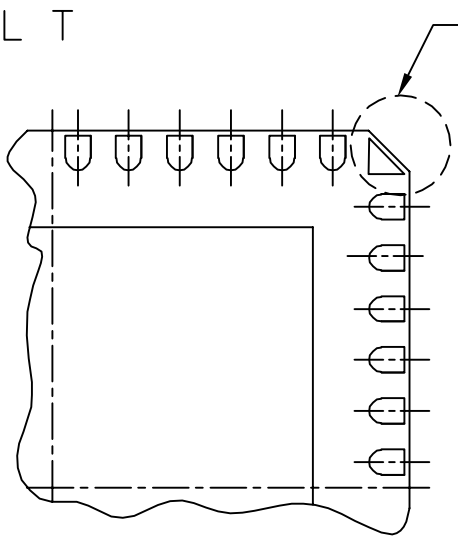
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

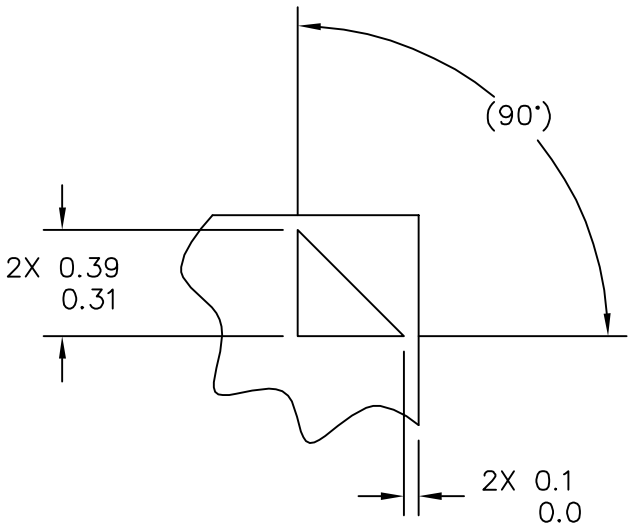
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.



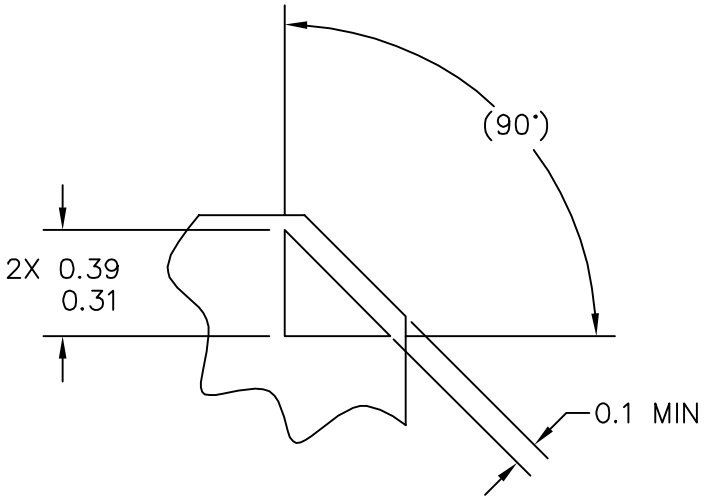
DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION2



DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION3



DETAIL T
PIN 1 BACKSIDE IDENTIFIER OPTION2



DETAIL S
PIN 1 BACKSIDE IDENTIFIER OPTION3

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)

CASE NUMBER: 1314-03
STANDARD: JEDEC-MO-220 VKKD-2
PACKAGE CODE: 6152
SHEET: 4 OF 5

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
6. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
7. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.
8. MIN METAL GAP SHOULD BE 0.2MM.