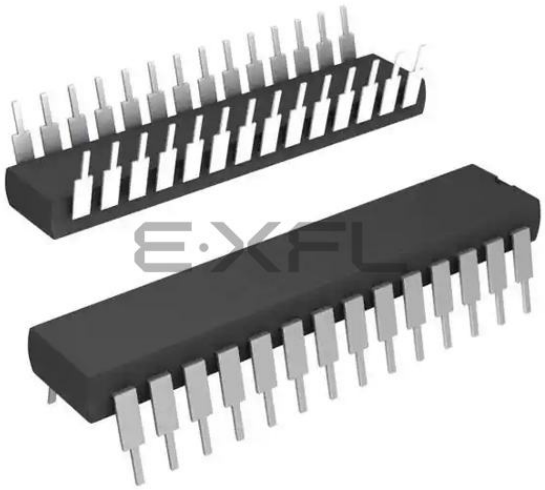

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08rd8cpe

2.3.4 Background/Mode Select (PTD0/BKGD/MS)

The background/mode select function is shared with an output-only port function on the PTD0/BKDG/MS pin. While in reset, the pin functions as a mode select pin. Immediately after reset rises, the pin functions as the background pin and can be used for background debug communication. While functioning as a background/mode select pin, this pin has an internal pullup device enabled. To use as an output-only port, BKGDPE in SOPT must be cleared.

If nothing is connected to this pin, the MCU will enter normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the rising edge of reset, which forces the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock could be as fast as the bus clock rate, so there should never be any significant capacitance connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

2.3.5 IRO Pin Description

The IRO pin is the output of the CMT. See the Carrier Modulator Timer (CMT) Module Chapter for a detailed description of this pin function.

2.3.6 General-Purpose I/O and Peripheral Ports

The remaining pins are shared among general-purpose I/O and on-chip peripheral functions such as timers and serial I/O systems. (Not all pins are available in all packages. See Table 2-2.) Immediately after reset, all 37 of these pins are configured as high-impedance general-purpose inputs with internal pullup devices disabled.

NOTE

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pullup devices or change the direction of unused pins to outputs so the pins do not float.

For information about controlling these pins as general-purpose I/O pins, see the Chapter 6, "Parallel Input/Output." For information about how and when on-chip peripheral systems use these pins, refer to the appropriate chapter from Table 2-1.

3.6 Stop Modes

One of three stop modes is entered upon execution of a STOP instruction when the STOPE bit in the system option register is set. In all stop modes, all internal clocks are halted. If the STOPE bit is not set when the CPU executes a STOP instruction, the MCU will not enter any of the stop modes and an illegal opcode reset is forced. The stop modes are selected by setting the appropriate bits in SPMSC2.

Table 3-1 summarizes the behavior of the MCU in each of the stop modes.

Table 3-1. Stop Mode Behavior

Mode	PDC	PPDC	CPU, Digital Peripherals, FLASH	RAM	OSC	ACMP	Regulator	I/O Pins	RTI
Stop1	1	0	Off	Off	Off	Standby	Standby	Reset	Off
Stop2	1	1	Off	Standby	Off	Standby	Standby	States held	Optionally on
Stop3	0	Don't care	Standby	Standby	Off	Standby	Standby	States held	Optionally on

3.6.1 Stop1 Mode

Stop1 mode provides the lowest possible standby power consumption by causing the internal circuitry of the MCU to be powered down. To enter stop1, the user must execute a STOP instruction with the PDC bit in SPMSC2 set and the PPDC bit clear. Stop1 can be entered only if the LVD reset is disabled (LVDRE = 0).

When the MCU is in stop1 mode, all internal circuits that are powered from the voltage regulator are turned off. The voltage regulator is in a low-power standby state, as are the OSC and ACMP.

Exit from stop1 is done by asserting any of the wakeup pins on the MCU: $\overline{\text{RESET}}$, IRQ, or KBI1, which have been enabled. IRQ and KBI pins are always active-low when used as wakeup pins in stop1 regardless of how they were configured before entering stop1.

Upon wakeup from stop1 mode, the MCU will start up as from a power-on reset (POR). The CPU will take the reset vector.

3.6.2 Stop2 Mode

Stop2 mode provides very low standby power consumption and maintains the contents of RAM and the current state of all of the I/O pins. To select entry into stop2 upon execution of a STOP instruction, the user must execute a STOP instruction with the PPDC and PDC bits in SPMSC2 set. Stop2 can be entered only if LVDRE = 0.

Before entering stop2 mode, the user must save the contents of the I/O port registers, as well as any other memory-mapped registers that they want to restore after exit of stop2, to locations in RAM. Upon exit from stop2, these values can be restored by user software.

When the MCU is in stop2 mode, all internal circuits that are powered from the voltage regulator are turned off, except for the RAM. The voltage regulator is in a low-power standby state, as is the ACMP. Upon entry

Table 4-1. Direct-Page Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0000	PTAD	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
$0001	PTAPE	PTAPE7	PTAPE6	PTAPE5	PTAPE4	PTAPE3	PTAPE2	PTAPE1	PTAPE0
$0002	Reserved	—	—	—	—	—	—	—	—
$0003	PTADD	PTADD7	PTADD6	PTADD5	PTADD4	PTADD3	PTADD2	PTADD1	PTADD0
$0004	PTBD	PTBD7	PTBD6	PTBD5	PTBD4	PTBD3	PTBD2	PTBD1	PTBD0
$0005	PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
$0006	Reserved	—	—	—	—	—	—	—	—
$0007	PTBDD	PTBDD7	PTBDD6	PTBDD5	PTBDD4	PTBDD3	PTBDD2	PTBDD1	PTBDD0
$0008	PTCD	PTCD7	PTCD6	PTCD5	PTCD4	PTCD3	PTCD2	PTCD1	PTCD0
$0009	PTCPE	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
$000A	Reserved	—	—	—	—	—	—	—	—
$000B	PTCDD	PTCDD7	PTCDD6	PTCDD5	PTCDD4	PTCDD3	PTCDD2	PTCDD1	PTCDD0
$000C	PTDD	0	PTDD6	PTDD5	PTDD4	PTDD3	PTDD2	PTDD1	PTDD0
$000D	PTDPE	0	PTDPE6	PTDPE5	PTDPE4	PTDPE3	PTDPE2	PTDPE1	PTDPE0
$000E	Reserved	—	—	—	—	—	—	—	—
$000F	PTDDD	0	PTDDD6	PTDDD5	PTDDD4	PTDDD3	PTDDD2	PTDDD1	PTDDD0
$0010	PTED	PTED7	PTED6	PTED5	PTED4	PTED3	PTED2	PTED1	PTED0
$0011	PTEPE	PTEPE7	PTEPE6	PTEPE5	PTEPE4	PTEPE3	PTEPE2	PTEPE1	PTEPE0
$0012	Reserved	—	—	—	—	—	—	—	—
$0013	PTEDD	PTEDD7	PTEDD6	PTEDD5	PTEDD4	PTEDD3	PTEDD2	PTEDD1	PTEDD0
$0014	KBI1SC	KBEDG7	KBEDG6	KBEDG5	KBEDG4	KBF	KBACK	KBIE	KBIMOD
$0015	KBI1PE	KBIPE7	KBIPE6	KBIPE5	KBIPE4	KBIPE3	KBIPE2	KBIPE1	KBIPE0
$0016	KBI2SC	0	0	0	0	KBF	KBACK	KBIE	KBIMOD
$0017	KBI2PE	0	0	0	0	KBIPE3	KBIPE2	KBIPE1	KBIPE0
$0018	SCI1BDH[1]	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
$0019	SCI1BDL[1]	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$001A	SCI1C1[1]	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$001B	SCI1C2[1]	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$001C	SCI1S1[1]	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
$001D	SCI1S2[1]	0	0	0	0	0	0	0	RAF
$001E	SCI1C3[1]	R8	T8	TXDIR	0	ORIE	NEIE	FEIE	PEIE
$001F	SCI1D[1]	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
$0020	CMTCGH1	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
$0021	CMTCGL1	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
$0022	CMTCGH2	SH7	SH6	SH5	SH4	SH3	SH2	SH1	SH0
$0023	CMTCGL2	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
$0024	CMTOC	IROL	CMTPOL	IROPEN	0	0	0	0	0
$0025	CMTMSC	EOCF	CMTDIV1	CMTDIV0	EXSPC	BASE	FSK	EOCIE	MCGEN
$0026	CMTCMD1	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8
$0027	CMTCMD2	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
$0028	CMTCMD3	SB15	SB14	SB13	SB12	SB11	SB10	SB9	SB8
$0029	CMTCMD4	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0

6.3 Pin Descriptions

The MC9S08RC/RD/RE/RG has a total of 39 parallel I/O pins distributed between four 8-bit ports and one 7-bit port. Not all pins are bonded out in all packages. Consult the pin assignment in Chapter 2, "Pins and Connections," for available parallel I/O pins. All of these pins are available for general-purpose I/O when they are not used by other on-chip peripheral systems.

The following paragraphs discuss each port and the software controls that determine each pin's use.

6.3.1 Port A

Port A		Bit 7	6	5	4	3	2	1	Bit 0
	MCU Pin:	PTA7/ KBI1P7	PTA6/ KBI1P6	PTA5/ KBI1P5	PTA4/ KBI1P4	PTA3/ KBI1P3	PTA2/ KBI1P2	PTA1/ KBI1P1	PTA0/ KBI1P0

Figure 6-1. Port A Pin Names

Port A is an 8-bit general-purpose I/O port shared with the KBI1 keyboard interrupt inputs. Bit 0 of port A is an input-only pin.

Port A pins are available as general-purpose I/O pins controlled by the port A data (PTAD), data direction (PTADD), and pullup enable (PTAPE) registers. Refer to Section 6.4, "Parallel I/O Controls," for more information about general-purpose I/O control.

Any of the port A pins can be configured as a KBI1 keyboard interrupt pin. Refer to the Keyboard Interrupt (KBI) Module chapter for more information about using port A pins as keyboard interrupt pins.

6.3.2 Port B

Port B		Bit 7	6	5	4	3	2	1	Bit 0
	MCU Pin:	PTB7/ TPM1CH1	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1/ RxD1	PTB0/ TxD1

Figure 6-2. Port B Pin Names

Port B is an 8-bit general-purpose I/O port with two pins shared with the SCI and one pin shared with the TPM. The port B output drivers are capable of high current drive.

Port B pins are available as general-purpose I/O pins controlled by the port B data (PTBD), data direction (PTBDD), and pullup enable (PTBPE) registers. Refer to Section 6.4, "Parallel I/O Controls," for more information about general-purpose I/O control.

When the SCI module is enabled, PTB0 and PTB1 function as the transmit (TxD1) and receive (RxD1) pins of the SCI. Refer to the Serial Communications Interface (SCI) Module chapter for more information about using PTB0 and PTB1 as SCI pins.

The TPM can be configured to use PTB7 as either an input capture, output compare, or PWM pin. Refer to the Timer/PWM Module (TPM) Module chapter for more information about using PTB7 as a timer pin.

Table 7-2. HCS08 Instruction Set Summary (Sheet 2 of 7)

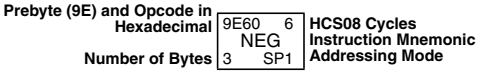
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles[1]
			V	H	I	N	Z	C				
BCLR *n,opr8a*	Clear Bit n in Memory	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	Branch if (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE *rel*	Branch if Greater Than or Equal To (Signed Operands)	Branch if (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGND	Enter Active Background if ENBDM = 1	Waits For and Processes BDM Commands Until GO, TRACE1, or TAGGO	–	–	–	–	–	–	INH	82		5+
BGT *rel*	Branch if Greater Than (Signed Operands)	Branch if (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	Branch if (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	Branch if (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	Branch if (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS *rel*	Branch if Higher or Same (Same as BCC)	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	Branch if IRQ pin = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	Branch if IRQ pin = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT *#opr8i* BIT *opr8a* BIT *opr16a* BIT *oprx16*,X BIT *oprx8*,X BIT ,X BIT *oprx16*,SP BIT *oprx8*,SP	Bit Test	(A) & (M) (CCR Updated but Operands Not Changed)	0	–	–			–	IMM DIR EXT IX2 IX1 IX SP2 SP1	A5 B5 C5 D5 E5 F5 9ED5 9EE5	ii dd hh ll ee ff ff ee ff ff	2 3 4 4 3 3 5 4
BLE *rel*	Branch if Less Than or Equal To (Signed Operands)	Branch if (Z) ǀ (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO *rel*	Branch if Lower (Same as BCS)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	Branch if (C) ǀ (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT *rel*	Branch if Less Than (Signed Operands)	Branch if (N ⊕ V) = 1	–	–	–	–	–	–	REL	91	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	Branch if (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI *rel*	Branch if Minus	Branch if (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	Branch if (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	Branch if (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	Branch if (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	No Test	–	–	–	–	–	–	REL	20	rr	3

Table 7-3. Opcode Map (Sheet 2 of 2)

Bit-Manipulation		Branch	Read-Modify-Write					Control		Register/Memory					
						9E60 6 NEG 3 SP1							9ED0 5 SUB 4 SP2	9EE0 4 SUB 3 SP1	
						9E61 6 CBEQ 4 SP1							9ED1 5 CMP 4 SP2	9EE1 4 CMP 3 SP1	
													9ED2 5 SBC 4 SP2	9EE2 4 SBC 3 SP1	
						9E63 6 COM 3 SP1							9ED3 5 CPX 4 SP2	9EE3 4 CPX 3 SP1	9EF3 6 CPHX 3 SP1
						9E64 6 LSR 3 SP1							9ED4 5 AND 4 SP2	9EE4 4 AND 3 SP1	
													9ED5 5 BIT 4 SP2	9EE5 4 BIT 3 SP1	
						9E66 6 ROR 3 SP1							9ED6 5 LDA 4 SP2	9EE6 4 LDA 3 SP1	
						9E67 6 ASR 3 SP1							9ED7 5 STA 4 SP2	9EE7 4 STA 3 SP1	
						9E68 6 LSL 3 SP1							9ED8 5 EOR 4 SP2	9EE8 4 EOR 3 SP1	
						9E69 6 ROL 3 SP1							9ED9 5 ADC 4 SP2	9EE9 4 ADC 3 SP1	
						9E6A 6 DEC 3 SP1							9EDA 5 ORA 4 SP2	9EEA 4 ORA 3 SP1	
						9E6B 8 DBNZ 4 SP1							9EDB 5 ADD 4 SP2	9EEB 4 ADD 3 SP1	
						9E6C 6 INC 3 SP1									
						9E6D 5 TST 3 SP1									
										9EAE 5 LDHX 2 IX	9EBE 6 LDHX 4 IX2	9ECE 5 LDHX 3 IX1	9EDE 5 LDX 4 SP2	9EEE 4 LDX 3 SP1	9EFE 5 LDHX 3 SP1
						9E6F 6 CLR 3 SP1							9EDF 5 STX 4 SP2	9EEF 4 STX 3 SP1	9EFF 5 STHX 3 SP1

INH	**Inherent**	**REL**	**Relative**	**SP1**	**Stack Pointer, 8-Bit Offset**
IMM	**Immediate**	**IX**	**Indexed, No Offset**	**SP2**	**Stack Pointer, 16-Bit Offset**
DIR	**Direct**	**IX1**	**Indexed, 8-Bit Offset**	**IX+**	**Indexed, No Offset with**
EXT	**Extended**	**IX2**	**Indexed, 16-Bit Offset**		**Post Increment**
DD	**DIR to DIR**	**IMD**	**IMM to DIR**	**IX1+**	**Indexed, 1-Byte Offset with**
IX+D	**IX+ to DIR**	**DIX+**	**DIR to IX+**		**Post Increment**

Note: All Sheet 2 Opcodes are Preceded by the Page 2 Prebyte (9E)



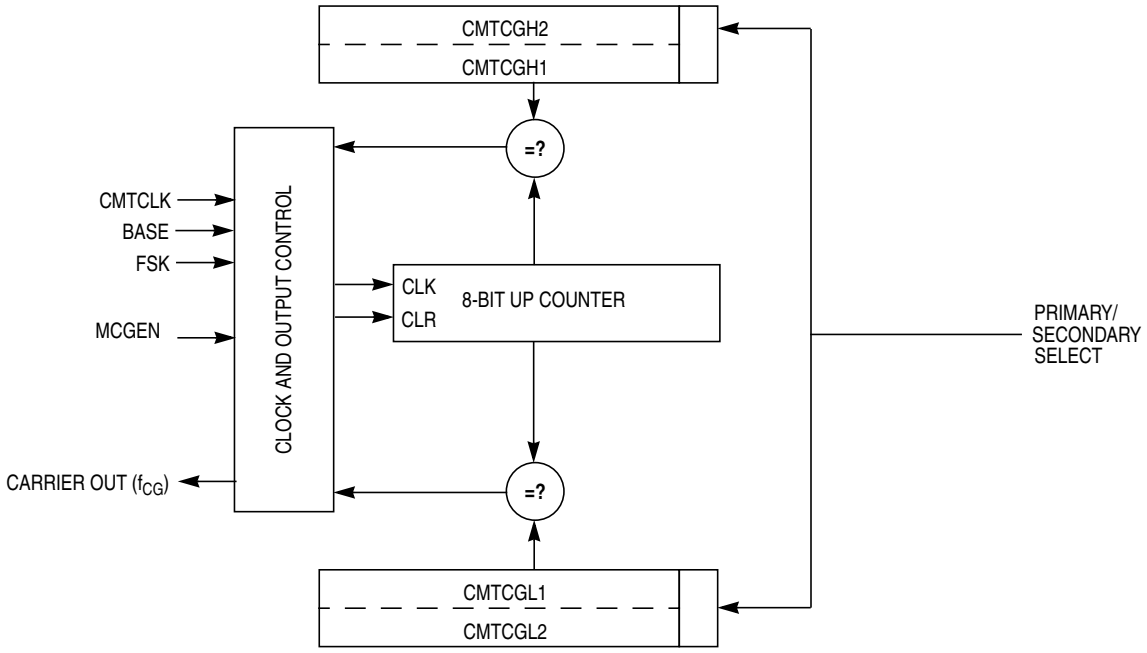


Figure 8-3. Carrier Generator Block Diagram

The high/low time counter is an 8-bit up counter. After each increment, the contents of the counter are compared with the appropriate high or low count value register. When the compare value is reached, the counter is reset to a value of $01, and the compare is redirected to the other count value register.

Assuming that the high time count compare register is currently active, a valid compare will cause the carrier output to be driven low. The counter will continue to increment (starting at reset value of $01). When the value stored in the selected low count value register is reached, the counter will again be reset and the carrier output will be driven high.

The cycle repeats, automatically generating a periodic signal that is directed to the modulator. The lowest frequency (maximum period) and highest frequency (minimum period) that can be generated are defined as:

$$f_{max} = f_{CMTCLK} \div (2 \times 1) \text{ Hz} \qquad \textit{Eqn. 8-1}$$

$$f_{min} = f_{CMTCLK} \div (2 \times (2^8 - 1)) \text{ Hz} \qquad \textit{Eqn. 8-2}$$

In the general case, the carrier generator output frequency is:

$$f_{CG} = f_{CMTCLK} \div (\text{Highcount} + \text{Lowcount}) \text{ Hz} \qquad \textit{Eqn. 8-3}$$

Where: $0 < \textit{Highcount} < 256$ and
$0 < \textit{Lowcount} < 256$

Chapter 10
Timer/PWM Module (S08TPMV1)

10.1 Introduction

The MC9S08RC/RD/RE/RG includes a timer/PWM (TPM) module that supports traditional input capture, output compare, or buffered edge-aligned pulse-width modulation (PWM) on each channel. A control bit in the TPM configures both channels in the timer to operate as center-aligned PWM functions. Timing functions in the TPM are based on a 16-bit counter with prescaler and modulo features to control frequency and range (period between overflows) of the time reference. This timing system is ideally suited for a wide range of control applications. The MC9S08RC/RD/RE/RG devices do not have a separate fixed internal clock source (XCLK). If the XCLK source is selected using the CLKSA and CLKSB control bits (see Table 10-2), the TPM will use the BUSCLK.

10.2 Features

Timer system features include:

- Two separate channels:
  - Each channel may be input capture, output compare, or buffered edge-aligned PWM
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs
- The TPM may be configured for buffered, center-aligned pulse-width modulation (CPWM) on both channels
- Clock source to prescaler for the TPM is selectable between the bus clock or an external pin:
  - Prescale taps for divide by 1, 2, 4, 8, 16, 32, 64, or 128
  - External clock input shared with TPM1CH0 timer channel pin
- 16-bit modulus register to control counter range
- Timer system enable
- One interrupt per channel plus terminal count interrupt

10.3 TPM Block Diagram

The TPM uses one input/output (I/O) pin per channel, TPM1CHn where n is the channel number (for example, 0–4). The TPM shares its I/O pins with general-purpose I/O port pins (refer to the Pins and Connections chapter for more information). Figure 10-2 shows the structure of a TPM. Some MCUs include more than one TPM, with various numbers of channels.

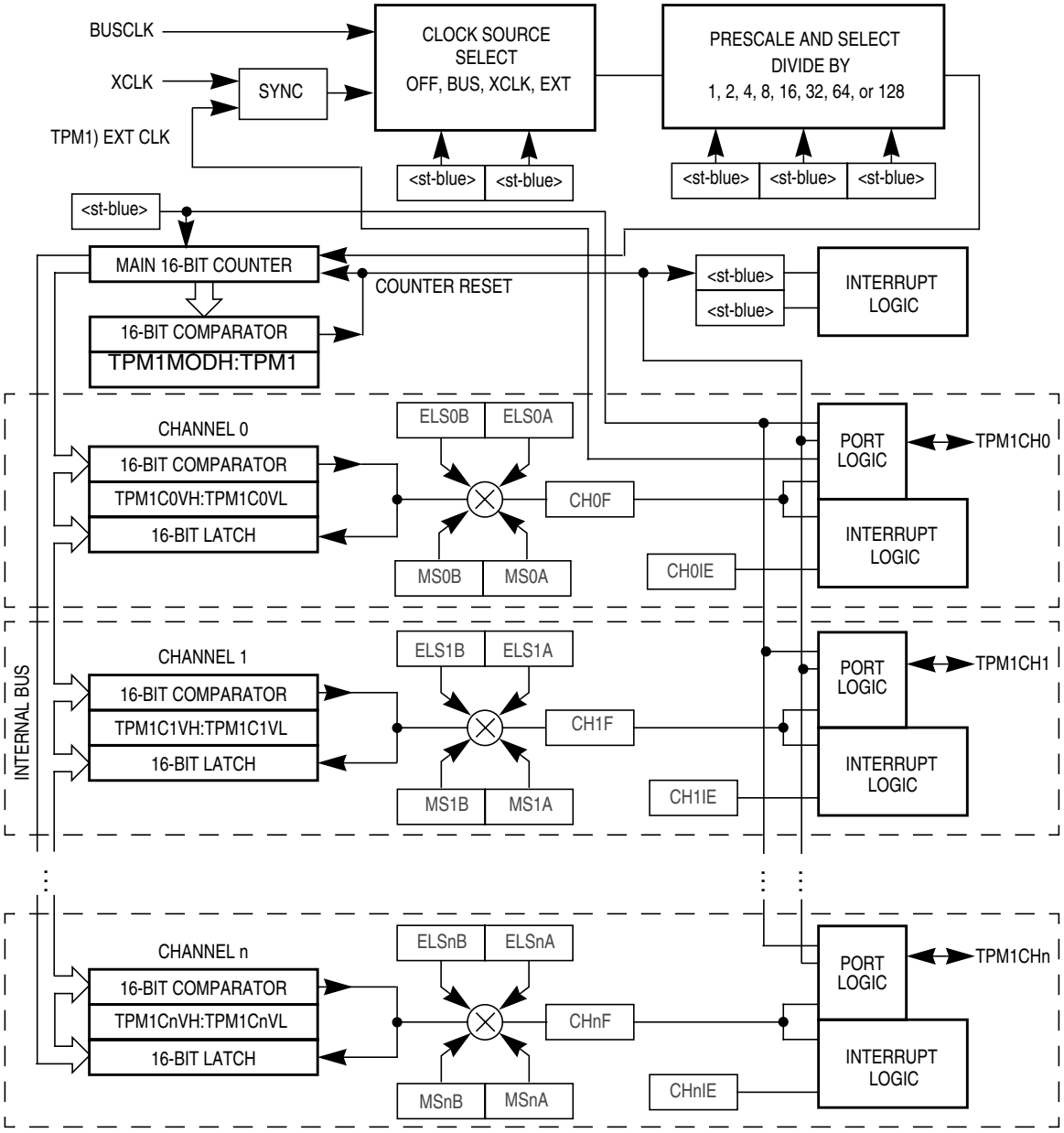


Figure 10-2. TPM Block Diagram

The central component of the TPM is the 16-bit counter that can operate as a free-running counter, a modulo counter, or an up-/down-counter when the TPM is configured for center-aligned PWM. The TPM counter (when operating in normal up-counting mode) provides the timing reference for the input capture,

Because the HCS08 MCU is an 8-bit architecture, a coherency mechanism is built into the timer counter for read operations. Whenever either byte of the counter is read (TPM1CNTH or TPM1CNTL), both bytes are captured into a buffer so when the other byte is read, the value will represent the other byte of the count at the time the first byte was read. The counter continues to count normally, but no new value can be read from either byte until both bytes of the old count have been read.

The main timer counter can be reset manually at any time by writing any value to either byte of the timer count TPM1CNTH or TPM1CNTL. Resetting the counter in this manner also resets the coherency mechanism in case only one byte of the counter was read before resetting the count.

10.5.2 Channel Mode Selection

Provided CPWMS = 0 (center-aligned PWM operation is not specified), the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and buffered edge-aligned PWM.

10.5.2.1 Input Capture Mode

With the input capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TPM latches the contents of the TPM counter into the channel value registers (TPM1CnVH:TPM1CnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

When either byte of the 16-bit capture register is read, both bytes are latched into a buffer to support coherent 16-bit accesses regardless of order. The coherency sequence can be manually reset by writing to the channel status/control register (TPM1CnSC).

An input capture event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.2 Output Compare Mode

With the output compare function, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter reaches the value in the channel value registers of an output compare channel, the TPM can set, clear, or toggle the channel pin.

In output compare mode, values are transferred to the corresponding timer channel value registers only after both 8-bit bytes of a 16-bit register have been written. This coherency sequence can be manually reset by writing to the channel status/control register (TPM1CnSC).

An output compare event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.3 Edge-Aligned PWM Mode

This type of PWM output uses the normal up-counting mode of the timer counter (CPWMS = 0) and can be used when other channels in the same TPM are configured for input capture or output compare functions. The period of this PWM signal is determined by the setting in the modulus register (TPM1MODH:TPM1MODL). The duty cycle is determined by the setting in the timer channel value

When background mode is active, the timer counter and the coherency mechanism are frozen such that the buffer latches remain in the state they were in when the background mode became active even if one or both bytes of the counter are read while background mode is active.

10.7.3 Timer Counter Modulo Registers (TPM1MODH:TPM1MODL)

The read/write TPM modulo registers contain the modulo value for the TPM counter. After the TPM counter reaches the modulo value, the TPM counter resumes counting from $0000 at the next clock (CPWMS = 0) or starts counting down (CPWMS = 1), and the overflow flag (TOF) becomes set. Writing to TPM1MODH or TPM1MODL inhibits the TOF bit and overflow interrupts until the other byte is written. Reset sets the TPM counter modulo registers to $0000, which results in a free-running timer counter (modulo disabled).

	7	6	5	4	3	2	1	0
R W	Bit 15	14	13	12	11	10	9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 10-8. Timer Counter Modulo Register High (TPM1MODH)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 10-9. Timer Counter Modulo Register Low (TPM1MODL)

It is good practice to wait for an overflow interrupt so both bytes of the modulo register can be written well before a new overflow. An alternative approach is to reset the TPM counter before writing to the TPM modulo registers to avoid confusion about when the first counter overflow will occur.

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS1}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CHPA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers.

Figure 13-6 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected ($\overline{SS}$ IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

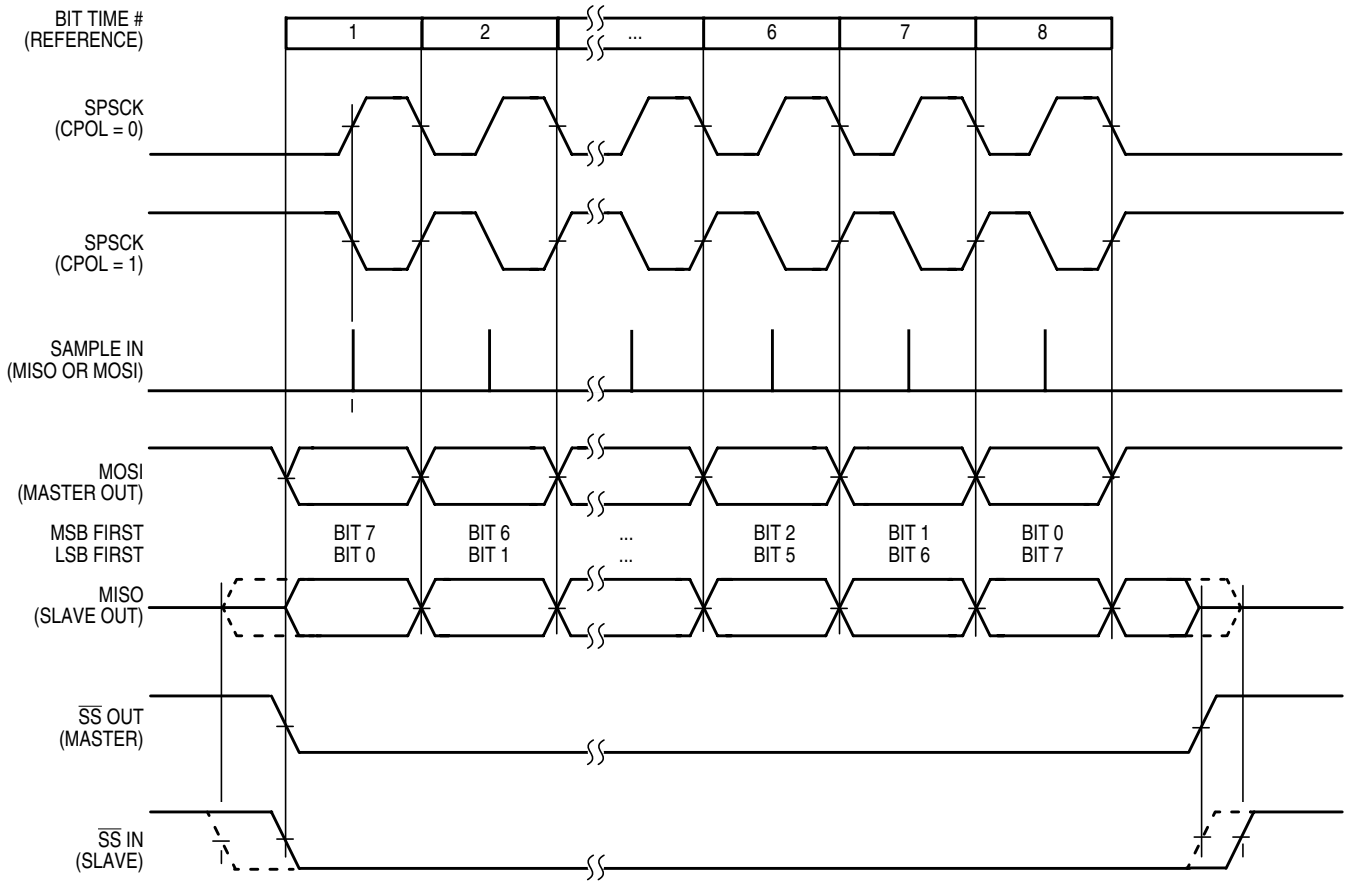


Figure 13-6. SPI Clock Formats (CPHA = 0)

When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when $\overline{SS1}$ goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's $\overline{SS}$ input must go to its inactive high level between transfers.

13.3.2 SPI Pin Controls

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to being general-purpose port I/O pins that are not controlled by the SPI.

13.3.2.1 SPSCK1 — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

13.3.2.2 MOSI1 — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data input. If SPC0 = 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and slave mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

13.3.2.3 MISO1 — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data output. If SPC0 = 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO) and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and master mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

13.3.2.4 $\overline{SS1}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN = 0), this pin is not used by the SPI and reverts to being a general-purpose port I/O pin. When the SPI is enabled as a master and MODFEN = 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE = 0) or as the slave select output (SSOE = 1).

13.4.1 SPI Control Register 1 (SPI1C1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

Figure 13-7. SPI Control Register 1 (SPI1C1)

SPIE — SPI Interrupt Enable (for SPRF and MODF)

This is the interrupt enable for SPI receive buffer full (SPRF) and mode fault (MODF) events.
1 = When SPRF or MODF is 1, request a hardware interrupt.
0 = Interrupts from SPRF and MODF inhibited (use polling).

SPE — SPI System Enable

Disabling the SPI halts any transfer that is in progress, clears data buffers, and initializes internal state machines. SPRF is cleared and SPTEF is set to indicate the SPI transmit data buffer is empty.
1 = SPI system enabled.
0 = SPI system inactive.

SPTIE — SPI Transmit Interrupt Enable

This is the interrupt enable bit for SPI transmit buffer empty (SPTEF).
1 = When SPTEF is 1, hardware interrupt requested.
0 = Interrupts from SPTEF inhibited (use polling).

MSTR — Master/Slave Mode Select
1 = SPI module configured as a master SPI device.
0 = SPI module configured as a slave SPI device.

CPOL — Clock Polarity

This bit effectively places an inverter in series with the clock signal from a master SPI or to a slave SPI device. Refer to Section 13.3.1, “SPI Clock Formats,” for more details.
1 = Active-low SPI clock (idles high).
0 = Active-high SPI clock (idles low).

CPHA — Clock Phase

This bit selects one of two clock formats for different kinds of synchronous serial peripheral devices. Refer to Section 13.3.1, “SPI Clock Formats,” for more details.
1 = First edge on SPSCK occurs at the start of the first cycle of an 8-cycle data transfer.
0 = First edge on SPSCK occurs at the middle of the first cycle of an 8-cycle data transfer.

Table A-5. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Maximum low-voltage safe state re-arm[3]	V_{REARM}	—	—	3.0	V
Input high voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IH}	0.70 × V_{DD}		—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}		—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—		0.35 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—		0.30 × V_{DD}	V
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}		—	V
Input leakage current (Per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	$\lvert I_{In}\rvert$	—	0.025	1.0	µA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	$\lvert I_{OZ}\rvert$	—	0.025	1.0	µA
Internal pullup resistors[4] [5]	R_{PU}	17.5		52.5	κW
Internal pulldown resistor (IRQ)	R_{PD}	17.5		52.5	κW
Output high voltage (V_{DD} ≥ 1.8 V) I_{OH} = –2 mA (ports A, C, D and E)	V_{OH}	V_{DD} – 0.5		—	V
Output high voltage (port B and IRO) I_{OH} = –10 mA (V_{DD} ≥ 2.7 V) I_{OH} = –6 mA (V_{DD} ≥ 2.3 V) I_{OH} = –3 mA (V_{DD} ≥ 1.8 V)		V_{DD} – 0.5		— — —	
Maximum total I_{OH} for all port pins	$\lvert I_{OHT}\rvert$	—		60	mA
Output low voltage (V_{DD} ≥ 1.8 V) I_{OL} = 2.0 mA (ports A, C, D and E)	V_{OL}	—		0.5	V
Output low voltage (port B) I_{OL} = 10.0 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		0.5 0.5 0.5	
Output low voltage (IRO) I_{OL} = 16 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		1.2 1.2 1.2	
Maximum total I_{OL} for all port pins	I_{OLT}	—		60	mA
dc injection current[2], [6], [7], [8],, [9] V_{IN} < V_{SS}, V_{IN} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins	$\lvert I_{IC}\rvert$	 — —		 0.2 5	 mA mA
Input capacitance (all non-supply pins)	C_{In}	—		7	pF

1. RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.
2. This parameter is characterized and not tested on each device.
3. If SAFE bit is set, V_{DD} must be above re-arm voltage to allow MCU to accept interrupts, refer to Section 5.6, “Low-Voltage Detect (LVD) System.”
4. Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.
5. The PTA0 pullup resistor may not pull up to the specified minimum V_{IH}. However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no dc load is present on the pin.
6. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

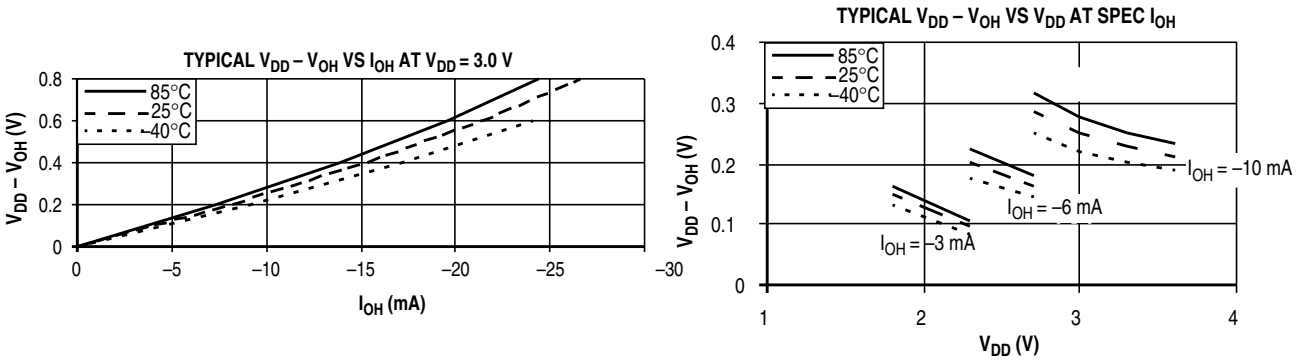


Figure A-4. Typical High-Side Driver (Source) Characteristics (Port B and IRO)

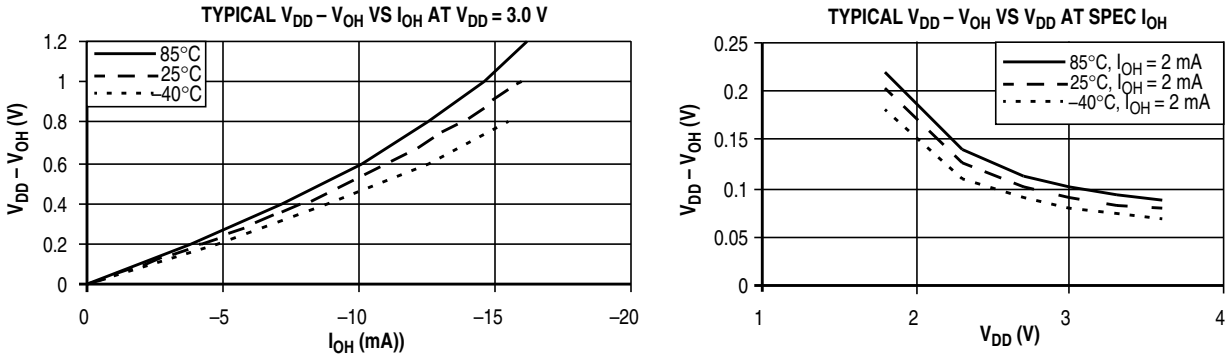


Figure A-5. Typical High-Side (Source) Characteristics (Ports A, C, D and E)

A.8 Oscillator Characteristics

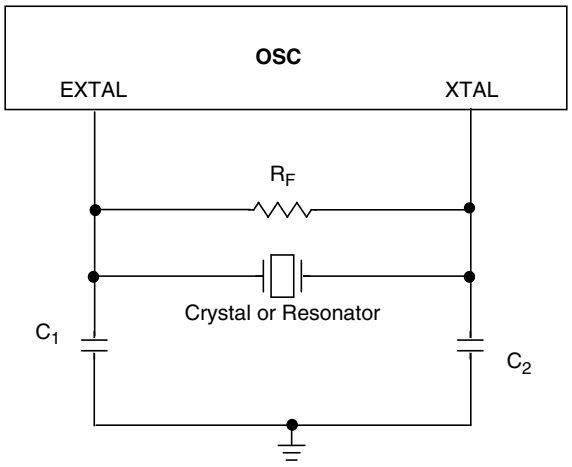


Table A-8. OSC Electrical Specifications (Temperature Range = -40 to 85°C Ambient)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Frequency	f_{OSC}	1	—	16	MHz
Load Capacitors	C_1 C_2	Note(2)			
Feedback resistor	R_F		1		MΩ

1. Data in typical column was characterized at 3.0 V, 25°C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.

A.9 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

A.9.1 Control Timing

Table A-9. Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	8	MHz
Real time interrupt internal oscillator period	t_{RTI}	400		1600	µs
External reset pulse width(1)	t_{extrst}	1.5 t_{cyc}		—	ns
Reset low drive(2)	t_{rstdrv}	34 t_{cyc}		—	ns
Active background debug mode latch setup time	t_{MSSU}	25		—	ns
Active background debug mode latch hold time	t_{MSH}	25		—	ns
IRQ pulse width(3)	t_{ILIH}	1.5 t_{cyc}		—	ns
Port rise and fall time (load = 50 pF)(4)	t_{Rise}, t_{Fall}	—	3		ns

1. This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

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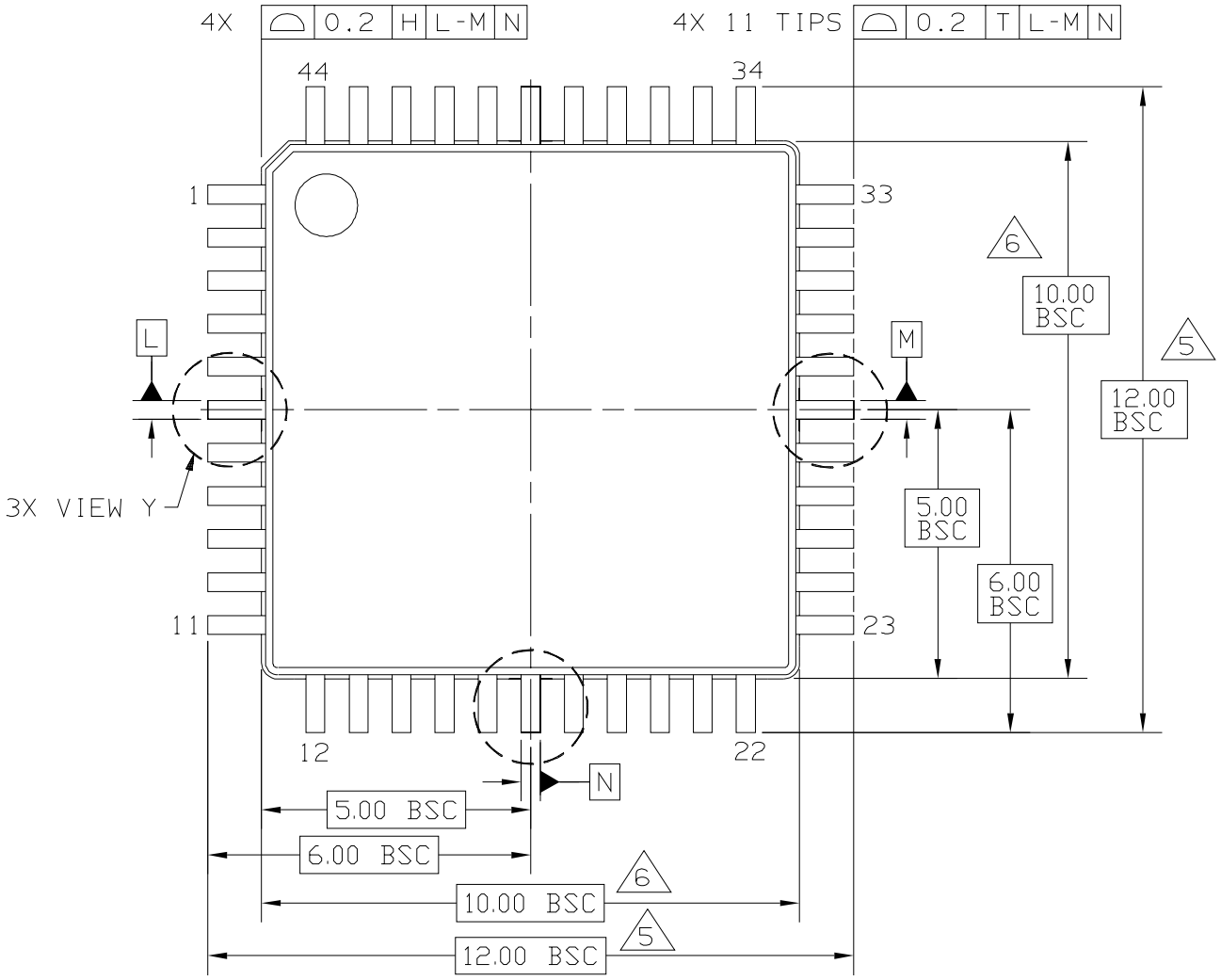

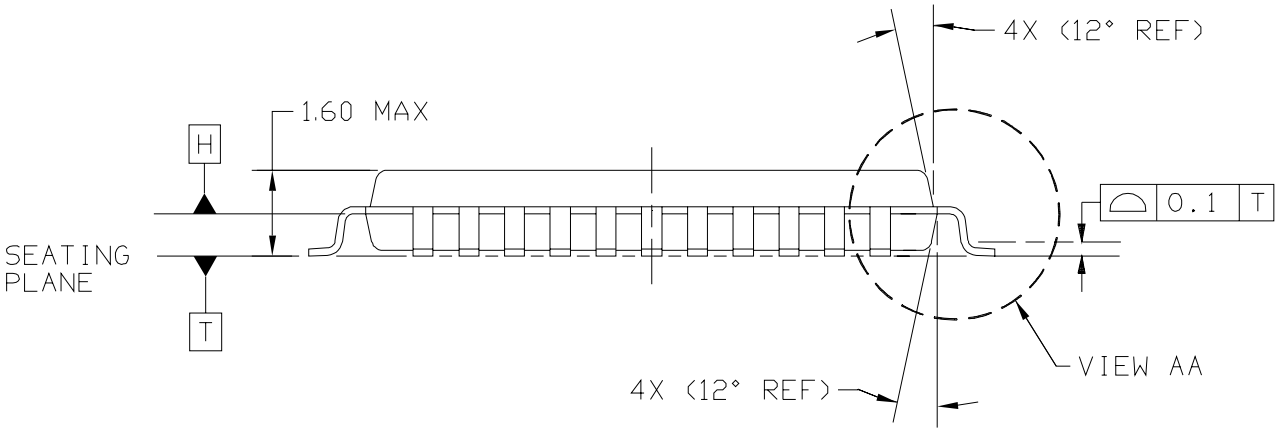

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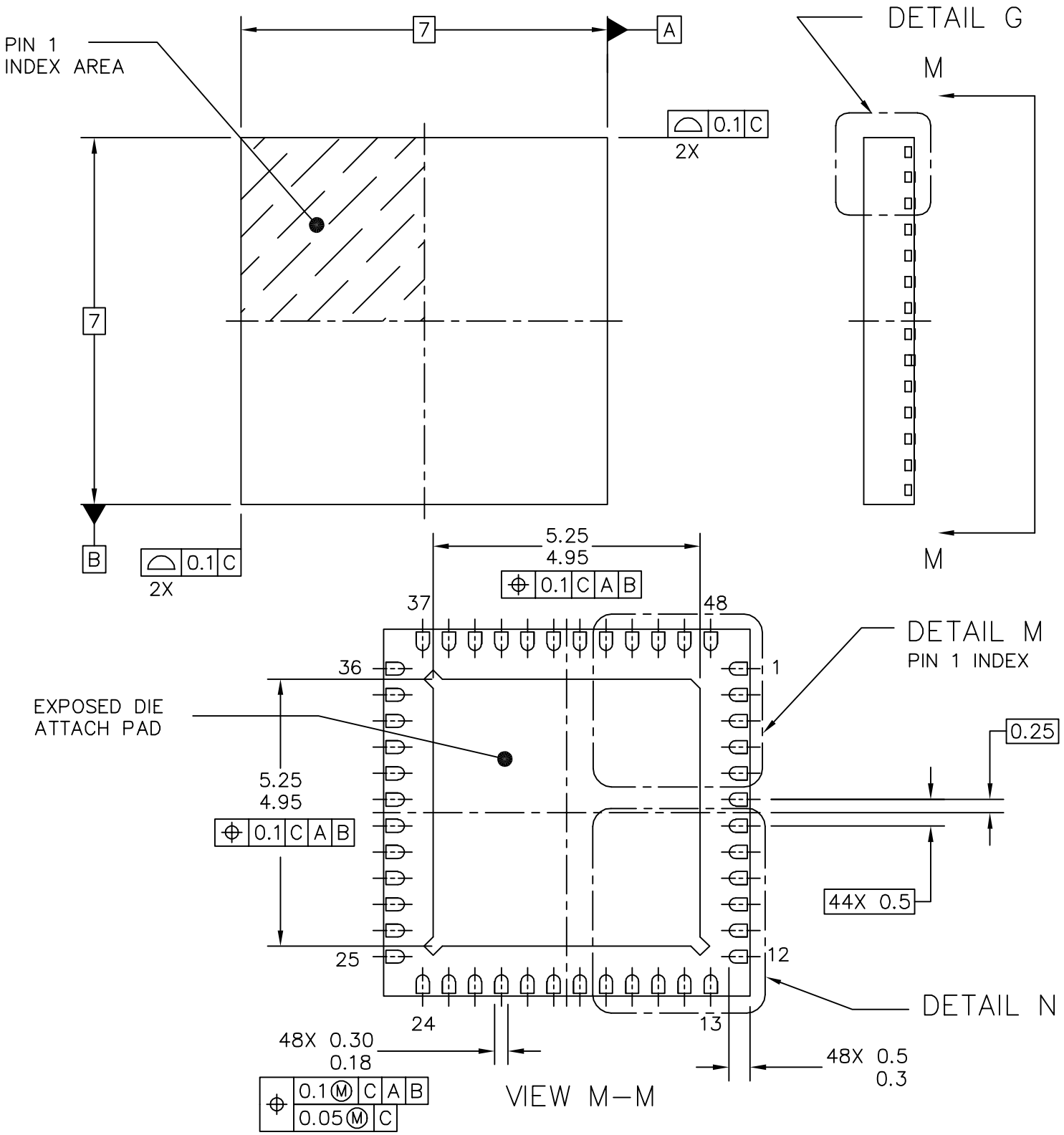

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