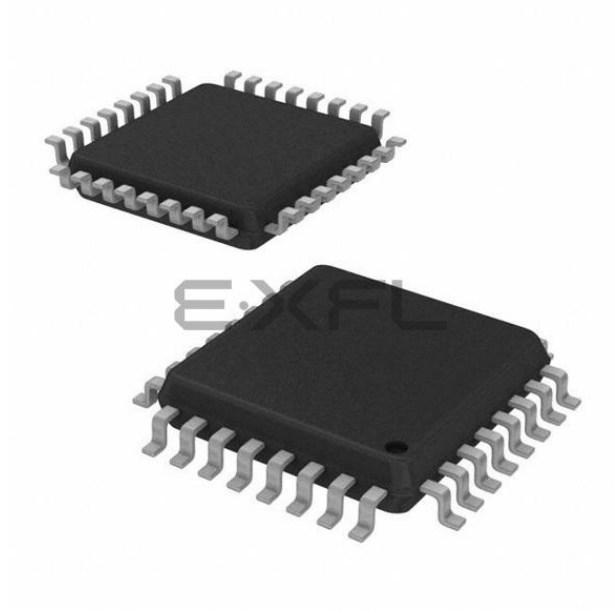


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08rd8fje

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

13.3.2.3 MISO1 — Master Data In, Slave Data Out 170
13.3.2.4 $\overline{SS1}$ — Slave Select 170
13.3.3 SPI Interrupts 171
13.3.4 Mode Fault Detection 171
13.4 SPI Registers and Control Bits 171
13.4.1 SPI Control Register 1 (SPI1C1) 172
13.4.2 SPI Control Register 2 (SPI1C2) 173
13.4.3 SPI Baud Rate Register (SPI1BR) 174
13.4.4 SPI Status Register (SPI1S) 176
13.4.5 SPI Data Register (SPI1D) 177

Chapter 14
Analog Comparator (S08ACMPV1)

14.1 Features 180
14.2 Block Diagram 180
14.3 Pin Description 180
14.4 Functional Description 181
14.4.1 Interrupts 181
14.4.2 Wait Mode Operation 181
14.4.3 Stop Mode Operation 181
14.4.4 Background Mode Operation 181
14.5 ACMP Status and Control Register (ACMP1SC) 182

Chapter 15
Development Support

15.1 Introduction 183
15.1.1 Features 183
15.2 Background Debug Controller (BDC) 184
15.2.1 BKGD Pin Description 184
15.2.2 Communication Details 185
15.2.3 BDC Commands 189
15.2.4 BDC Hardware Breakpoint 191
15.3 On-Chip Debug System (DBG) 192
15.3.1 Comparators A and B 192
15.3.2 Bus Capture Information and FIFO Operation 192
15.3.3 Change-of-Flow Information 193
15.3.4 Tag vs. Force Breakpoints and Triggers 193
15.3.5 Trigger Modes 194
15.3.6 Hardware Breakpoints 196
15.4 Register Definition 196
15.4.1 BDC Registers and Control Bits 196
15.4.1.1 BDC Status and Control Register (BDCSCR) 197
15.4.1.2 BDC Breakpoint Match Register (BDCBKPT) 198
15.4.2 System Background Debug Force Reset Register (SBDFR) 198

Table 2-2. Signal Properties

Pin Name	Dir[1]	High Current Pin	Pullup[2]	Comments[3]
V_{DD}		—	—	
V_{SS}		—	—	
XTAL	O	—	—	Crystal oscillator output
EXTAL	I	—	—	Crystal oscillator input
IRO	O	Y	—	Infrared output
PTA0/KBI1P0	I	N	SWC	PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}.
PTA1/KBI1P1	I/O	N	SWC	
PTA2/KBI1P2	I/O	N	SWC	
PTA3/KBI1P3	I/O	N	SWC	
PTA4/KBI1P4	I/O	N	SWC	
PTA5/KBI1P5	I/O	N	SWC	
PTA6/KBI1P6	I/O	N	SWC	
PTA7/KBI1P7	I/O	N	SWC	
PTB0/TxD1	I/O	Y	SWC	
PTB1/RxD1	I/O	Y	SWC	
PTB2	I/O	Y	SWC	
PTB3	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB4	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB5	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB6	I/O	Y	SWC	Available only in 32-, 44-, and 48-pin packagess
PTB7/TPM1CH1	I/O	Y	SWC	
PTC0/KBI2P0	I/O	N	SWC	
PTC1/KBI2P1	I/O	N	SWC	
PTC2/KBI2P2	I/O	N	SWC	
PTC3/KBI2P3	I/O	N	SWC	
PTC4/MOSI1	I/O	N	SWC	
PTC5/MISO1	I/O	N	SWC	
PTC6/SPSCK1	I/O	N	SWC	
PTC7/$\overline{SS1}$	I/O	N	SWC	
PTD0/BKGD/MS	I/O	N	SWC[4]	Output-only when configured as PTD0 pin. Pullup enabled.
PTD1/$\overline{RESET}$	I/O	N	SWC[3]	Output-only when configured as PTD1 pin.

	7	6	5	4	3	2	1	0
R			KEYACC					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-7. FLASH Configuration Register (FCNFG)

Table 4-8. FCNFG Field Descriptions

Field	Description
5 KEYACC	**Enable Writing of Access Key** — This bit enables writing of the backdoor comparison key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, “Security." 0 Writes to $FFB0–$FFB7 are interpreted as the start of a FLASH programming or erase command. 1 Writes to NVBACKKEY ($FFB0–$FFB7) are interpreted as comparison key writes. Reads of the FLASH return invalid data.

4.6.4 FLASH Protection Register (FPROT and NVPROT)

During reset, the contents of the nonvolatile location NVPROT is copied from FLASH into FPROT. Bits 0, 1, and 2 are not used and each always reads as 0. This register may be read at any time, but user program writes have no meaning or effect. Background debug commands can write to FPROT at $1824.

	7	6	5	4	3	2	1	0
R	FPOPEN	FPDIS	FPS2	FPS1	FPS0	0	0	0
W	(1)	(1)	(1)	(1)	(1)			
Reset	This register is loaded from nonvolatile location NVPROT during reset.							

= Unimplemented or Reserved

Figure 4-8. FLASH Protection Register (FPROT)

1. Background commands can be used to change the contents of these bits in FPROT.

Table 4-9. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Open Unprotected FLASH for Program/Erase** 0 Entire FLASH memory is block protected (no program or erase allowed). 1 Any FLASH location, not otherwise block protected or secured, may be erased or programmed.
6 FPDIS	**FLASH Protection Disable** 0 FLASH block specified by FPS2:FPS0 is block protected (program and erase not allowed). 1 No FLASH block is protected.
5:3 FPS[2:0]	**FLASH Protect Size Selects** — When FPDIS = 0, this 3-bit field determines the size of a protected block of FLASH locations at the high address end of the FLASH (see Table 4-10 and Table 4-11). Protected FLASH locations cannot be erased or programmed.

The MC9S08RC/RD/RE/RG has these sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect
- Illegal address (16K and 8K devices only)
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register. Whenever the MCU enters reset, the reset pin is driven low for 34 internal bus cycles where the internal bus frequency is one-half the OSC frequency. After the 34 cycles are completed, the pin is released and will be pulled up by the internal pullup resistor, unless it is held low externally. After the pin is released, it is sampled after another 38 cycles to determine whether the reset pin is the cause of the MCU reset.

5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP timer periodically. If the application program gets lost and fails to reset the COP before it times out, a system reset is generated to force the system back to a known starting point. The COP watchdog is enabled by the COPE bit in SOPT (see Section 5.8.4, “System Options Register (SOPT),” for additional information). The COP timer is reset by writing any value to the address of SRS. This write does not affect the data in the read-only SRS. Instead, the act of writing to this address is decoded and sends a reset signal to the COP timer.

After any reset, the COP timer is enabled. This provides a reliable way to detect code that is not executing as intended. If the COP watchdog is not used in an application, it can be disabled by clearing the COPE bit in the write-once SOPT register. Also, the COPT bit can be used to choose one of two timeout periods (2^{18} or 2^{20} cycles of the bus rate clock). Even if the application will use the reset default settings in COPE and COPT, the user must write to write-once SOPT during reset initialization to lock in the settings. That way, they cannot be changed accidentally if the application program gets lost.

The write to SRS that services (clears) the COP timer must not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

When the MCU is in active background mode, the COP timer is temporarily disabled.

5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it was before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such

The space period provides an interpulse gap (no carrier). If CMTCMD3:CMTCMD4 = $0000, then the modulator and carrier generator will switch between carrier frequencies without a gap or any carrier glitches (zero space).

Using timing data for carrier burst and interpulse gap length calculated by the CPU, FSK mode can automatically generate a phase-coherent, dual-frequency FSK signal with programmable burst and interburst gaps.

The mark and space time equations for FSK mode are:

$$t_{mark} = (CMTCMD1:CMTCMD2 + 1) \div f_{CG} \quad \textit{Eqn. 8-7}$$

$$t_{space} = CMTCMD3:CMTCMD4 \div f_{CG} \quad \textit{Eqn. 8-8}$$

Where f_{CG} is the frequency output from the carrier generator. The example in Figure 8-6 shows what the IRO pin output looks like in FSK mode with the following values: CMTCMD1:CMTCMD2 = $0003, CMTCMD3:CMTCMD4 = $0002, primary carrier high count = $01, primary carrier low count = $02, secondary carrier high count = $03, and secondary carrier low count = $01.

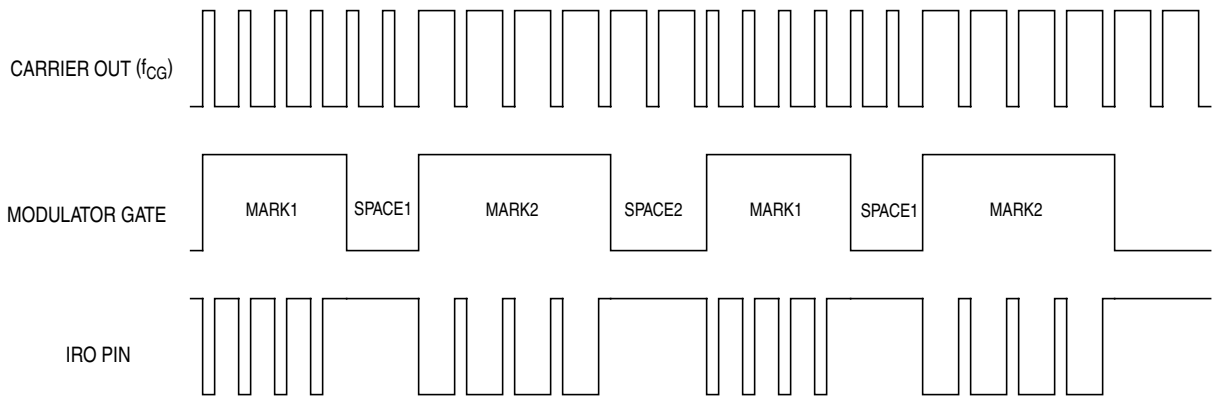


Figure 8-6. Example CMT Output in FSK Mode

8.5.3 Extended Space Operation

In time, baseband, or FSK mode, the space period can be made longer than the maximum possible value of the space period register. Setting the EXSPC bit in the CMTMSC register will force the modulator to treat the next modulation period (beginning with the next load of the counter and space period register) as a space period equal in length to the mark and space counts combined. Subsequent modulation periods will consist entirely of these extended space periods with no mark periods. Clearing EXSPC will return the modulator to standard operation at the beginning of the next modulation period.

8.5.3.1 EXSPC Operation in Time Mode

To calculate the length of an extended space in time or baseband modes, add the mark and space times and multiply by the number of modulation periods that EXSPC is set.

10.7.4 Timer Channel n Status and Control Register (TPM1CnSC)

TPM1CnSC contains the channel interrupt status flag and control bits that are used to configure the interrupt enable, channel configuration, and pin function.

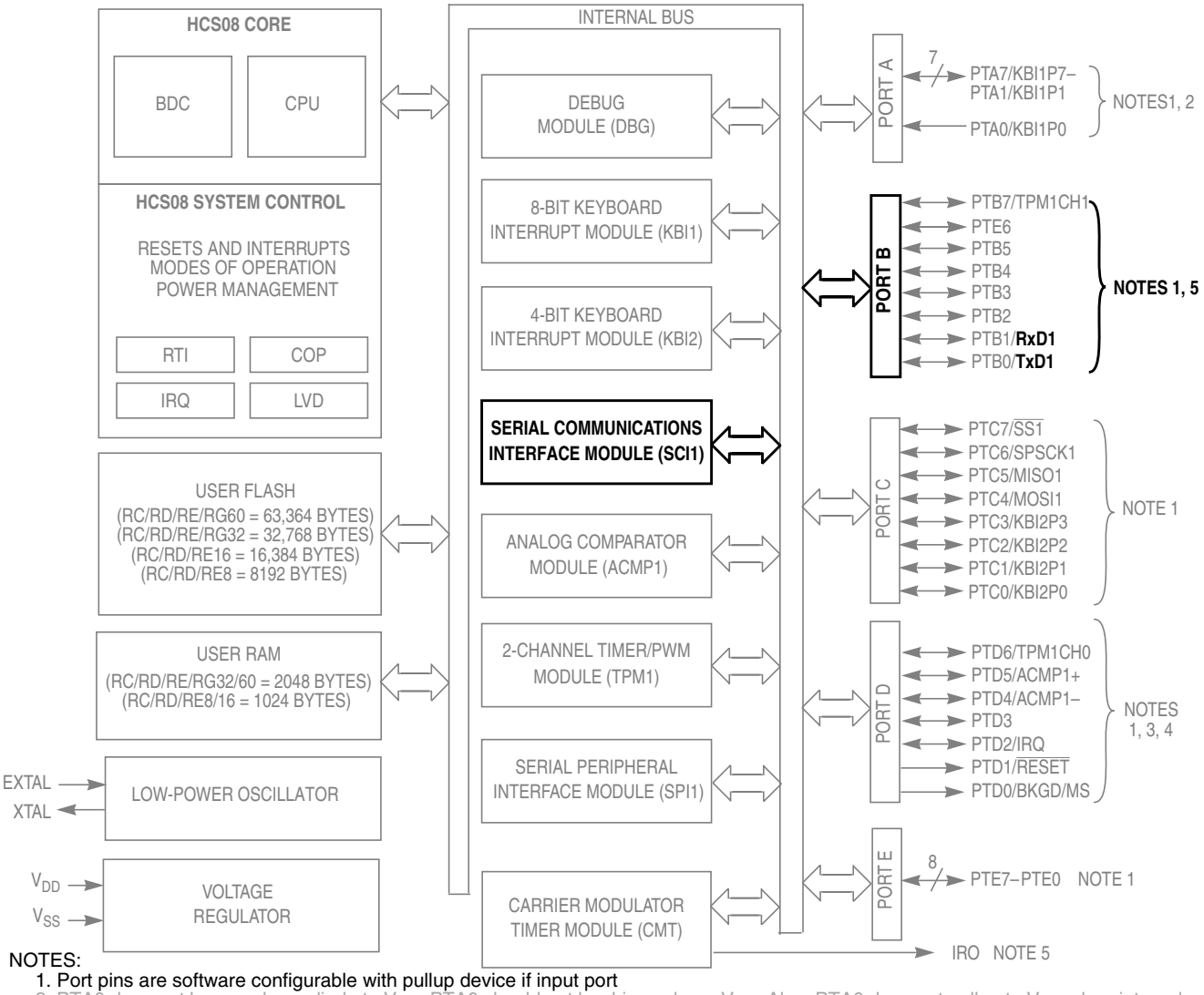
	7	6	5	4	3	2	1	0
R	CHnF	CHnIE	MSnB	MSnA	ELSnB	ELSnA	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-10. Timer Channel n Status and Control Register (TPM1CnSC)

Table 10-4. TPM1CnSC Register Field Descriptions

Field	Description
7 CHnF	**Channel n Flag** — When channel n is configured for input capture, this flag bit is set when an active edge occurs on the channel n pin. When channel n is an output compare or edge-aligned PWM channel, CHnF is set when the value in the TPM counter registers matches the value in the TPM channel n value registers. This flag is seldom used with center-aligned PWMs because it is set every time the counter matches the channel value register, which correspond to both edges of the active duty cycle period. A corresponding interrupt is requested when CHnF is set and interrupts are enabled (CHnIE = 1). Clear CHnF by reading TPM1CnSC while CHnF is set and then writing a 0 to CHnF. If another interrupt request occurs before the clearing sequence is complete, the sequence is reset so CHnF would remain set after the clear sequence was completed for the earlier CHnF. This is done so a CHnF interrupt request cannot be lost by clearing a previous CHnF. Reset clears CHnF. Writing a 1 to CHnF has no effect. 0 No input capture or output compare event occurred on channel n 1 Input capture or output compare event occurred on channel n
6 CHnIE	**Channel n Interrupt Enable** — This read/write bit enables interrupts from channel n. Reset clears CHnIE. 0 Channel n interrupt requests disabled (use software polling) 1 Channel n interrupt requests enabled
5 MSnB	**Mode Select B for TPM Channel n** — When CPWMS = 0, MSnB = 1 configures TPM channel n for edge-aligned PWM mode. For a summary of channel mode and setup controls, refer to Table 10-5.
4 MSnA	**Mode Select A for TPM Channel n** — When CPWMS = 0 and MSnB = 0, MSnA configures TPM channel n for input capture mode or output compare mode. Refer to Table 10-5 for a summary of channel mode and setup controls.
3:2 ELSn[B:A]	**Edge/Level Select Bits** — Depending on the operating mode for the timer channel as set by CPWMS:MSnB:MSnA and shown in Table 10-5, these bits select the polarity of the input edge that triggers an input capture event, select the level that will be driven in response to an output compare match, or select the polarity of the PWM output. Setting ELSnB:ELSnA to 0:0 configures the related timer pin as a general-purpose I/O pin unrelated to any timer channel functions. This function is typically used to temporarily disable an input capture channel or to make the timer pin available as a general-purpose I/O pin when the associated timer channel is set up as a software timer that does not require the use of a pin. This is also the setting required for channel 0 when the TPM1CH0 pin is used as an external clock input.



NOTES:
1. Port pins are software configurable with pullup device if input port
2. PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}. Also, PTA0 does not pullup to V_{DD} when internal pullup is enabled.
3. IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)
4. The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 11-1. MC9S08RC/RD/RE/RG Block Diagram Highlighting SCI Block and Pins

Figure 12-2 shows the receiver portion of the SCI.

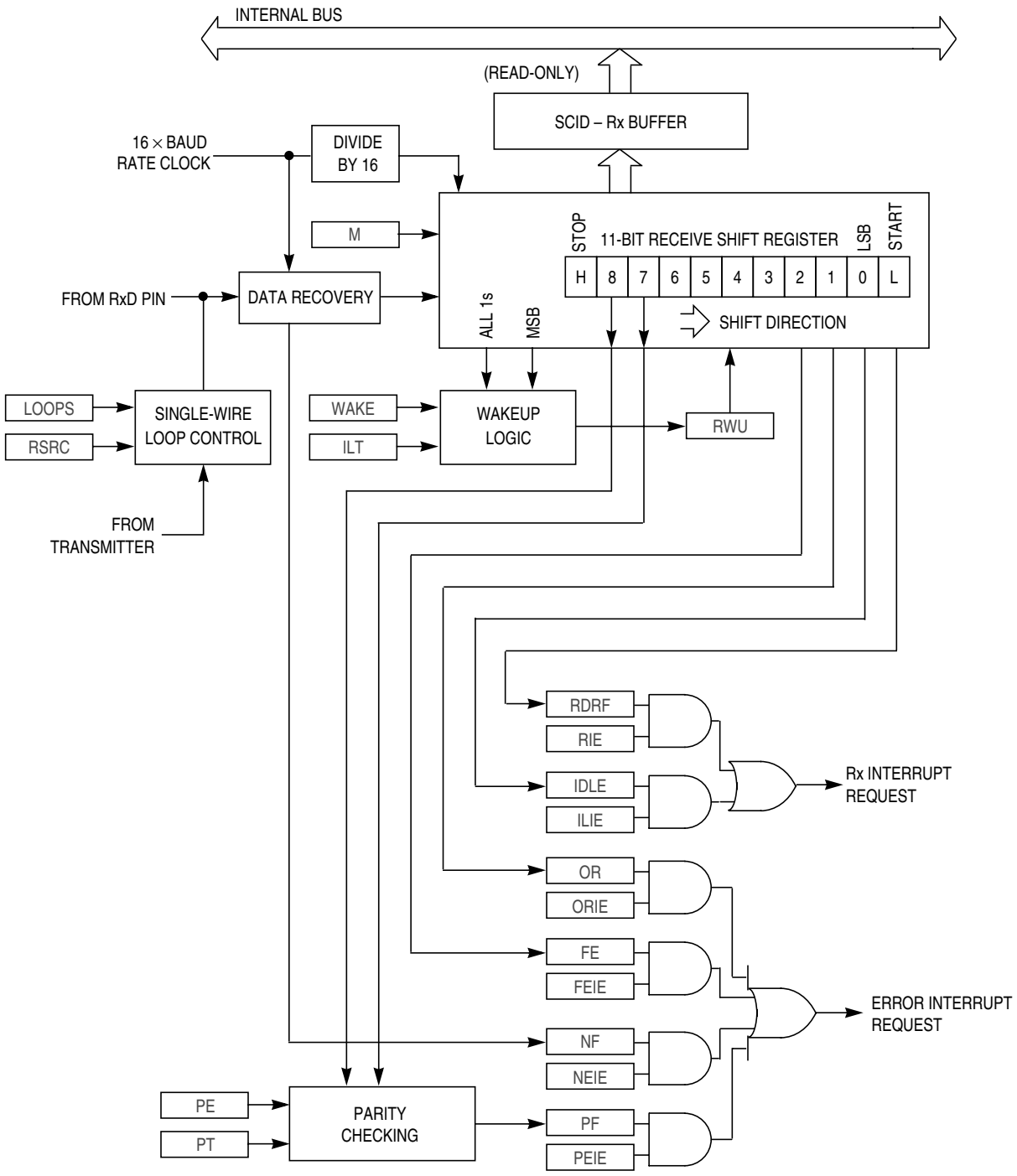


Figure 12-2. SCI Receiver Block Diagram

the transmit data register is transferred to the shift register (synchronized with the baud rate clock) and the transmit data register empty (TDRE) status flag is set to indicate another character may be written to the transmit data buffer at SCI1D.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD1 pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD1 high, waiting for more characters to transmit.

Writing 0 to TE does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity that is in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

12.3.2.1 Send Break and Queued Idle

The SBK control bit in SCI1C2 is used to send break characters which were originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0 (10 bit times including the start and stop bits). Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 1 and then write 0 to the SBK bit. This action queues a break character to be sent as soon as the shifter is available. If SBK is still 1 when the queued break moves into the shifter (synchronized to the baud rate clock), an additional break character is queued. If the receiving device is another Freescale Semiconductor SCI, the break characters will be received as 0s in all eight data bits and a framing error (FE = 1) occurs.

When idle-line wakeup is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the TE bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while TE = 0, the SCI transmitter never actually releases control of the TxD1 pin. If there is a possibility of the shifter finishing while TE = 0, set the general-purpose I/O controls so the pin that is shared with TxD1 is an output driving a logic 1. This ensures that the TxD1 line will look like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to TE.

12.3.3 Receiver Functional Description

In this section, the data sampling technique used to reconstruct receiver data is described in more detail; two variations of the receiver wakeup function are explained. (The receiver block diagram is shown in Figure 12-2.)

The receiver is enabled by setting the RE bit in SCI1C2. Character frames consist of a start bit of logic 0, eight (or nine) data bits (LSB first), and a stop bit of logic 1. For information about 9-bit data mode, refer to Section 12.3.5.1, “8- and 9-Bit Data Modes.” For the remainder of this discussion, we assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (RDRF) status flag is set. If RDRF was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program

Figure 15-2 shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target HCS08 MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target transmission period, there is no need to treat the line as an open-drain signal during this period.

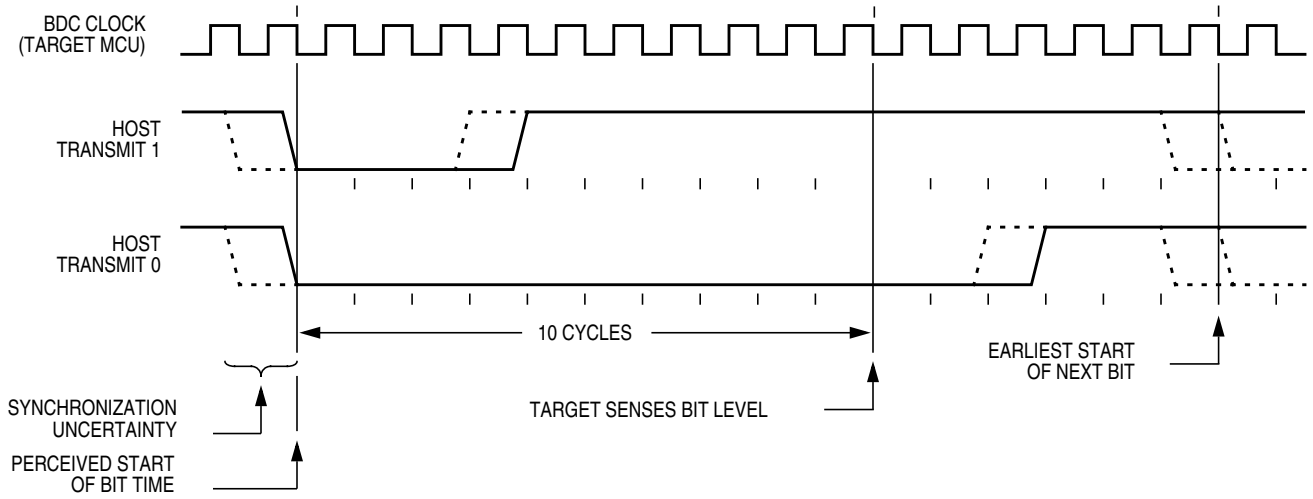


Figure 15-2. BDC Host-to-Target Serial Bit Timing

the host must perform ((8 – CNT) – 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Section 15.3.5, “Trigger Modes”), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

15.3.3 Change-of-Flow Information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

15.3.4 Tag vs. Force Breakpoints and Triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

A-Only — Trigger when the address matches the value in comparator A

A OR B — Trigger when the address matches either the value in comparator A or the value in comparator B

A Then B — Trigger when the address matches the value in comparator B but only after the address for another cycle matched the value in comparator A. There can be any number of cycles after the A match and before the B match.

A AND B Data (Full Mode) — This is called a full mode because address, data, and R/W (optionally) must match within the same bus cycle to cause a trigger event. Comparator A checks address, the low byte of comparator B checks data, and R/W is checked against RWA if RWAEN = 1. The high-order half of comparator B is not used.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

A AND NOT B Data (Full Mode) — Address must match comparator A, data must not match the low half of comparator B, and R/W must match RWA if RWAEN = 1. All three conditions must be met within the same bus cycle to cause a trigger.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

Event-Only B (Store Data) — Trigger events occur each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

A Then Event-Only B (Store Data) — After the address has matched the value in comparator A, a trigger event occurs each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

Inside Range (A ≤ Address ≤ B) — A trigger occurs when the address is greater than or equal to the value in comparator A and less than or equal to the value in comparator B at the same time.

Outside Range (Address < A or Address > B) — A trigger occurs when the address is either less than the value in comparator A or greater than the value in comparator B.

A.6 Supply Current Characteristics

Table A-6. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)[1]	Typical[2]	Max	Temp. (°C)
Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	3	500 µA	1.525 mA 1.525 mA	70 85
		2	450 µA	1.475 mA 1.475 mA	70 85
Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	3	3.8 mA	4.8 mA 4.8 mA	70 85
		2	2.6 mA	3.6 mA 3.6 mA	70 85
Stop1 mode supply current	$S1I_{DD}$	3	100 nA	350 nA 736 nA	70 85
		2	100 nA	150 nA 450 nA	70 85
Stop2 mode supply current	$S2I_{DD}$	3	500 nA	1.20 µA 1.90 µA	70 85
		2	500 nA	1.00 µA 1.70 µA	70 85
Stop3 mode supply current	$S3I_{DD}$	3	600 nA	2.65 µA 4.65 µA	70 85
		2	500 nA	2.30 µA 4.30 µA	70 85
RTI adder from stop2 or stop3		3	300 nA		
		2	300 nA		
Adder for LVD reset enabled in stop3		3	70 µA		
		2	60 µA		

1. 3 V values are 100% tested; 2 V values are characterized but not tested.
2. Typicals are measured at 25°C.
3. Does not include any dc loads on port pins

A.7 Analog Comparator (ACMP) Electricals

Table A-7. ACMP Electrical Specifications (Temp Range = -40 to 85° C Ambient)

Characteristic	Symbol	Min	Typical	Max	Unit
Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V
Analog input offset voltage	VAIO		—	40	mV
Analog Comparator initialization delay	t_{AINIT}		—	1	µs
Analog Comparator bandgap reference voltage	V_{BG}	1.208	1.218	1.228	V

2. When any reset is initiated, internal circuitry drives the reset pin low for about 34 cycles of f_{Bus} and then samples the level on the reset pin about 38 cycles later to distinguish external reset requests from internal requests.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

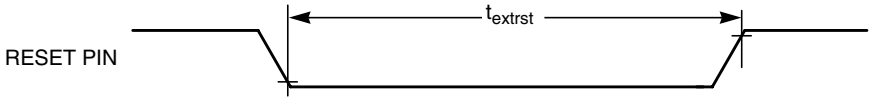


Figure A-6. Reset Timing

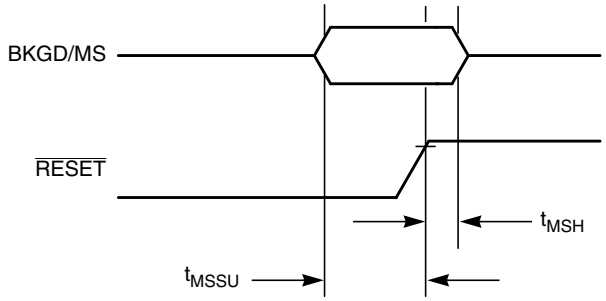


Figure A-7. Active Background Debug Mode Latch Timing

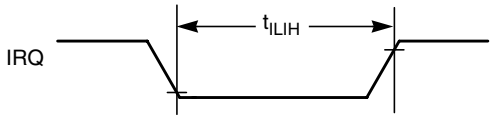


Figure A-8. IRQ Timing

A.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

freescale semiconductor
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.
ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

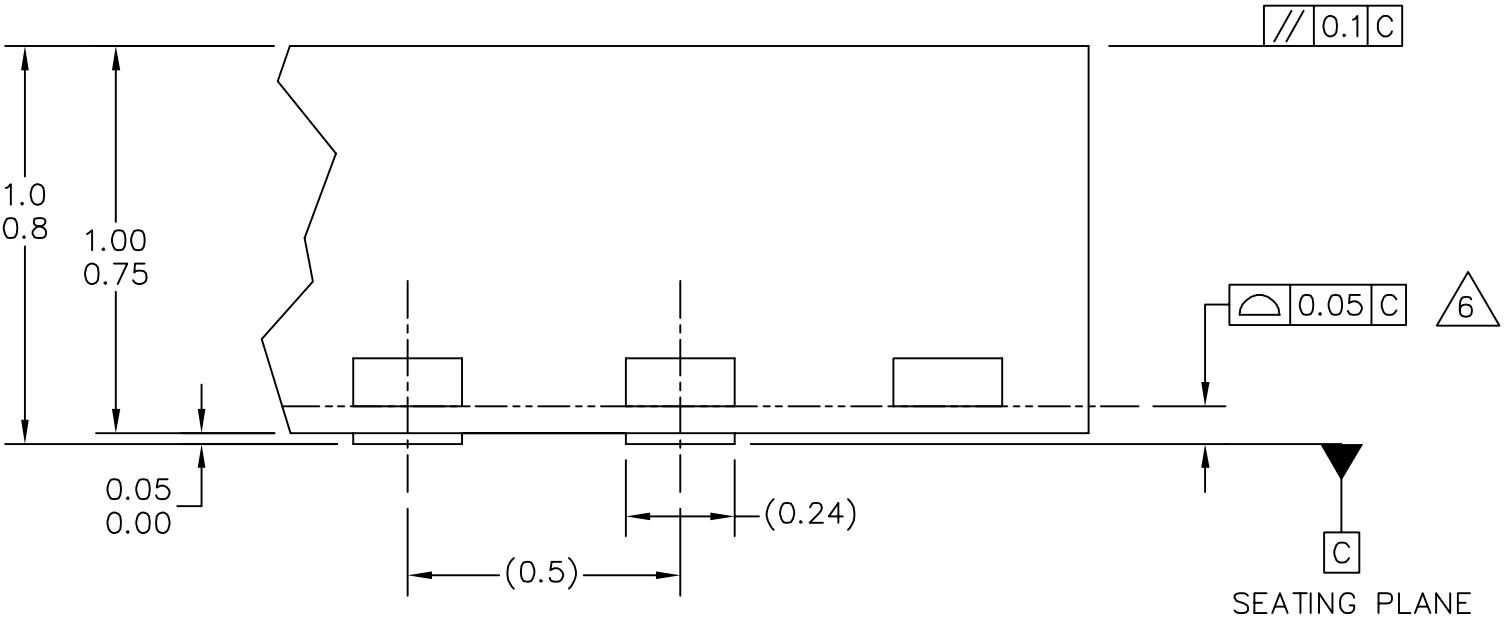
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

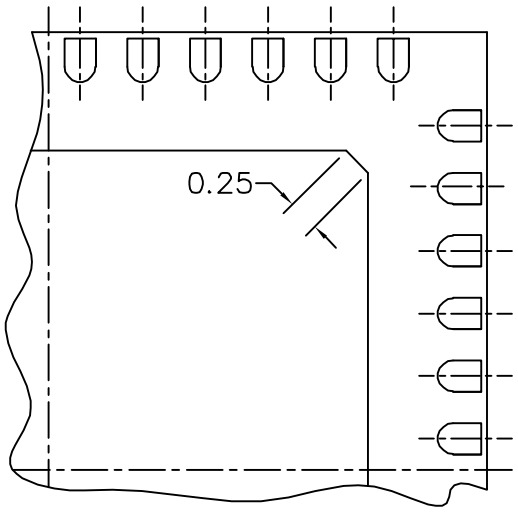
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

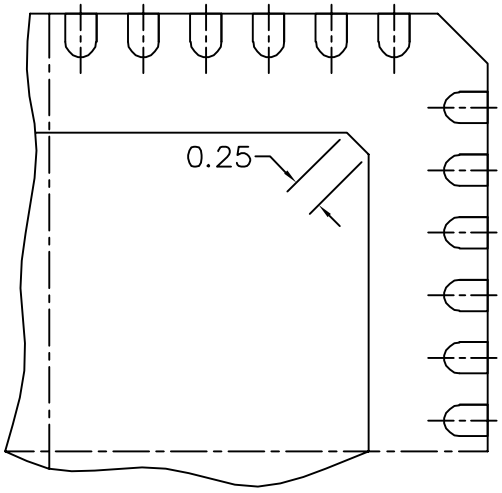
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.
ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.



DETAIL G
VIEW ROTATED 90° CW



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION1

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)

CASE NUMBER: 1314-03
STANDARD: JEDEC-MO-220 VKKD-2
PACKAGE CODE: 6152