



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08rd8pe

Section Number	Title	Page
7.3.4	Direct Addressing Mode (DIR)	91
7.3.5	Extended Addressing Mode (EXT)	91
7.3.6	Indexed Addressing Mode	91
7.3.6.1	Indexed, No Offset (IX)	92
7.3.6.2	Indexed, No Offset with Post Increment (IX+)	92
7.3.6.3	Indexed, 8-Bit Offset (IX1)	92
7.3.6.4	Indexed, 8-Bit Offset with Post Increment (IX1+)	92
7.3.6.5	Indexed, 16-Bit Offset (IX2)	92
7.3.6.6	SP-Relative, 8-Bit Offset (SP1)	92
7.3.6.7	SP-Relative, 16-Bit Offset (SP2)	92
7.4	Special Operations	92
7.4.1	Reset Sequence	93
7.4.2	Interrupt Sequence	93
7.4.3	Wait Mode Operation	94
7.4.4	Stop Mode Operation	94
7.4.5	BGND Instruction	94
7.5	HCS08 Instruction Set Summary	95

Chapter 8

Carrier Modulator Timer (S08CMTV1)

8.1	Introduction	107
8.2	Features	108
8.3	CMT Block Diagram	108
8.4	Pin Description	108
8.5	Functional Description	109
8.5.1	Carrier Generator	110
8.5.2	Modulator	112
8.5.2.1	Time Mode	113
8.5.2.2	Baseband Mode	114
8.5.2.3	FSK Mode	114
8.5.3	Extended Space Operation	115
8.5.3.1	EXSPC Operation in Time Mode	115
8.5.3.2	EXSPC Operation in FSK Mode	116
8.5.4	Transmitter	116
8.5.5	CMT Interrupts	117
8.5.6	Wait Mode Operation	117
8.5.7	Stop Mode Operation	117
8.5.8	Background Mode Operation	118
8.6	CMT Registers and Control Bits	118
8.6.1	Carrier Generator Data Registers (CMTCGH1, CMTCGL1, CMTCGH2, and CMTCGL2)	118
8.6.2	CMT Output Control Register (CMTOC)	120
8.6.3	CMT Modulator Status and Control Register (CMTMSC)	121
8.6.4	CMT Modulator Data Registers (CMTCMD1, CMTCMD2, CMTCMD3, and CMTCMD4)	122

3.6.4 Active BDM Enabled in Stop Mode

Entry into the active background mode from run mode is enabled if the ENBDM bit in BDCSCR is set. This register is described in the Development Support chapter of this data sheet. If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode so background debug communication is still possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation. The MCU cannot enter either stop1 mode or stop2 mode if ENBDM is set.

Most background commands are not available in stop mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from stop and enter active background mode if the ENBDM bit is set. After active background mode is entered, all background commands are available. Table 3-2 summarizes the behavior of the MCU in stop when entry into the active background mode is enabled.

Table 3-2. BDM Enabled Stop Mode Behavior

Mode	PDC	PPDC	CPU, Digital Peripherals, FLASH	RAM	OSC	ACMP	Regulator	I/O Pins	RTI
Stop3	Don't care	Don't care	Standby	Standby	On	Standby	On	States held	Optionally on

3.6.5 LVD Reset Enabled

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD reset is enabled in stop by setting the LVDRE bit in SPMSC1 when the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode. If the user attempts to enter either stop1 or stop2 with the LVD reset enabled (LVDRE = 1) the MCU will instead enter stop3. Table 3-3 summarizes the behavior of the MCU in stop when LVD reset is enabled.

Table 3-3. LVD Enabled Stop Mode Behavior

Mode	PDC	PPDC	CPU, Digital Peripherals, FLASH	RAM	OSC	ACMP	Regulator	I/O Pins	RTI
Stop3	Don't care	Don't care	Standby	Standby	On	Standby	On	States held	Optionally on

3.6.6 On-Chip Peripheral Modules in Stop Mode

When the MCU enters any stop mode, system clocks to the internal peripheral modules are stopped. Even in the exception case (ENBDM = 1), where clocks are kept alive to the background debug logic, clocks to the peripheral systems are halted to reduce power consumption.

Chapter 4 Memory

4.1 MC9S08RC/RD/RE/RG Memory Map

As shown in Figure 4-1, on-chip memory in the MC9S08RC/RD/RE/RG series of MCUs consists of RAM, FLASH program memory for nonvolatile data storage, and I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers (\$0000 through \$0045 for 32K and 60K parts, and \$0000 through \$003F for 16K and 8K parts)
- High-page registers (\$1800 through \$182B)
- Nonvolatile registers (\$FFB0 through \$FFBF)

- Writing to a FLASH address before the internal FLASH clock frequency has been set by writing to the FCDIV register
- Writing to a FLASH address while FCBEF is not set (A new command cannot be started until the command buffer is empty.)
- Writing a second time to a FLASH address before launching the previous command (There is only one write to FLASH for every command.)
- Writing a second time to FCMD before launching the previous command (There is only one write to FCMD for every command.)
- Writing to any FLASH control register other than FCMD after writing to a FLASH address
- Writing any command code other than the five allowed codes (\$05, \$20, \$25, \$40, or \$41) to FCMD
- Accessing (read or write) any FLASH control register other than the write to FSTAT (to clear FCBEF and launch the command) after writing the command to FCMD
- The MCU enters stop mode while a program or erase command is in progress (The command is aborted.)
- Writing the byte program, burst program, or page erase command code (\$20, \$25, or \$40) with a background debug command while the MCU is secured (The background debug controller can only do blank check and mass erase commands when the MCU is secure.)
- Writing 0 to FCBEF to cancel a partial command

4.4.6 FLASH Block Protection

Block protection prevents program or erase changes for FLASH memory locations in a designated address range. Mass erase is disabled when any block of FLASH is protected. The MC9S08RC/RD/RE/RG allows a block of memory at the end of FLASH, and/or the entire FLASH memory to be block protected. A disable control bit and a 3-bit control field, for each of the blocks, allows the user to independently set the size of these blocks. A separate control bit allows block protection of the entire FLASH memory array. All seven of these control bits are located in the FPROT register (see Section 4.6.4, “FLASH Protection Register (FPROT and NVPROT)”).

At reset, the high-page register (FPROT) is loaded with the contents of the NVPROT location that is in the nonvolatile register block of the FLASH memory. The value in FPROT cannot be changed directly from application software so a runaway program cannot alter the block protection settings. If the last 512 bytes of FLASH (which includes the NVPROT register) is protected, the application program cannot alter the block protection settings (intentionally or unintentionally). The FPROT control bits can be written by background debug commands to allow a way to erase a protected FLASH memory.

One use for block protection is to block protect an area of FLASH memory for a bootloader program. This bootloader program then can be used to erase the rest of the FLASH memory and reprogram it. Because the bootloader is protected, it remains intact even if MCU power is lost during an erase and reprogram operation.

2. Writing the user-entered key values to the NVBACKKEY through NVBACKKEY+7 locations. These writes must be done in order starting with the value for NVBACKKEY and ending with NVBACKKEY+7. STHX must not be used for these writes because these writes cannot be done on adjacent bus cycles. User software normally would get the key codes from outside the MCU system through a communication interface such as a serial I/O.
3. Writing 0 to KEYACC in the FCNFG register. If the 8-byte key that was just written matches the key stored in the FLASH locations, SEC01:SEC00 are automatically changed to 1:0 and security will be disengaged until the next reset.

The security key can be written only from RAM, so it cannot be entered through background commands without the cooperation of a secure user program. The FLASH memory cannot be accessed by read operations while KEYACC is set.

The backdoor comparison key (NVBACKKEY through NVBACKKEY+7) is located in FLASH memory locations in the nonvolatile register space so users can program these locations exactly as they would program any other FLASH memory location. The nonvolatile registers are in the same 512-byte block of FLASH as the reset and interrupt vectors, so block protecting that space also block protects the backdoor comparison key. Block protects cannot be changed from user application programs, so if the vector space is block protected, the backdoor security key mechanism cannot permanently change the block protect, security settings, or the backdoor key.

Security can always be disengaged through the background debug interface by performing these steps:

1. Disable any block protections by writing FPROT. FPROT can be written only with background debug commands, not from application software.
2. Mass erase FLASH if necessary.
3. Blank check FLASH. Provided FLASH is completely erased, security is disengaged until the next reset.

To avoid returning to secure mode after the next reset, program NVOPT so SEC01:SEC00 = 1:0.

4.6 FLASH Registers and Control Bits

The FLASH module has nine 8-bit registers in the high-page register space, three locations in the nonvolatile register space in FLASH memory that are copied into three corresponding high-page control registers at reset. There is also an 8-byte comparison key in FLASH memory. Refer to Table 4-2 and Table 4-3 for the absolute address assignments for all FLASH registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

4.6.1 FLASH Clock Divider Register (FCDIV)

Bit 7 of this register is a read-only status flag. Bits 6 through 0 may be read at any time but can be written only one time. Before any erase or programming operations are possible, write to this register to set the frequency of the clock for the nonvolatile memory system within acceptable limits.

4.6.5 FLASH Status Register (FSTAT)

Bits 3, 1, and 0 always read 0 and writes have no meaning or effect. The remaining five bits are status bits that can be read at any time. Writes to these bits have special meanings that are discussed in the bit descriptions.

	7	6	5	4	3	2	1	0
R	FCBEF	FCCF	FPVIOL	FACCERR	0	FBLANK	0	0
W								
Reset	1	1	0	0	0	0	0	0


 = Unimplemented or Reserved

Figure 4-9. FLASH Status Register (FSTAT)

Table 4-12. FSTAT Field Descriptions

Field	Description
7 FCBEF	FLASH Command Buffer Empty Flag — The FCBEF bit is used to launch commands. It also indicates that the command buffer is empty so that a new command sequence can be executed when performing burst programming. The FCBEF bit is cleared by writing a 1 to it or when a burst program command is transferred to the array for programming. Only burst program commands can be buffered. 0 Command buffer is full (not ready for additional commands). 1 A new burst program command may be written to the command buffer.
6 FCCF	FLASH Command Complete Flag — FCCF is set automatically when the command buffer is empty and no command is being processed. FCCF is cleared automatically when a new command is started (by writing 1 to FCBEF to register a command). Writing to FCCF has no meaning or effect. 0 Command in progress 1 All commands complete
5 FPVIOL	Protection Violation Flag — FPVIOL is set automatically when FCBEF is cleared to register a command that attempts to erase or program a location in a protected block (the erroneous command is ignored). FPVIOL is cleared by writing a 1 to FPVIOL. 0 No protection violation. 1 An attempt was made to erase or program a protected location.
4 FACCERR	Access Error Flag — FACCERR is set automatically when the proper command sequence is not followed exactly (the erroneous command is ignored), if a program or erase operation is attempted before the FCDIV register has been initialized, or if the MCU enters stop while a command was in progress. For a more detailed discussion of the exact actions that are considered access errors, see Section 4.4.5, "Access Errors." FACCERR is cleared by writing a 1 to FACCERR. Writing a 0 to FACCERR has no meaning or effect. 0 No access error. 1 An access error has occurred.
2 FBLANK	FLASH Verified as All Blank (erased) Flag — FBLANK is set automatically at the conclusion of a blank check command if the entire FLASH array was verified to be erased. FBLANK is cleared by clearing FCBEF to write a new valid command. Writing to FBLANK has no meaning or effect. 0 After a blank check command is completed and FCCF = 1, FBLANK = 0 indicates the FLASH array is not completely erased. 1 After a blank check command is completed and FCCF = 1, FBLANK = 1 indicates the FLASH array is completely erased (all \$FF).

4.6.6 FLASH Command Register (FCMD)

Only four command codes are recognized in normal user modes as shown in Table 4-14. Refer to Section 4.4.3, “Program and Erase Command Execution,” for a detailed discussion of FLASH programming and erase operations.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	FCMD7	FCMD6	FCMD5	FCMD4	FCMD3	FCMD2	FCMD1	FCMD0
Reset	0	0	0	0	0	0	0	0

Figure 4-10. FLASH Command Register (FCMD)

Table 4-13. FCMD Field Descriptions

Field	Description
7:0 FCMD[7:0]	See Table 4-14 for FLASH commands.

Table 4-14. FLASH Commands

Command	FCMD	Equate File Label
Blank check	\$05	mBlank
Byte program	\$20	mByteProg
Byte program – burst mode	\$25	mBurstProg
Page erase (512 bytes/page)	\$40	mPageErase
Mass erase (all FLASH)	\$41	mMassErase

All other command codes are illegal and generate an access error.

It is not necessary to perform a blank check command after a mass erase operation. Only blank check is required as part of the security unlocking mechanism.

The MC9S08RC/RD/RE/RG has these sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect
- Illegal address (16K and 8K devices only)
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register. Whenever the MCU enters reset, the reset pin is driven low for 34 internal bus cycles where the internal bus frequency is one-half the OSC frequency. After the 34 cycles are completed, the pin is released and will be pulled up by the internal pullup resistor, unless it is held low externally. After the pin is released, it is sampled after another 38 cycles to determine whether the reset pin is the cause of the MCU reset.

5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP timer periodically. If the application program gets lost and fails to reset the COP before it times out, a system reset is generated to force the system back to a known starting point. The COP watchdog is enabled by the COPE bit in SOPT (see Section 5.8.4, “System Options Register (SOPT),” for additional information). The COP timer is reset by writing any value to the address of SRS. This write does not affect the data in the read-only SRS. Instead, the act of writing to this address is decoded and sends a reset signal to the COP timer.

After any reset, the COP timer is enabled. This provides a reliable way to detect code that is not executing as intended. If the COP watchdog is not used in an application, it can be disabled by clearing the COPE bit in the write-once SOPT register. Also, the COPT bit can be used to choose one of two timeout periods (2^{18} or 2^{20} cycles of the bus rate clock). Even if the application will use the reset default settings in COPE and COPT, the user must write to write-once SOPT during reset initialization to lock in the settings. That way, they cannot be changed accidentally if the application program gets lost.

The write to SRS that services (clears) the COP timer must not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

When the MCU is in active background mode, the COP timer is temporarily disabled.

5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it was before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such

Table 5-1. Vector Summary

Vector Priority	Vector Number	Address (High/Low)	Vector Name	Module	Source	Enable	Description
<div>Lower</div> <div>↑</div> <div>↓</div> <div>Higher</div>	16 through 31	\$FFC0/FFC1 through \$FFDE/FFDF	Unused Vector Space (available for user program)				
	15	\$FFE0/FFE1	Vspi1	SPI ⁽¹⁾	SPIF MODF SPTEF	SPIE SPIE SPTIE	SPI
	14	\$FFE2/FFE3	Vrti	System control	RTIF	RTIE	Real-time interrupt
	13	\$FFE4/FFE5	Vkeyboard2	KBI2	KBF	KBIE	Keyboard 2 pins
	12	\$FFE6/FFE7	Vkeyboard1	KBI1	KBF	KBIE	Keyboard 1 pins
	11	\$FFE8/FFE9	Vacmp1	ACMP ⁽²⁾	ACF	ACIE	ACMP compare
	10	\$FFEA/FFEB	Vcmt	CMT	EOCF	EOCIE	CMT
	9	\$FFEC/FFED	Vsci1tx	SCI ⁽³⁾	TDRE TC	TIE TCIE	SCI transmit
	8	\$FFEE/FFEF	Vsci1rx	SCI ⁽³⁾	IDLE RDRF	ILIE RIE	SCI receive
	7	\$FFF0/FFF1	Vsci1err	SCI ⁽³⁾	OR NF FE PF	ORIE NFIE FEIE PFIE	SCI error
	6	\$FFF2/FFF3	Vtpm1ovf	TPM	TOF	TOIE	TPM overflow
	5	\$FFF4/FFF5	Vtpm1ch1	TPM	CH1F	CH1IE	TPM channel 1
	4	\$FFF6/FFF7	Vtpm1ch0	TPM	CH0F	CH0IE	TPM channel 0
	3	\$FFF8/FFF9	Virq	IRQ	IRQF	IRQIE	IRQ pin
	2	\$FFFA/FFFB	Vlvd	System control	LVDF	LVDIE	Low-voltage detect
	1	\$FFFC/FFFD	Vswi	Core	SWI Instruction	—	Software interrupt
	0	\$FFFE/FFFF	Vreset	System control	COP LVD RESET pin Illegal opcode Illegal address	COPE LVDRE RSTPE — —	Watchdog timer Low-voltage detect External pin Illegal opcode Illegal address

1. The SPI module is not included on the MC9S08RC/RD/RE devices. This vector location is unused for those devices.
2. The analog comparator (ACMP) module is not included on the MC9S08RD devices. This vector location is unused for those devices.
3. The SCI module is not included on the MC9S08RC devices. This vector location is unused for those devices.

5.6 Low-Voltage Detect (LVD) System

The MC9S08RC/RD/RE/RG includes a system to protect against low-voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit, an LVD circuit with flag bits for warning and detection, and a mechanism for entering a system safe state following an LVD interrupt. The LVD circuit can be configured to generate an interrupt or a reset when low supply voltage has been detected.

6.6.3 Port C Registers (PTCD, PTCPE, and PTCDD)

Port C pins used as general-purpose I/O pins are controlled by the port C data (PTCD), data direction (PTCDD), and pullup enable (PTCPE) registers.

	7	6	5	4	3	2	1	0
R								
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-12. Port C Data Register (PTCD)

Table 6-7. PTCD Field Descriptions

Field	Description
7:0 PTCD[7:0]	Port C Data Register Bits — For port C pins that are inputs, reads return the logic level on the pin. For port C pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTCD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

	7	6	5	4	3	2	1	0
R								
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-13. Pullup Enable for Port C (PTCPE)

Table 6-8. PTCPE Field Descriptions

Field	Description
7:0 PTCPE[7:0]	Pullup Enable for Port C Bits — For port C pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled. For port C pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled. 0 Internal pullup device disabled. 1 Internal pullup device enabled.

Table 7-1. CCR Register Field Descriptions

Field	Description
7 V	Two's Complement Overflow Flag — The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag. 0 No overflow 1 Overflow
4 H	Half-Carry Flag — The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C condition code bits to automatically add a correction value to the result from a previous ADD or ADC on BCD operands to correct the result to a valid BCD value. 0 No carry between bits 3 and 4 1 Carry between bits 3 and 4
3 I	Interrupt Mask Bit — When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the first instruction of the interrupt service routine is executed. Interrupts are not recognized at the instruction boundary after any instruction that clears I (CLI or TAP). This ensures that the next instruction after a CLI or TAP will always be executed without the possibility of an intervening interrupt, provided I was set. 0 Interrupts enabled 1 Interrupts disabled
2 N	Negative Flag — The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result. Simply loading or storing an 8-bit or 16-bit value causes N to be set if the most significant bit of the loaded or stored value was 1. 0 Non-negative result 1 Negative result
1 Z	Zero Flag — The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of 0x00 or 0x0000. Simply loading or storing an 8-bit or 16-bit value causes Z to be set if the loaded or stored value was all 0s. 0 Non-zero result 1 Zero result
0 C	Carry/Borrow Flag — The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag. 0 No carry out of bit 7 1 Carry out of bit 7

7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location



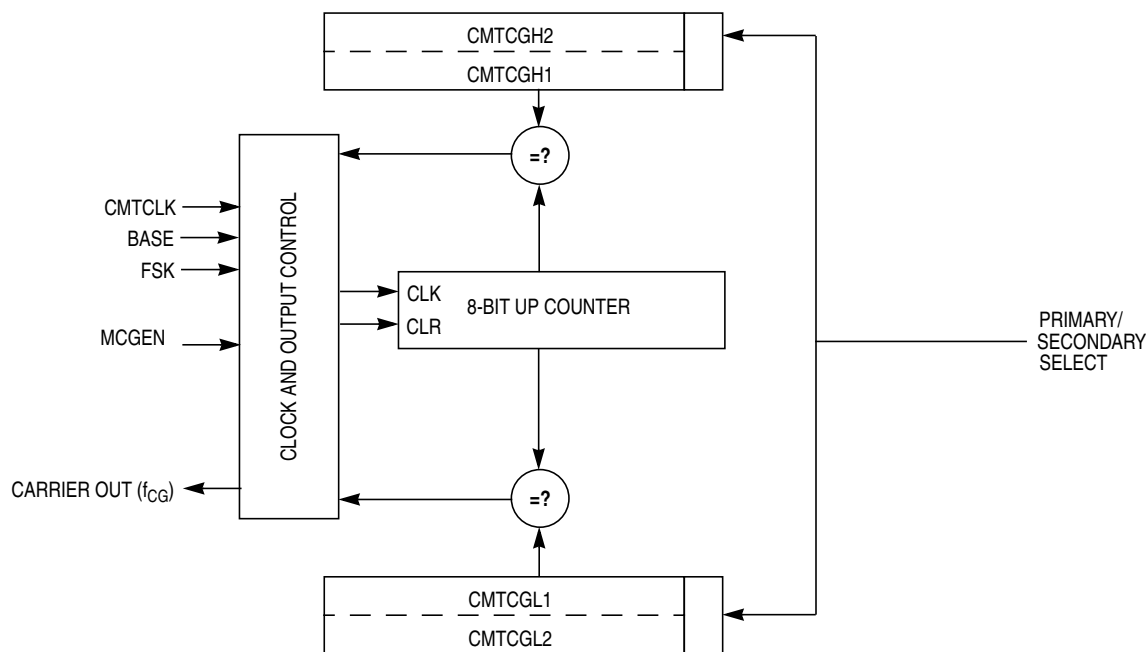


Figure 8-3. Carrier Generator Block Diagram

The high/low time counter is an 8-bit up counter. After each increment, the contents of the counter are compared with the appropriate high or low count value register. When the compare value is reached, the counter is reset to a value of \$01, and the compare is redirected to the other count value register.

Assuming that the high time count compare register is currently active, a valid compare will cause the carrier output to be driven low. The counter will continue to increment (starting at reset value of \$01). When the value stored in the selected low count value register is reached, the counter will again be reset and the carrier output will be driven high.

The cycle repeats, automatically generating a periodic signal that is directed to the modulator. The lowest frequency (maximum period) and highest frequency (minimum period) that can be generated are defined as:

$$f_{\max} = f_{\text{CMTCLK}} \div (2 \times 1) \text{ Hz} \quad \text{Eqn. 8-1}$$

$$f_{\min} = f_{\text{CMTCLK}} \div (2 \times (2^8 - 1)) \text{ Hz} \quad \text{Eqn. 8-2}$$

In the general case, the carrier generator output frequency is:

$$f_{\text{CG}} = f_{\text{CMTCLK}} \div (\text{Highcount} + \text{Lowcount}) \text{ Hz} \quad \text{Eqn. 8-3}$$

Where: $0 < \text{Highcount} < 256$ and
 $0 < \text{Lowcount} < 256$

Chapter 10

Timer/PWM Module (S08TPMV1)

10.1 Introduction

The MC9S08RC/RD/RE/RG includes a timer/PWM (TPM) module that supports traditional input capture, output compare, or buffered edge-aligned pulse-width modulation (PWM) on each channel. A control bit in the TPM configures both channels in the timer to operate as center-aligned PWM functions. Timing functions in the TPM are based on a 16-bit counter with prescaler and modulo features to control frequency and range (period between overflows) of the time reference. This timing system is ideally suited for a wide range of control applications. The MC9S08RC/RD/RE/RG devices do not have a separate fixed internal clock source (XCLK). If the XCLK source is selected using the CLKSA and CLKSB control bits (see Table 10-2), the TPM will use the BUSCLK.

10.2 Features

Timer system features include:

- Two separate channels:
 - Each channel may be input capture, output compare, or buffered edge-aligned PWM
 - Rising-edge, falling-edge, or any-edge input capture trigger
 - Set, clear, or toggle output compare action
 - Selectable polarity on PWM outputs
- The TPM may be configured for buffered, center-aligned pulse-width modulation (CPWM) on both channels
- Clock source to prescaler for the TPM is selectable between the bus clock or an external pin:
 - Prescale taps for divide by 1, 2, 4, 8, 16, 32, 64, or 128
 - External clock input shared with TPM1CH0 timer channel pin
- 16-bit modulus register to control counter range
- Timer system enable
- One interrupt per channel plus terminal count interrupt

Because the HCS08 MCU is an 8-bit architecture, a coherency mechanism is built into the timer counter for read operations. Whenever either byte of the counter is read (TPM1CNTH or TPM1CNTL), both bytes are captured into a buffer so when the other byte is read, the value will represent the other byte of the count at the time the first byte was read. The counter continues to count normally, but no new value can be read from either byte until both bytes of the old count have been read.

The main timer counter can be reset manually at any time by writing any value to either byte of the timer count TPM1CNTH or TPM1CNTL. Resetting the counter in this manner also resets the coherency mechanism in case only one byte of the counter was read before resetting the count.

10.5.2 Channel Mode Selection

Provided CPWMS = 0 (center-aligned PWM operation is not specified), the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and buffered edge-aligned PWM.

10.5.2.1 Input Capture Mode

With the input capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TPM latches the contents of the TPM counter into the channel value registers (TPM1CnVH:TPM1CnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

When either byte of the 16-bit capture register is read, both bytes are latched into a buffer to support coherent 16-bit accesses regardless of order. The coherency sequence can be manually reset by writing to the channel status/control register (TPM1CnSC).

An input capture event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.2 Output Compare Mode

With the output compare function, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter reaches the value in the channel value registers of an output compare channel, the TPM can set, clear, or toggle the channel pin.

In output compare mode, values are transferred to the corresponding timer channel value registers only after both 8-bit bytes of a 16-bit register have been written. This coherency sequence can be manually reset by writing to the channel status/control register (TPM1CnSC).

An output compare event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

10.5.2.3 Edge-Aligned PWM Mode

This type of PWM output uses the normal up-counting mode of the timer counter (CPWMS = 0) and can be used when other channels in the same TPM are configured for input capture or output compare functions. The period of this PWM signal is determined by the setting in the modulus register (TPM1MODH:TPM1MODL). The duty cycle is determined by the setting in the timer channel value

Table 10-2. TPM Clock Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
0:0	No clock selected (TPM disabled)
0:1	Bus rate clock (BUSCLK)
1:0	Fixed system clock (XCLK)
1:1	External source (TPM1 Ext Clk) ^{1,2}

1. The maximum frequency that is allowed as an external clock is one-fourth of the bus frequency.
2. When the TPM1CH0 pin is selected as the TPM clock source, the corresponding ELS0B:ELS0A control bits should be set to 0:0 so channel 0 does not try to use the same pin for a conflicting function.

Table 10-3. Prescale Divisor Selection

PS2:PS1:PS0	TPM Clock Source Divided-By
0:0:0	1
0:0:1	2
0:1:0	4
0:1:1	8
1:0:0	16
1:0:1	32
1:1:0	64
1:1:1	128

10.7.2 Timer Counter Registers (TPM1CNTH:TPM1CNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPM1CNTH or TPM1CNTL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This allows coherent 16-bit reads in either order. The coherency mechanism is automatically restarted by an MCU reset, a write of any value to TPM1CNTH or TPM1CNTL, or any write to the timer status/control register (TPM1SC).

Reset clears the TPM counter registers.

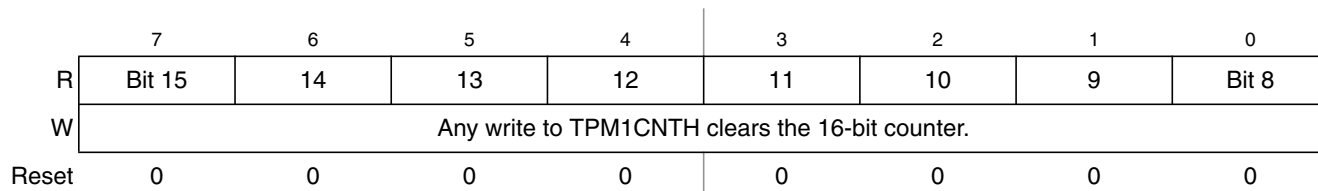


Figure 10-6. Timer Counter Register High (TPM1CNTH)

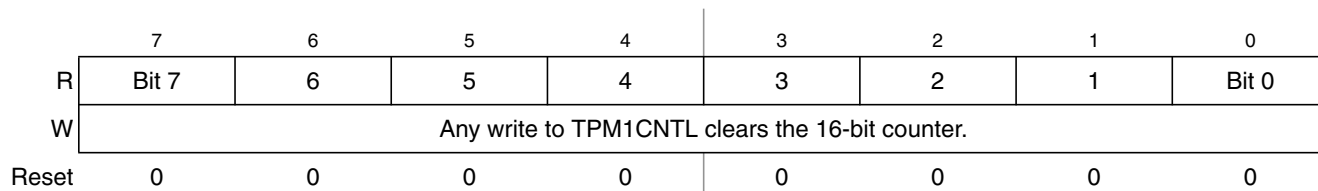


Figure 10-7. Timer Counter Register Low (TPM1CNTL)

Chapter 11

Serial Communications Interface (S08SCIV1)

11.1 Introduction

The MC9S08RDxx, MC9S08RExx, and MC9S08RGxx devices include a serial communications interface (SCI) module, which is sometimes called a universal asynchronous receiver/transmitters (UART). The SCI module shares pins with PTB0 and PTB1 port pins. When the SCI is enabled, the pins are controlled by the SCI module.

Figure 11-1 is a device-level block diagram with the SCI highlighted.

SCI1D. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead and the data and any associated NF, FE, or PF condition is lost.

12.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

12.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCI1C1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCI1C3. For the receiver, the ninth bit is held in R8 in SCI1C3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCI1D.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCI1D to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

12.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes.

No SCI module registers are affected in stop3 mode.

Because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

12.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is

Figure 15-3 shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.

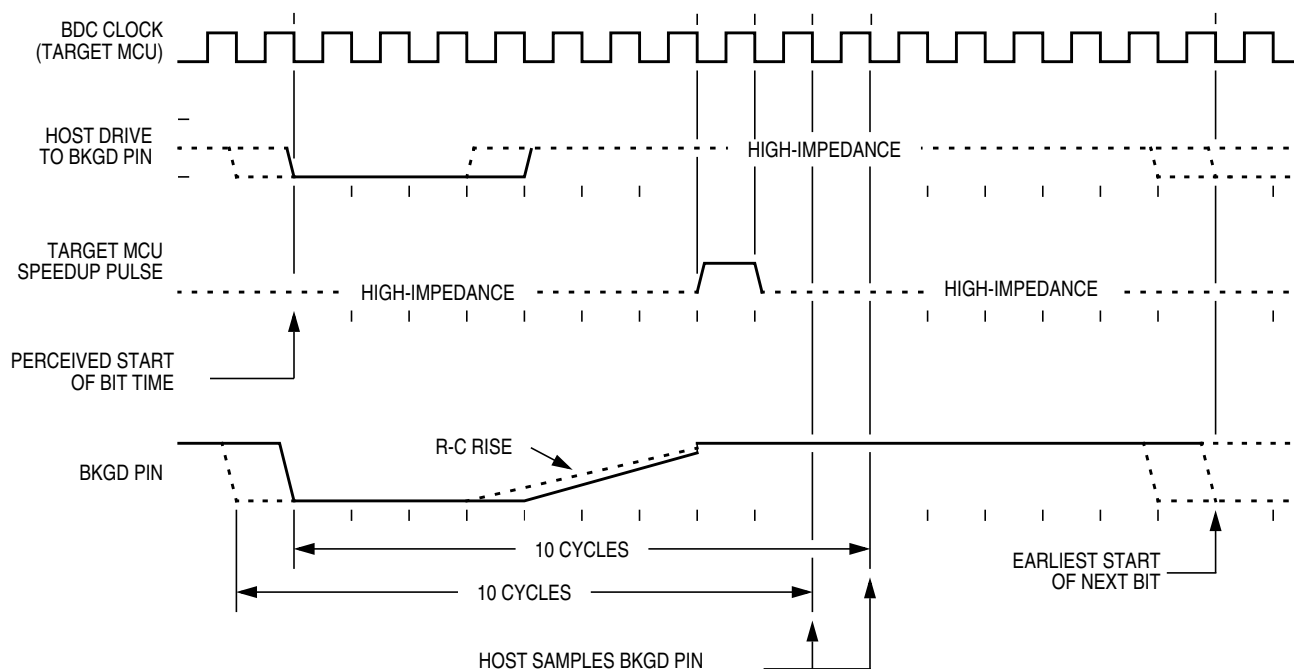


Figure 15-3. BDC Target-to-Host Serial Bit Timing (Logic 1)

15.4.3.8 Debug Trigger Register (DBGT)

This register can be read any time, but may be written only if ARM = 0, except bits 4 and 5 are hard-wired to 0s.

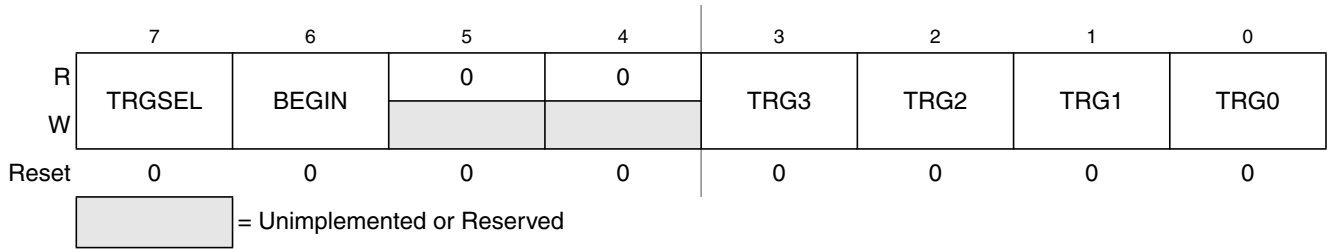


Figure 15-8. Debug Trigger Register (DBGT)

Table 15-5. DBGT Register Field Descriptions

Field	Description
7 TRGSEL	Trigger Type — Controls whether the match outputs from comparators A and B are qualified with the opcode tracking logic in the debug module. If TRGSEL is set, a match signal from comparator A or B must propagate through the opcode tracking logic and a trigger event is only signalled to the FIFO logic if the opcode at the match address is actually executed. 0 Trigger on access to compare address (force) 1 Trigger if opcode at compare address is executed (tag)
6 BEGIN	Begin/End Trigger Select — Controls whether the FIFO starts filling at a trigger or fills in a circular manner until a trigger ends the capture of information. In event-only trigger modes, this bit is ignored and all debug runs are assumed to be begin traces. 0 Data stored in FIFO until trigger (end trace) 1 Trigger initiates data storage (begin trace)
3:0 TRG[3:0]	Select Trigger Mode — Selects one of nine triggering modes, as described below. 0000 A-only 0001 A OR B 0010 A Then B 0011 Event-only B (store data) 0100 A then event-only B (store data) 0101 A AND B data (full mode) 0110 A AND NOT B data (full mode) 0111 Inside range: $A \leq \text{address} \leq B$ 1000 Outside range: $\text{address} < A$ or $\text{address} > B$ 1001 – 1111 (No trigger)