What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08re8cfge

List of Chapters

Chapter 6
Parallel Input/Output

Chapter 7
Central Processor Unit (S08CPUV2)

Table 2-2. Signal Properties

Pin Name	Dir[1]	High Current Pin	Pullup[2]	Comments[3]
V_{DD}		—	—	
V_{SS}		—	—	
XTAL	O	—	—	Crystal oscillator output
EXTAL	I	—	—	Crystal oscillator input
IRO	O	Y	—	Infrared output
PTA0/KBI1P0	I	N	SWC	PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}.
PTA1/KBI1P1	I/O	N	SWC	
PTA2/KBI1P2	I/O	N	SWC	
PTA3/KBI1P3	I/O	N	SWC	
PTA4/KBI1P4	I/O	N	SWC	
PTA5/KBI1P5	I/O	N	SWC	
PTA6/KBI1P6	I/O	N	SWC	
PTA7/KBI1P7	I/O	N	SWC	
PTB0/TxD1	I/O	Y	SWC	
PTB1/RxD1	I/O	Y	SWC	
PTB2	I/O	Y	SWC	
PTB3	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB4	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB5	I/O	Y	SWC	Available only in 44- and 48-pin packages
PTB6	I/O	Y	SWC	Available only in 32-, 44-, and 48-pin packagess
PTB7/TPM1CH1	I/O	Y	SWC	
PTC0/KBI2P0	I/O	N	SWC	
PTC1/KBI2P1	I/O	N	SWC	
PTC2/KBI2P2	I/O	N	SWC	
PTC3/KBI2P3	I/O	N	SWC	
PTC4/MOSI1	I/O	N	SWC	
PTC5/MISO1	I/O	N	SWC	
PTC6/SPSCK1	I/O	N	SWC	
PTC7/$\overline{SS1}$	I/O	N	SWC	
PTD0/BKGD/MS	I/O	N	SWC[4]	Output-only when configured as PTD0 pin. Pullup enabled.
PTD1/$\overline{RESET}$	I/O	N	SWC[3]	Output-only when configured as PTD1 pin.

Table 4-1. Direct-Page Register Summary (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$002A	IRQSC	0	0	IRQEDG	IRQPE	IRQF	IRQACK	IRQIE	IRQMOD
$002B	ACMP1SC[2]	ACME	ACBGS	ACF	ACIE	ACO	—	ACMOD1	ACMOD0
$002C–$002F	Reserved	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
$0030	TPM1SC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
$0031	TPM1CNTH	Bit 15	14	13	12	11	10	9	Bit 8
$0032	TPM1CNTL	Bit 7	6	5	4	3	2	1	Bit 0
$0033	TPM1MODH	Bit 15	14	13	12	11	10	9	Bit 8
$0034	TPM1MODL	Bit 7	6	5	4	3	2	1	Bit 0
$0035	TPM1C0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
$0036	TPM1C0VH	Bit 15	14	13	12	11	10	9	Bit 8
$0037	TPM1C0VL	Bit 7	6	5	4	3	2	1	Bit 0
$0038	TPM1C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
$0039	TPM1C1VH	Bit 15	14	13	12	11	10	9	Bit 8
$003A	TPM1C1VL	Bit 7	6	5	4	3	2	1	Bit 0
$003B–$003F	Reserved	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
$0040	**SPI1C1**[3]	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
$0041	SPI1C2[3]	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
$0042	**SPI1BR**[3]	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
$0043	**SPI1S**[3]	SPRF	0	SPTEF	MODF	0	0	0	0
$0044	Reserved	—	—	—	—	—	—	—	—
$0045	**SPI1D**[3]	Bit 7	6	5	4	3	2	1	Bit 0

1. The SCI module is not included on the MC9S08RC devices. This is a reserved location for those devices.

2. The analog comparator (ACMP) module is not included on the MC9S08RD devices. This is a reserved location for those devices.

3. The SPI module is not included on the MC9S08RC/RD/RE devices. These are reserved locations on the 32K and 60K versions of these devices. The address range $0040–$004F are RAM locations on the 16K and 8K devices. There are no MC9S08RG8/16 devices.

High-page registers, shown in Table 4-2, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at $1800.

Table 4-2. High-Page Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$1800	SRS	POR	PIN	COP	ILOP	ILAD[1]	0	LVD	0
$1801	SBDFR	0	0	0	0	0	0	0	BDFR
$1802	SOPT	7	COPT	STOPE	—	0	0	BKGDPE	RSTPE
$1803–$1804	Reserved	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
$1805	Reserved	0	0	0	0	0	0	0	0
$1806	SDIDH	REV3	REV2	REV1	REV0	ID11	ID10	ID9	ID8
$1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
$1808	SRTISC	RTIF	RTIACK	RTICLKS	RTIE	0	RTIS2	RTIS1	RTIS0

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4.4.7 Vector Redirection

Whenever any block protection is enabled, the reset and interrupt vectors will be protected. For this reason, a mechanism for redirecting vector reads is provided. Vector redirection allows users to modify interrupt vector information without unprotecting bootloader and reset vector space. For redirection to occur, at least some portion but not all of the FLASH memory must be block protected by programming the NVPROT register located at address $FFBD. All of the interrupt vectors (memory locations $FFC0–$FFFD) are redirected, while the reset vector ($FFFE:FFFF) is not.

For example, if 512 bytes of FLASH are protected, the protected address region is from $FE00 through $FFFF. The interrupt vectors ($FFC0–$FFFD) are redirected to the locations $FDC0–$FDFD. Now, if an SPI interrupt is taken for instance, the values in the locations $FDE0:FDE1 are used for the vector instead of the values in the locations $FFE0:FFE1. This allows the user to reprogram the unprotected portion of the FLASH with new program code including new interrupt vector values while leaving the protected area, which includes the default vector locations, unchanged.

4.5 Security

The MC9S08RC/RD/RE/RG includes circuitry to prevent unauthorized access to the contents of FLASH and RAM memory. When security is engaged, FLASH and RAM are considered secure resources. Direct-page registers, high-page registers, and the background debug controller are considered unsecured resources. Programs executing within secure memory have normal access to any MCU memory locations and resources. Attempts to access a secure memory location with a program executing from an unsecured memory space or through the background debug interface are blocked (writes are ignored and reads return all 0s).

Security is engaged or disengaged based on the state of two nonvolatile register bits (SEC01:SEC00) in the FOPT register. During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into the working FOPT register in high-page register space. A user engages security by programming the NVOPT location, which can be done at the same time the FLASH memory is programmed. The 1:0 state disengages security while the other three combinations engage security. Notice the erased state (1:1) makes the MCU secure. During development, whenever the FLASH is erased, it is good practice to immediately program the SEC00 bit to 0 in NVOPT so SEC01:SEC00 = 1:0. This would allow the MCU to remain unsecured after a subsequent reset.

The on-chip debug module cannot be enabled while the MCU is secure. The separate background debug controller can still be used for background memory access commands, but the MCU cannot enter active background mode except by holding BKGD/MS low at the rising edge of reset.

A user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. If the nonvolatile KEYEN bit in NVOPT/FOPT is 0, the backdoor key is disabled and there is no way to disengage security without completely erasing all FLASH locations. If KEYEN is 1, a secure user program can temporarily disengage security by:

1. Writing 1 to KEYACC in the FCNFG register. This makes the FLASH module interpret writes to the backdoor comparison key locations (NVBACKKEY through NVBACKKEY+7) as values to be compared against the key rather than as the first step in a FLASH program or erase command.
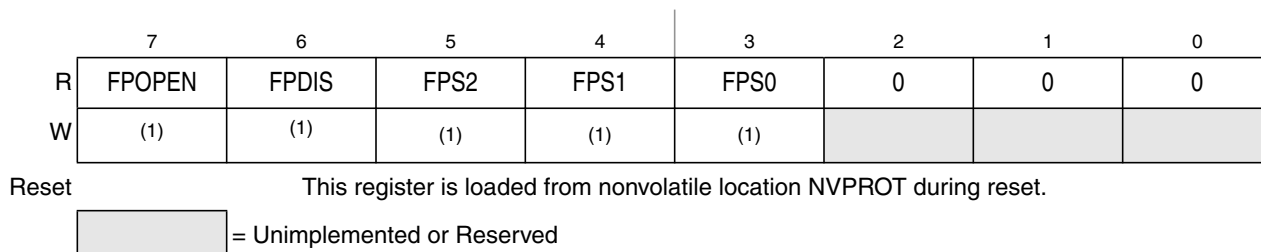
	7	6	5	4	3	2	1	0
R			KEYACC					
W								
Reset	0	0	0	0	0	0	0	0

[ ] = Unimplemented or Reserved
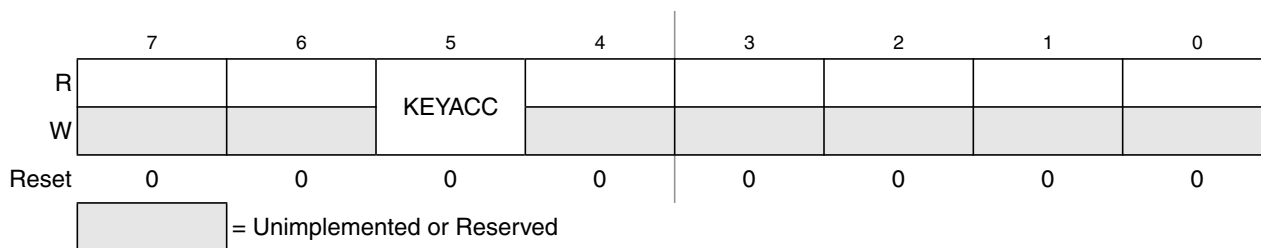
Figure 4-7. FLASH Configuration Register (FCNFG)

Table 4-8. FCNFG Field Descriptions

Field	Description
5 KEYACC	**Enable Writing of Access Key** — This bit enables writing of the backdoor comparison key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, "Security." 0 Writes to $FFB0–$FFB7 are interpreted as the start of a FLASH programming or erase command. 1 Writes to NVBACKKEY ($FFB0–$FFB7) are interpreted as comparison key writes. Reads of the FLASH return invalid data.

4.6.4 FLASH Protection Register (FPROT and NVPROT)

During reset, the contents of the nonvolatile location NVPROT is copied from FLASH into FPROT. Bits 0, 1, and 2 are not used and each always reads as 0. This register may be read at any time, but user program writes have no meaning or effect. Background debug commands can write to FPROT at $1824.

	7	6	5	4	3	2	1	0
R	FPOPEN	FPDIS	FPS2	FPS1	FPS0	0	0	0
W	(1)	(1)	(1)	(1)	(1)			
Reset			This register is loaded from nonvolatile location NVPROT during reset.					

[ ] = Unimplemented or Reserved

Figure 4-8. FLASH Protection Register (FPROT)
1. Background commands can be used to change the contents of these bits in FPROT.

Table 4-9. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Open Unprotected FLASH for Program/Erase** 0 Entire FLASH memory is block protected (no program or erase allowed). 1 Any FLASH location, not otherwise block protected or secured, may be erased or programmed.
6 FPDIS	**FLASH Protection Disable** 0 FLASH block specified by FPS2:FPS0 is block protected (program and erase not allowed). 1 No FLASH block is protected.
5:3 FPS[2:0]	**FLASH Protect Size Selects** — When FPDIS = 0, this 3-bit field determines the size of a protected block of FLASH locations at the high address end of the FLASH (see Table 4-10 and Table 4-11). Protected FLASH locations cannot be erased or programmed.

6.6.1   Port A Registers (PTAD, PTAPE, and PTADD)

Port A pins used as general-purpose I/O pins are controlled by the port A data (PTAD), data direction (PTADD), and pullup enable (PTAPE) registers.
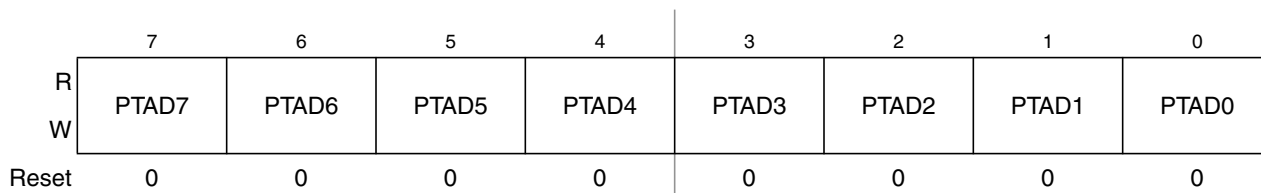
	7	6	5	4	3	2	1	0
R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-6. Port A Data Register (PTAD)

Table 6-1. PTAD Field Descriptions

Field	Description
7:0 PTAD[7:0]	**Port A Data Register Bits** — For port A pins that are inputs, reads of this register return the logic level on the pin. For port A pins that are configured as outputs, reads of this register return the last value written to this register. Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTAD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

	7	6	5	4	3	2	1	0
R	PTAPE7	PTAPE6	PTAPE5	PTAPE4	PTAPE3	PTAPE2	PTAPE1	PTAPE0
W								
Reset	0	0	0	0	0	0	0	0
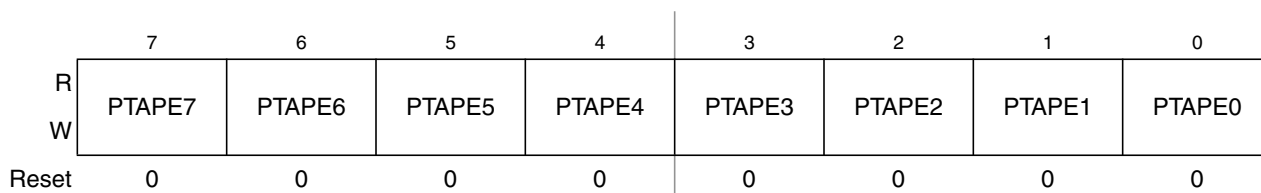
Figure 6-7. Pullup Enable for Port A (PTAPE)

Table 6-2. PTAPE Field Descriptions

Field	Description
7:0 PTAPE[7:0]	**Pullup Enable for Port A Bits** — For port A pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled provided the corresponding PTADDn is a logic 0. For port A pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled. When any of bits 7 through 4 of port A are enabled as KBI inputs and are configured to detect rising edges/high levels, the pullup enable bits enable pulldown rather than pullup devices. 0 Internal pullup device disabled. 1 Internal pullup device enabled.

Table 7-2. HCS08 Instruction Set Summary (Sheet 5 of 7)

Source Form	Operation	Description	Effect on CCR V	H	I	N	Z	C	Address Mode	Opcode	Operand	Bus Cycles[1]
LDX #opr8i LDX opr8a LDX opr16a LDX oprx16,X LDX oprx8,X LDX ,X LDX oprx16,SP LDX oprx8,SP	Load X (Index Register Low) from Memory	X ← (M)	0	–	–			–	IMM DIR EXT IX2 IX1 IX SP2 SP1	AE BE CE DE EE FE 9EDE 9EEE	ii dd hh ll ee ff ff ee ff ff	2 3 4 4 3 3 5 4
LSL opr8a LSLA LSLX LSL oprx8,X LSL ,X LSL oprx8,SP	Logical Shift Left (Same as ASL)			–	–				DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	5 1 1 5 4 6
LSR opr8a LSRA LSRX LSR oprx8,X LSR ,X LSR oprx8,SP	Logical Shift Right			–	–	0			DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	5 1 1 5 4 6
MOV opr8a,opr8a MOV opr8a,X+ MOV #opr8i,opr8a MOV ,X+,opr8a	Move	(M)destination ← (M)source H:X ← (H:X) + 0x0001 in IX+/DIR and DIR/IX+ Modes	0	–	–			–	DIR/DIR DIR/IX+ IMM/DIR IX+/DIR	4E 5E 6E 7E	dd dd dd ii dd dd	5 5 4 5
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	0	INH	42		5
NEG opr8a NEGA NEGX NEG oprx8,X NEG ,X NEG oprx8,SP	Negate (Two's Complement)	M ← – (M) = 0x00 – (M) A ← – (A) = 0x00 – (A) X ← – (X) = 0x00 – (X) M ← – (M) = 0x00 – (M) M ← – (M) = 0x00 – (M) M ← – (M) = 0x00 – (M)		–	–				DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff	5 1 1 5 4 6
NOP	No Operation	Uses 1 Bus Cycle	–	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap Accumulator	A ← (A[3:0]:A[7:4])	–	–	–	–	–	–	INH	62		1
ORA #opr8i ORA opr8a ORA opr16a ORA oprx16,X ORA oprx8,X ORA ,X ORA oprx16,SP ORA oprx8,SP	Inclusive OR Accumulator and Memory	A ← (A)	(M)	0	–	–			–	IMM DIR EXT IX2 IX1 IX SP2 SP1	AA BA CA DA EA FA 9EDA 9EEA	ii dd hh ll ee ff ff ee ff ff	2 3 4 4 3 3 5 4
PSHA	Push Accumulator onto Stack	Push (A); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	87		2
PSHH	Push H (Index Register High) onto Stack	Push (H); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	8B		2
PSHX	Push X (Index Register Low) onto Stack	Push (X); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	89		2
PULA	Pull Accumulator from Stack	SP ← (SP + 0x0001); Pull (A)	–	–	–	–	–	–	INH	86		3
PULH	Pull H (Index Register High) from Stack	SP ← (SP + 0x0001); Pull (H)	–	–	–	–	–	–	INH	8A		3
PULX	Pull X (Index Register Low) from Stack	SP ← (SP + 0x0001); Pull (X)	–	–	–	–	–	–	INH	88		3
ROL opr8a ROLA ROLX ROL oprx8,X ROL ,X ROL oprx8,SP	Rotate Left through Carry			–	–				DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	5 1 1 5 4 6

Chapter 8
Carrier Modulator Timer (S08CMTV1)

8.1   Introduction

Figure 8-1. MC9S08RC/RD/RE/RG Block Diagram
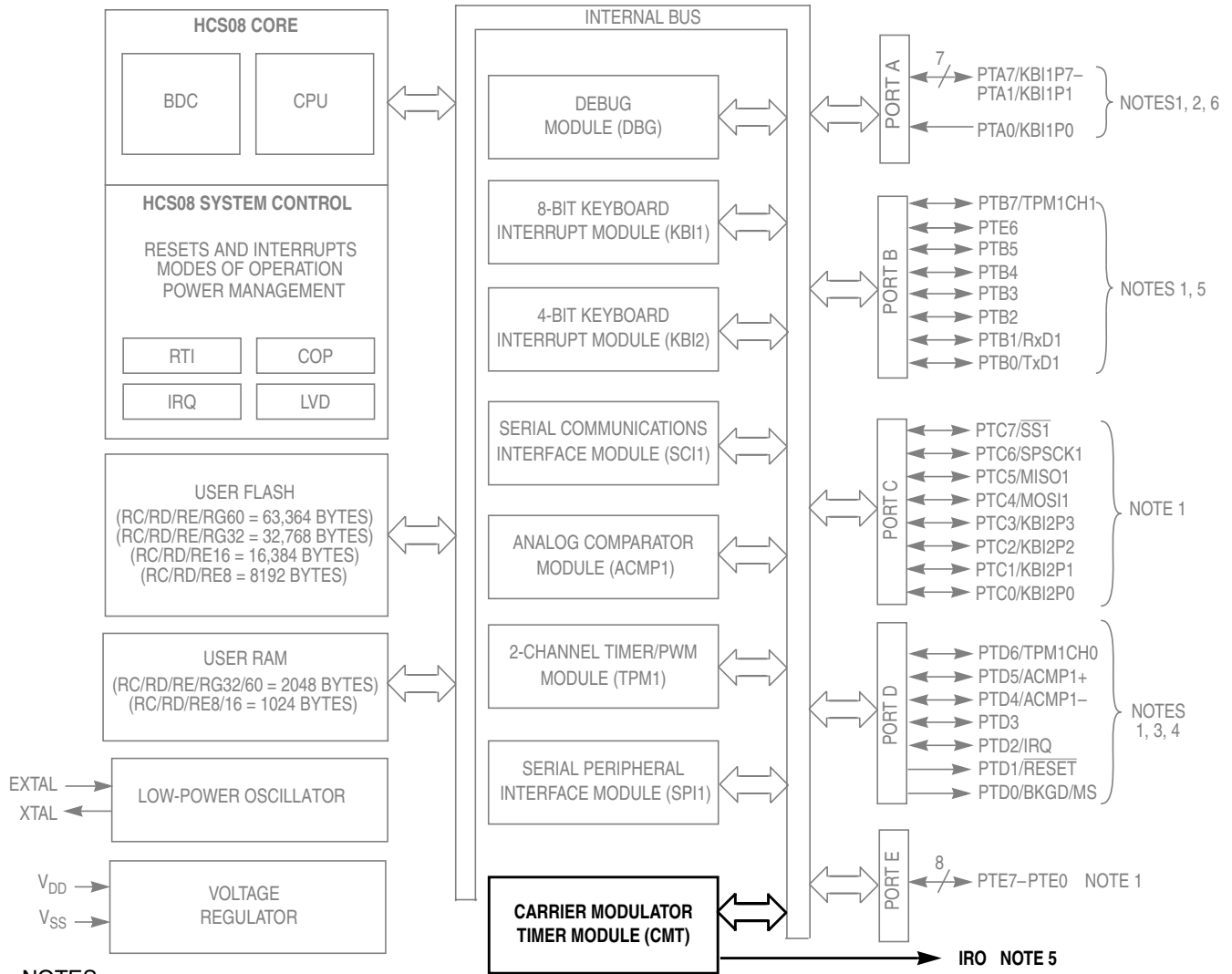
NOTES:
1. Port pins are software configurable with pullup device if input port
2. PTA0 does not have a clamp diode to VDD. PTA0 should not be driven above VDD. Also, PTA0 does not pullup to VDD when internal pullup is enabled.
3. IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)
4. The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)
5. **High current drive**
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

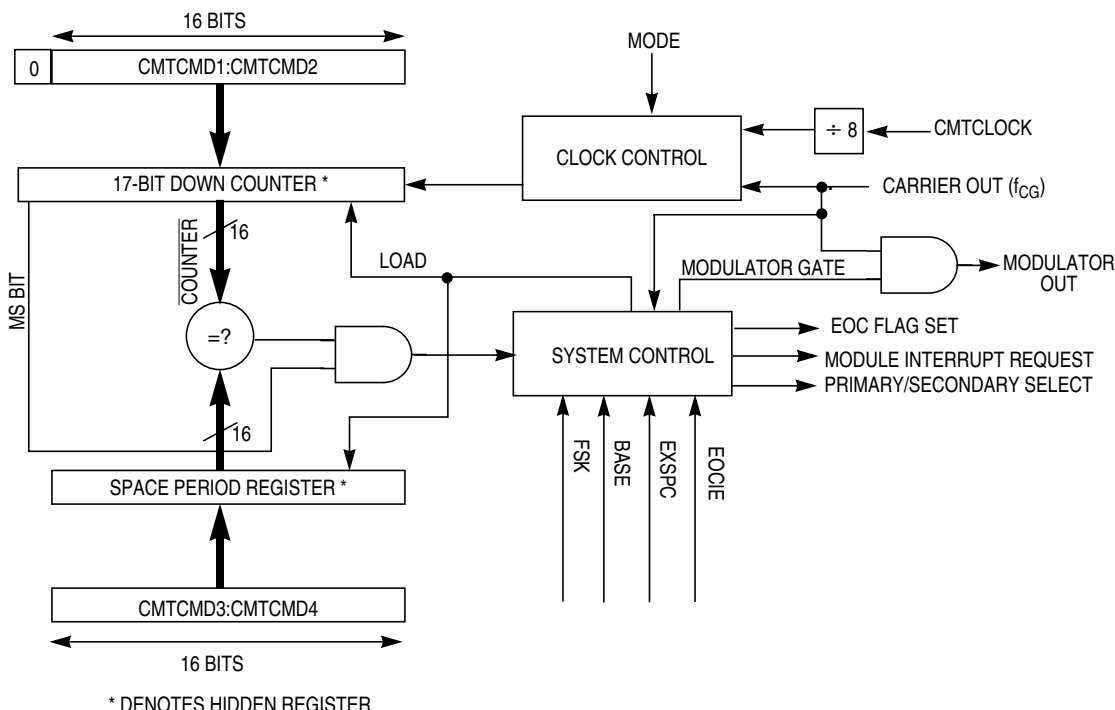**MC9S08RC/RD/RE/RG Data Sheet, Rev. 1.11**

Figure 8-4. Modulator Block Diagram

8.5.2.1 Time Mode

When the modulator operates in time mode (MCGEN bit is set, BASE bit is clear, and FSK bit is clear), the modulation mark period consists of an integer number of CMTCLK ÷ 8 clock periods. The modulation space period consists of zero or an integer number of CMTCLK ÷ 8 clock periods. With an 8 MHz bus and CMTDIV1:CMTDIV0 = 00, the modulator resolution is 1 µs and has a maximum mark and space period of about 65.535 ms each. See Figure 8-5 for an example of the time mode and baseband mode outputs.

The mark and space time equations for time and baseband mode are:

$$t_{mark} = (CMTCMD1:CMTCMD2 + 1) \div (f_{CMTCLK} \div 8)$$ *Eqn. 8-5*

$$t_{space} = CMTCMD3:CMTCMD4 \div (f_{CMTCLK} \div 8)$$ *Eqn. 8-6*

where CMTCMD1:CMTCMD2 and CMTCMD3:CMTCMD4 are the decimal values of the concatenated registers.

NOTE

If the modulator is disabled while the t_{mark} time is less than the programmed carrier high time (t_{mark} < CMTCGH1/f_{CMTCLK}), the modulator can enter into an illegal state and end the curent cycle before the programmed value. Make sure to program t_{mark} greater than the carrier high time to avoid this illegal state.

$$t_{exspace} = t_{space} + (t_{mark} + t_{space}) \text{ x (number of modulation periods)} \qquad \textit{Eqn. 8-9}$$

For an example of extended space operation, see Figure 8-7.

NOTE

The EXSPC feature can be used to emulate a zero mark event.
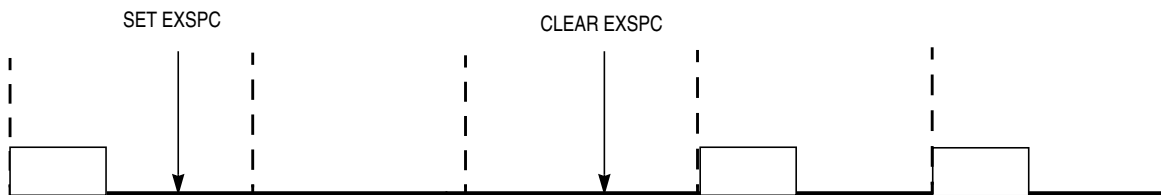

Figure 8-7. Extended Space Operation

8.5.3.2   EXSPC Operation in FSK Mode

In FSK mode, the modulator continues to count carrier out clocks, alternating between the primary and secondary registers at the end of each modulation period.

To calculate the length of an extended space in FSK mode, the user must know whether the EXSPC bit was set on a primary or secondary modulation period, as well as the total number of both primary and secondary modulation periods completed while the EXSPC bit is high. A status bit for the current modulation is not accessible to the CPU. If necessary, software should maintain tracking of the current modulation cycle (primary or secondary). The extended space period ends at the completion of the space period time of the modulation period during which the EXSPC bit is cleared.

If the EXSPC bit was set during a primary modulation cycle, use the equation:

$$t_{exspace} = (t_{space})_p + (t_{mark} + t_{space})_s + (t_{mark} + t_{space})_p +... \qquad \textit{Eqn. 8-10}$$

Where the subscripts p and s refer to mark and space times for the primary and secondary modulation cycles.

If the EXSPC bit was set during a secondary modulation cycle, use the equation:

$$t_{exspace} = (t_{space})_s + (t_{mark} + t_{space})_p + (t_{mark} + t_{space})_s +... \qquad \textit{Eqn. 8-11}$$

8.5.4   Transmitter

The transmitter output block controls the state of the infrared out pin (IRO). The modulator output is gated on to the IRO pin when the modulator/carrier generator is enabled. When the modulator/carrier generator is disabled, the IRO pin is controlled by the state of the IRO latch.

A polarity bit in the CMTOC register enables the IRO pin to be high true or low true.

8.5.5   CMT Interrupts

The end of cycle flag (EOCF) is set when:

- The modulator is not currently active and the MCGEN bit is set to begin the initial CMT transmission
- At the end of each modulation cycle (when the counter is reloaded from CMTCMD1:CMTCMD2) while the MCGEN bit is set

In the case where the MCGEN bit is cleared and then set before the end of the modulation cycle, the EOCF bit will not be set when the MCGEN is set, but will become set at the end of the current modulation cycle.

When the MCGEN becomes disabled, the CMT module does not set the EOC flag at the end of the last modulation cycle.

The EOCF bit is cleared by reading the CMT modulator status and control register (CMTMSC) followed by an access of CMTCMD2 or CMTCMD4.

If the EOC interrupt enable (EOCIE) bit is high when the EOCF bit is set, the CMT module will generate an interrupt request. The EOCF bit must be cleared within the interrupt service routine to prevent another interrupt from being generated after exiting the interrupt service routine.

The EOC interrupt is coincident with loading the down-counter with the contents of CMTCMD1:CMTCMD2 and loading the space period register with the contents of CMTCMD3:CMTCMD4. The EOC interrupt provides a means for the user to reload new mark/space values into the modulator data registers. Modulator data register updates will take effect at the end of the current modulation cycle. Note that the down-counter and space period register are updated at the end of every modulation cycle, regardless of interrupt handling and the state of the EOCF flag.

8.5.6   Wait Mode Operation

During wait mode the CMT, if enabled, will continue to operate normally. However, there will be no new codes or changes of pattern mode while in wait mode, because the CPU is not operating.

8.5.7   Stop Mode Operation

During all stop modes, clocks to the CMT module are halted.

In stop1 and stop2 modes, all CMT register data is lost and must be re-initialized upon recovery from these two stop modes.

No CMT module registers are affected in stop3 mode.

Note, because the clocks are halted, the CMT will resume upon exit from stop (only in stop3 mode). Software should ensure stop2 or stop3 mode is not entered while the modulator is in operation to prevent the IRO pin from being asserted while in stop mode. This may require a time-out period from the time that the MCGEN bit is cleared to allow the last modulator cycle to complete.

independently be configured to operate in input capture, output compare, or buffered edge-aligned PWM mode.

The following sections describe the main 16-bit counter and each of the timer operating modes (input capture, output compare, edge-aligned PWM, and center-aligned PWM). Because details of pin operation and interrupt activity depend on the operating mode, these topics are covered in the associated mode sections.

10.5.1   Counter

All timer functions are based on the main 16-bit counter (TPM1CNTH:TPM1CNTL). This section discusses selection of the clock source, up-counting vs. up-/down-counting, end-of-count overflow, and manual counter reset.

After any MCU reset, CLKSB:CLKSA = 0:0 so no clock source is selected and the TPM is inactive. Normally, CLKSB:CLKSA would be set to 0:1 so the bus clock drives the timer counter. The clock source for the TPM can be selected to be off, the bus clock (BUSCLK), the fixed system clock (XCLK), or an external input through the TPM1CH0 pin. The maximum frequency allowed for the external clock option is one-fourth the bus rate. Refer to Section 10.7.1, "Timer Status and Control Register (TPM1SC)," and Table 10-2 for more information about clock source selection.

When the microcontroller is in active background mode, the TPM temporarily suspends all counting until the microcontroller returns to normal user operating mode. During stop mode, all TPM clocks are stopped; therefore, the TPM is effectively disabled until clocks resume. During wait mode, the TPM continues to operate normally.

The main 16-bit counter has two counting modes. When center-aligned PWM is selected (CPWMS = 1), the counter operates in up-/down-counting mode. Otherwise, the counter operates as a simple up-counter. As an up-counter, the main 16-bit counter counts from $0000 through its terminal count and then continues with $0000. The terminal count is $FFFF or a modulus value in TPM1MODH:TPM1MODL.

When center-aligned PWM operation is specified, the counter counts upward from $0000 through its terminal count and then counts downward to $0000 where it returns to up-counting. Both $0000 and the terminal count value (value in TPM1MODH:TPM1MODL) are normal length counts (one timer clock period long).

An interrupt flag and enable are associated with the main 16-bit counter. The timer overflow flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE = 0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE = 1) where a static hardware interrupt is automatically generated whenever the TOF flag is 1.

The conditions that cause TOF to become set depend on the counting mode (up or up/down). In up-counting mode, the main 16-bit counter counts from $0000 through $FFFF and overflows to $0000 on the next counting clock. TOF becomes set at the transition from $FFFF to $0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to $0000. When the main 16-bit counter is operating in up-/down-counting mode, the TOF flag gets set as the counter changes direction at the transition from the value set in the modulus register and the next lower count value. This corresponds to the end of a PWM period. (The $0000 count value corresponds to the center of a period.)

10.6   TPM Interrupts

The TPM generates an optional interrupt for the main counter overflow and an interrupt for each channel. The meaning of channel interrupts depends on the mode of operation for each channel. If the channel is configured for input capture, the interrupt flag is set each time the selected input capture edge is recognized. If the channel is configured for output compare or PWM modes, the interrupt flag is set each time the main timer counter matches the value in the 16-bit channel value register. See the Resets, Interrupts, and System Configuration chapter for absolute interrupt vector addresses, priority, and local interrupt mask control bits.

For each interrupt source in the TPM, a flag bit is set on recognition of the interrupt condition such as timer overflow, channel input capture, or output compare events. This flag may be read (polled) by software to verify that the action has occurred, or an associated enable bit (TOIE or CHnIE) can be set to enable hardware interrupt generation. While the interrupt enable bit is set, a static interrupt will be generated whenever the associated interrupt flag equals 1. It is the responsibility of user software to perform a sequence of steps to clear the interrupt flag before returning from the interrupt service routine.

10.6.1   Clearing Timer Interrupt Flags

TPM interrupt flags are cleared by a 2-step process that includes a read of the flag bit while it is set (1) followed by a write of 0 to the bit. If a new event is detected between these two steps, the sequence is reset and the interrupt flag remains set after the second step to avoid the possibility of missing the new event.

10.6.2   Timer Overflow Interrupt Description

The conditions that cause TOF to become set depend on the counting mode (up or up/down). In up-counting mode, the 16-bit timer counter counts from $0000 through $FFFF and overflows to $0000 on the next counting clock. TOF becomes set at the transition from $FFFF to $0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to $0000. When the counter is operating in up-/down-counting mode, the TOF flag gets set as the counter changes direction at the transition from the value set in the modulus register and the next lower count value. This corresponds to the end of a PWM period. (The $0000 count value corresponds to the center of a period.)

10.6.3   Channel Event Interrupt Description

The meaning of channel interrupts depends on the current mode of the channel (input capture, output compare, edge-aligned PWM, or center-aligned PWM).

When a channel is configured as an input capture channel, the ELSnB:ELSnA control bits select rising edges, falling edges, any edge, or no edge (off) as the edge that triggers an input capture event. When the selected edge is detected, the interrupt flag is set. The flag is cleared by the 2-step sequence described in Section 10.6.1, "Clearing Timer Interrupt Flags."

When a channel is configured as an output compare channel, the interrupt flag is set each time the main timer counter matches the 16-bit value in the channel value register. The flag is cleared by the 2-step sequence described in Section 10.6.1, "Clearing Timer Interrupt Flags."

Chapter 11
Serial Communications Interface (S08SCIV1)

11.1 Introduction

The MC9S08RDxx, MC9S08RExx, and MC9S08RGxx devices include a serial communications interface (SCI) module, which is sometimes called a universal asynchronous receiver/transmitters (UART). The SCI module shares pins with PTB0 and PTB1 port pins. When the SCI is enabled, the pins are controlled by the SCI module.

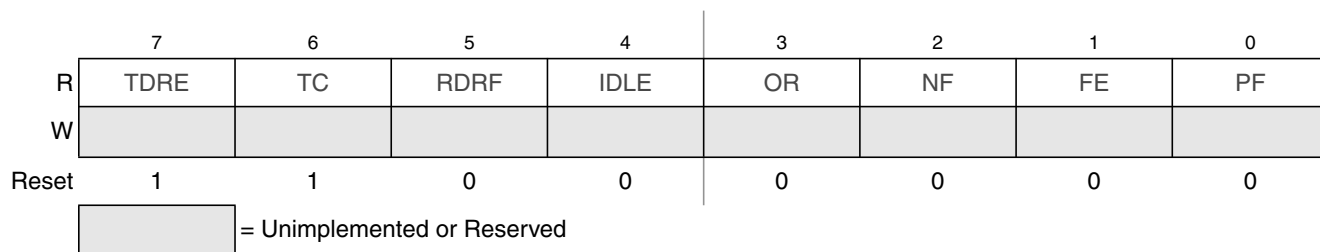Figure 11-1 is a device-level block diagram with the SCI highlighted.

Table 12-4. SCI1C2 Register Field Descriptions (continued)

Field	Description
1 RWU	**Receiver Wakeup Control** — This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is either an idle line between messages (WAKE = 0, idle-line wakeup), or a logic 1 in the most significant data bit in a character (WAKE = 1, address-mark wakeup). Application software sets RWU and (normally) a selected hardware condition automatically clears RWU. Refer to Section 12.3.3.2, "Receiver Wakeup Operation," for more details. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	**Send Break** — Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 bit times of logic 0 are queued as long as SBK = 1. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. Refer to Section 12.3.2.1, "Send Break and Queued Idle," for more details. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

12.2.4 SCI Status Register 1 (SCI1S1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.

	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W								
Reset	1	1	0	0	0	0	0	0

☐ = Unimplemented or Reserved

Figure 12-7. SCI Status Register 1 (SCI1S1)

Table 12-5. SCI1S1 Register Field Descriptions

Field	Description
7 TDRE	**Transmit Data Register Empty Flag** — TDRE is set immediately after reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCI1S1 with TDRE = 1 and then write to the SCI data register (SCI1D). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.

6
TC
	Transmission Complete Flag — TC is set immediately after reset and when TDRE = 1 and no data, preamble, or break character is being transmitted.
	0 Transmitter active (sending data, a preamble, or a break).
	1 Transmitter idle (transmission activity complete).
	TC is cleared automatically by reading SCI1S1 with TC = 1 and then doing one of the following three things:
	   • Write to the SCI data register (SCI1D) to transmit new data
	   • Queue a preamble by changing TE from 0 to 1
	   • Queue a break character by writing 1 to SBK in SCI1C2

the transmit data register is transferred to the shift register (synchronized with the baud rate clock) and the transmit data register empty (TDRE) status flag is set to indicate another character may be written to the transmit data buffer at SCI1D.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD1 pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD1 high, waiting for more characters to transmit.

Writing 0 to TE does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity that is in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

12.3.2.1   Send Break and Queued Idle

The SBK control bit in SCI1C2 is used to send break characters which were originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0 (10 bit times including the start and stop bits). Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 1 and then write 0 to the SBK bit. This action queues a break character to be sent as soon as the shifter is available. If SBK is still 1 when the queued break moves into the shifter (synchronized to the baud rate clock), an additional break character is queued. If the receiving device is another Freescale Semiconductor SCI, the break characters will be received as 0s in all eight data bits and a framing error (FE = 1) occurs.

When idle-line wakeup is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the TE bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while TE = 0, the SCI transmitter never actually releases control of the TxD1 pin. If there is a possibility of the shifter finishing while TE = 0, set the general-purpose I/O controls so the pin that is shared with TxD1 is an output driving a logic 1. This ensures that the TxD1 line will look like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to TE.

12.3.3   Receiver Functional Description

In this section, the data sampling technique used to reconstruct receiver data is described in more detail; two variations of the receiver wakeup function are explained. (The receiver block diagram is shown in Figure 12-2.)

The receiver is enabled by setting the RE bit in SCI1C2. Character frames consist of a start bit of logic 0, eight (or nine) data bits (LSB first), and a stop bit of logic 1. For information about 9-bit data mode, refer to Section 12.3.5.1, "8- and 9-Bit Data Modes." For the remainder of this discussion, we assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (RDRF) status flag is set. If RDRF was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								BDFR[1]
Reset	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

[1] BDFR is writable only through serial active background mode debug commands, not from user programs.

Figure 15-6. System Background Debug Force Reset Register (SBDFR)

Table 15-3. SBDFR Register Field Description

Field	Description
0 BDFR	**Background Debug Force Reset** — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

15.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

15.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

15.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

15.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

15.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

Table A-5. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Maximum low-voltage safe state re-arm[3]	V_{REARM}	—	—	3.0	V
Input high voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$		—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$		—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—		$0.35 \times V_{DD}$	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—		$0.30 \times V_{DD}$	V
Input hysteresis (all digital inputs)	V_{hys}	$0.06 \times V_{DD}$		—	V
Input leakage current (Per pin) $V_{In} = V_{DD}$ or $V_{SS,}$ all input only pins	$|I_{In}|$	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or $V_{SS,}$ all input/output	$|I_{OZ}|$	—	0.025	1.0	μA
Internal pullup resistors[4] [5]	R_{PU}	17.5		52.5	κW
Internal pulldown resistor (IRQ)	R_{PD}	17.5		52.5	κW
Output high voltage (V_{DD} ≥ 1.8 V) I_{OH} = –2 mA (ports A, C, D and E)	V_{OH}	V_{DD} – 0.5		—	V
Output high voltage (port B and IRO) I_{OH} = –10 mA (V_{DD} ≥ 2.7 V) I_{OH} = –6 mA (V_{DD} ≥ 2.3 V) I_{OH} = –3 mA (V_{DD} ≥ 1.8 V)		V_{DD} – 0.5		— — —	
Maximum total I_{OH} for all port pins	$|I_{OHT}|$	—		60	mA
Output low voltage (V_{DD} ≥ 1.8 V) I_{OL} = 2.0 mA (ports A, C, D and E)	V_{OL}	—		0.5	V
Output low voltage (port B) I_{OL} = 10.0 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		0.5 0.5 0.5	
Output low voltage (IRO) I_{OL} = 16 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		1.2 1.2 1.2	
Maximum total I_{OL} for all port pins	I_{OLT}	—		60	mA
dc injection current[2], [6], [7], [8], [9] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins	$|I_{IC}|$	— —		0.2 5	mA mA
Input capacitance (all non-supply pins)	C_{In}	—		7	pF

1. RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.

2. This parameter is characterized and not tested on each device.

3. If SAFE bit is set, V_{DD} must be above re-arm voltage to allow MCU to accept interrupts, refer to Section 5.6, "Low-Voltage Detect (LVD) System."

4. Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

5. The PTA0 pullup resistor may not pull up to the specified minimum V_{IH}. However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no dc load is present on the pin.

6. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

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A.10 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter.

Table A-12. FLASH Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase	$V_{prog/erase}$	2.05		3.6	V
Supply voltage for read operation $0 < f_{Bus} < 8$ MHz	V_{Read}	1.8		3.6	V
Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
Page erase time[2]	t_{Page}		4000		t_{Fcyc}
Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
Program/erase endurance[3] T_L to $T_H = -40°C$ to $+ 85°C$ $T = 25°C$		10,000	100,000	— —	cycles
Data retention[4]	t_{D_ret}	15	100	—	years

1. The frequency of this clock is controlled by a software setting.

2. These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3. **Typical endurance for FLASH** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

4. **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.