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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08rg32cfge

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Chapter 1
Introduction

1.1 Overview

The MC9S08RC/RD/RE/RG are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in this family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Features

Features of the MC9S08RC/RD/RE/RG Family of devices are listed here. Please see Table 1-1 for the features that are available on the different family members.

HCS08 CPU (Central Processor Unit)	• Object code fully upward-compatible with M68HC05 and M68HC08 Families • HC08 instruction set with added BGND instruction • Support for up to 32 interrupt/reset sources • Power-saving modes: wait plus three stops
On-Chip Memory	• On-chip in-circuit programmable FLASH memory with block protection and security option • On-chip random-access memory (RAM)
Oscillator (OSC)	• Low power oscillator capable of operating from crystal or resonator from 1 to 16 MHz • 8 MHz internal bus frequency
Analog Comparator (ACMP1)	• On-chip analog comparator with internal reference (ACMP1) • Full rail-to-rail supply operation • Option to compare to a fixed internal bandgap reference voltage
Serial Communications Interface Module (SCI1)	• Full-duplex, standard non-return-to-zero (NRZ) format • Double-buffered transmitter and receiver with separate enables • Programmable 8-bit or 9-bit character length • Programmable baud rates (13-bit modulo divider)
Serial Peripheral Interface Module (SPI1)	• Master or slave mode operation • Full-duplex or single-wire bidirectional option • Programmable transmit bit rate • Double-buffered transmit and receive • Serial clock phase and polarity options • Slave select output • Selectable MSB-first or LSB-first shifting

2.3.4 Background/Mode Select (PTD0/BKGD/MS)

The background/mode select function is shared with an output-only port function on the PTD0/BKDG/MS pin. While in reset, the pin functions as a mode select pin. Immediately after reset rises, the pin functions as the background pin and can be used for background debug communication. While functioning as a background/mode select pin, this pin has an internal pullup device enabled. To use as an output-only port, BKGDPE in SOPT must be cleared.

If nothing is connected to this pin, the MCU will enter normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the rising edge of reset, which forces the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock could be as fast as the bus clock rate, so there should never be any significant capacitance connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

2.3.5 IRO Pin Description

The IRO pin is the output of the CMT. See the Carrier Modulator Timer (CMT) Module Chapter for a detailed description of this pin function.

2.3.6 General-Purpose I/O and Peripheral Ports

The remaining pins are shared among general-purpose I/O and on-chip peripheral functions such as timers and serial I/O systems. (Not all pins are available in all packages. See Table 2-2.) Immediately after reset, all 37 of these pins are configured as high-impedance general-purpose inputs with internal pullup devices disabled.

NOTE

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pullup devices or change the direction of unused pins to outputs so the pins do not float.

For information about controlling these pins as general-purpose I/O pins, see the Chapter 6, "Parallel Input/Output." For information about how and when on-chip peripheral systems use these pins, refer to the appropriate chapter from Table 2-1.

3.6 Stop Modes

One of three stop modes is entered upon execution of a STOP instruction when the STOPE bit in the system option register is set. In all stop modes, all internal clocks are halted. If the STOPE bit is not set when the CPU executes a STOP instruction, the MCU will not enter any of the stop modes and an illegal opcode reset is forced. The stop modes are selected by setting the appropriate bits in SPMSC2.

Table 3-1 summarizes the behavior of the MCU in each of the stop modes.

Table 3-1. Stop Mode Behavior

Mode	PDC	PPDC	CPU, Digital Peripherals, FLASH	RAM	OSC	ACMP	Regulator	I/O Pins	RTI
Stop1	1	0	Off	Off	Off	Standby	Standby	Reset	Off
Stop2	1	1	Off	Standby	Off	Standby	Standby	States held	Optionally on
Stop3	0	Don't care	Standby	Standby	Off	Standby	Standby	States held	Optionally on

3.6.1 Stop1 Mode

Stop1 mode provides the lowest possible standby power consumption by causing the internal circuitry of the MCU to be powered down. To enter stop1, the user must execute a STOP instruction with the PDC bit in SPMSC2 set and the PPDC bit clear. Stop1 can be entered only if the LVD reset is disabled (LVDRE = 0).

When the MCU is in stop1 mode, all internal circuits that are powered from the voltage regulator are turned off. The voltage regulator is in a low-power standby state, as are the OSC and ACMP.

Exit from stop1 is done by asserting any of the wakeup pins on the MCU: $\overline{\text{RESET}}$, IRQ, or KBI1, which have been enabled. IRQ and KBI pins are always active-low when used as wakeup pins in stop1 regardless of how they were configured before entering stop1.

Upon wakeup from stop1 mode, the MCU will start up as from a power-on reset (POR). The CPU will take the reset vector.

3.6.2 Stop2 Mode

Stop2 mode provides very low standby power consumption and maintains the contents of RAM and the current state of all of the I/O pins. To select entry into stop2 upon execution of a STOP instruction, the user must execute a STOP instruction with the PPDC and PDC bits in SPMSC2 set. Stop2 can be entered only if LVDRE = 0.

Before entering stop2 mode, the user must save the contents of the I/O port registers, as well as any other memory-mapped registers that they want to restore after exit of stop2, to locations in RAM. Upon exit from stop2, these values can be restored by user software.

When the MCU is in stop2 mode, all internal circuits that are powered from the voltage regulator are turned off, except for the RAM. The voltage regulator is in a low-power standby state, as is the ACMP. Upon entry

into stop2, the states of the I/O pins are latched. The states are held while in stop2 mode and after exiting stop2 mode until a 1 is written to PPDACK in SPMSC2.

Exit from stop2 is done by asserting any of the wakeup pins: $\overline{\text{RESET}}$, IRQ, or KBI1 that have been enabled, or through the real-time interrupt. IRQ and KBI1 pins are always active-low when used as wakeup pins in stop2 regardless of how they were configured before entering stop2. (KBI2 will not wake the MCU from stop2.)

Upon wakeup from stop2 mode, the MCU will start up as from a power-on reset (POR) except pin states remain latched. The CPU will take the reset vector. The system and all peripherals will be in their default reset states and must be initialized.

After waking up from stop2, the PPDF bit in SPMSC2 is set. This flag may be used to direct user code to go to a stop2 recovery routine. PPDF remains set and the I/O pin states remain latched until a 1 is written to PPDACK in SPMSC2.

For pins that were configured as general-purpose I/O, the user must copy the contents of the I/O port registers, which have been saved in RAM, back to the port registers before writing to the PPDACK bit. If the port registers are not restored from RAM before writing to PPDACK, then the register bits will be in their reset states when the I/O pin latches are opened and the I/O pins will switch to their reset states.

For pins that were configured as peripheral I/O, the user must reconfigure the peripheral module that interfaces to the pin before writing to the PPDACK bit. If the peripheral module is not enabled before writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

3.6.3 Stop3 Mode

Upon entering stop3 mode, all of the clocks in the MCU, including the oscillator itself, are halted. The OSC is turned off, the ACMP is disabled, and the voltage regulator is put in standby. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are not latched at the pin as in stop2. Instead they are maintained by virtue of the states of the internal logic driving the pins being maintained.

Exit from stop3 is done by asserting $\overline{\text{RESET}}$, any asynchronous interrupt pin that has been enabled, or through the real-time interrupt. The asynchronous interrupt pins are the IRQ or KBI1 and KBI2 pins.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, then the MCU will be reset and operation will resume after taking the reset vector. Exit by means of an asynchronous interrupt or the real-time interrupt will result in the MCU taking the appropriate interrupt vector.

A separate self-clocked source (≈1 kHz) for the real-time interrupt allows a wakeup from stop2 or stop3 mode with no external components. When RTIS2:RTIS1:RTIS0 = 0:0:0, the real-time interrupt function and this 1-kHz source are disabled. Power consumption is lower when the 1-kHz source is disabled, but in that case the real-time interrupt cannot wake the MCU from stop.

Figure 4-2. Reset and Interrupt Vectors

Vector Number	Address (High/Low)	Vector	Vector Name
16 through 31	$FFC0:FFC1 ⇕ $FFDE:FFDF	Unused Vector Space (available for user program)	
15	$FFE0:FFE1	SPI[1]	Vspi1
14	$FFE2:FFE3	RTI	Vrti
13	$FFE4:FFE5	KBI2	Vkeyboard2
12	$FFE6:FFE7	KBI1	Vkeyboard1
11	$FFE8:FFE9	ACMP[2]	Vacmp1
10	$FFEA:FFEB	CMT	Vcmt
9	$FFEC:FFED	SCI Transmit[3]	Vsci1tx
8	$FFEE:FFEF	SCI Receive[3]	Vsci1rx
7	$FFF0:FFF1	SCI Error[3]	Vsci1err
6	$FFF2:FFF3	TPM Overflow	Vtpm1ovf
5	$FFF4:FFF5	TPM Channel 1	Vtpm1ch1
4	$FFF6:FFF7	TPM Channel 0	Vtpm1ch0
3	$FFF8:FFF9	IRQ	Virq
2	$FFFA:FFFB	Low Voltage Detect	Vlvd
1	$FFFC:FFFD	SWI	Vswi
0	$FFFE:FFFF	Reset	Vreset

1. The SPI module is not included on the MC9S08RC/RD/RE devices. This vector location is unused for those devices.
2. The analog comparator (ACMP) module is not included on the MC9S08RD devices. This vector location is unused for those devices.
3. The SCI module is not included on the MC9S08RC devices. This vector location is unused for those devices.

- Writing to a FLASH address before the internal FLASH clock frequency has been set by writing to the FCDIV register
- Writing to a FLASH address while FCBEF is not set (A new command cannot be started until the command buffer is empty.)
- Writing a second time to a FLASH address before launching the previous command (There is only one write to FLASH for every command.)
- Writing a second time to FCMD before launching the previous command (There is only one write to FCMD for every command.)
- Writing to any FLASH control register other than FCMD after writing to a FLASH address
- Writing any command code other than the five allowed codes ($05, $20, $25, $40, or $41) to FCMD
- Accessing (read or write) any FLASH control register other than the write to FSTAT (to clear FCBEF and launch the command) after writing the command to FCMD
- The MCU enters stop mode while a program or erase command is in progress (The command is aborted.)
- Writing the byte program, burst program, or page erase command code ($20, $25, or $40) with a background debug command while the MCU is secured (The background debug controller can only do blank check and mass erase commands when the MCU is secure.)
- Writing 0 to FCBEF to cancel a partial command

4.4.6 FLASH Block Protection

Block protection prevents program or erase changes for FLASH memory locations in a designated address range. Mass erase is disabled when any block of FLASH is protected. The MC9S08RC/RD/RE/RG allows a block of memory at the end of FLASH, and/or the entire FLASH memory to be block protected. A disable control bit and a 3-bit control field, for each of the blocks, allows the user to independently set the size of these blocks. A separate control bit allows block protection of the entire FLASH memory array. All seven of these control bits are located in the FPROT register (see Section 4.6.4, “FLASH Protection Register (FPROT and NVPROT)“).

At reset, the high-page register (FPROT) is loaded with the contents of the NVPROT location that is in the nonvolatile register block of the FLASH memory. The value in FPROT cannot be changed directly from application software so a runaway program cannot alter the block protection settings. If the last 512 bytes of FLASH (which includes the NVPROT register) is protected, the application program cannot alter the block protection settings (intentionally or unintentionally). The FPROT control bits can be written by background debug commands to allow a way to erase a protected FLASH memory.

One use for block protection is to block protect an area of FLASH memory for a bootloader program. This bootloader program then can be used to erase the rest of the FLASH memory and reprogram it. Because the bootloader is protected, it remains intact even if MCU power is lost during an erase and reprogram operation.

6.6.3 Port C Registers (PTCD, PTCPE, and PTCDD)

Port C pins used as general-purpose I/O pins are controlled by the port C data (PTCD), data direction (PTCDD), and pullup enable (PTCPE) registers.

	7	6	5	4	3	2	1	0
R W	PTCD7	PTCD6	PTCD5	PTCD4	PTCD3	PTCD2	PTCD1	PTCD0
Reset	0	0	0	0	0	0	0	0

Figure 6-12. Port C Data Register (PTCD)

Table 6-7. PTCD Field Descriptions

Field	Description
7:0 PTCD[7:0]	**Port C Data Register Bits** — For port C pins that are inputs, reads return the logic level on the pin. For port C pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTCD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

	7	6	5	4	3	2	1	0
R W	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
Reset	0	0	0	0	0	0	0	0

Figure 6-13. Pullup Enable for Port C (PTCPE)

Table 6-8. PTCPE Field Descriptions

Field	Description
7:0 PTCPE[7:0]	**Pullup Enable for Port C Bits** — For port C pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled. For port C pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled. 0 Internal pullup device disabled. 1 Internal pullup device enabled.

	7	6	5	4	3	2	1	0
R W	PTEDD7	PTEDD6	PTEDD5	PTEDD4	PTEDD3	PTEDD2	PTEDD1	PTEDD0
Reset	0	0	0	0	0	0	0	0

Figure 6-20. Data Direction for Port E (PTEDD)

Table 6-15. PTEDD Field Descriptions

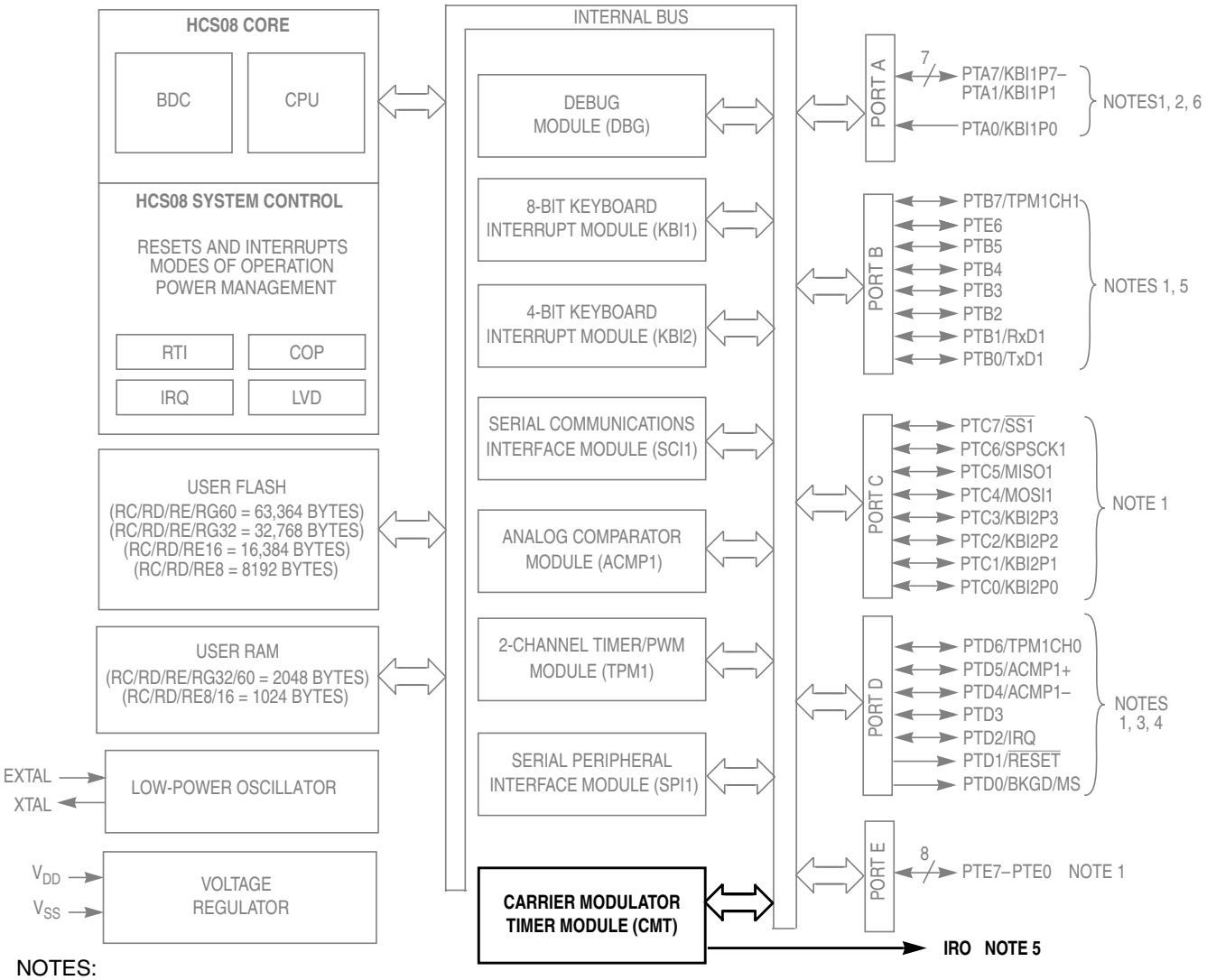
Field	Description
7:0 PTEDD[7:0]	**Data Direction for Port E Bits** — These read/write bits control the direction of port E pins and what is read for PTED reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port E bit n and PTED reads return the contents of PTEDn.

Table 7-2. HCS08 Instruction Set Summary (Sheet 3 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles[1]
			V	H	I	N	Z	C				
BRCLR *n,opr8a,rel*	Branch if Bit *n* in Memory Clear	Branch if (Mn) = 0	–	–	–	–	–		DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	Uses 3 Bus Cycles	–	–	–	–	–	–	REL	21	rr	3
BRSET *n,opr8a,rel*	Branch if Bit *n* in Memory Set	Branch if (Mn) = 1	–	–	–	–	–		DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n,opr8a*	Set Bit *n* in Memory	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 0x0002 push (PCL); SP ← (SP) – 0x0001 push (PCH); SP ← (SP) – 0x0001 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	5
CBEQ *oprx8,rel* CBEQA *#opr8i,rel* CBEQX *#opr8i,rel* CBEQ *oprx8*,X+,*rel* CBEQ ,X+,*rel* CBEQ *oprx8*,SP,*rel*	Compare and Branch if Equal	Branch if (A) = (M) Branch if (A) = (M) Branch if (X) = (M) Branch if (A) = (M) Branch if (A) = (M) Branch if (A) = (M)	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 5 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask Bit	I ← 0	–	–	0	–	–	–	INH	9A		1
CLR *oprx8*,X CLR ,X CLR *oprx8*,SP	Clear	M ← 0x00 A ← 0x00 X ← 0x00 H ← 0x00 M ← 0x00 M ← 0x00 M ← 0x00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	5 1 1 1 5 4 6
CMP *#opr8i* CMP *opr8a* CMP *opr16a* CMP *oprx16*,X CMP *oprx8*,X CMP ,X CMP *oprx16*,SP CMP *oprx8*,SP	Compare Accumulator with Memory	(A) – (M) (CCR Updated But Operands Not Changed)		–	–				IMM DIR EXT IX2 IX1 IX SP2 SP1	A1 B1 C1 D1 E1 F1 9ED1 9EE1	ii dd hh ll ee ff ff ee ff ff	2 3 4 4 3 3 5 4
COM *oprx8*,X COM ,X COM *oprx8*,SP	Complement (One's Complement)	M ← (M)= 0xFF – (M) A ← (A) = 0xFF – (A) X ← (X) = 0xFF – (X) M ← (M) = 0xFF – (M) M ← (M) = 0xFF – (M) M ← (M) = 0xFF – (M)	0	–	–			1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	5 1 1 5 4 6
CPHX *opr16a* CPHX *#opr16i* CPHX *opr8a* CPHX *oprx8*,SP	Compare Index Register (H:X) with Memory	(H:X) – (M:M + 0x0001) (CCR Updated But Operands Not Changed)		–	–				EXT IMM DIR SP1	3E 65 75 9EF3	hh ll jj kk dd ff	6 3 5 6

Chapter 8
Carrier Modulator Timer (S08CMTV1)

8.1 Introduction



NOTES:
1. Port pins are software configurable with pullup device if input port
2. PTA0 does not have a clamp diode to VDD. PTA0 should not be driven above VDD. Also, PTA0 does not pullup to VDD when internal pullup is enabled.
3. IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)
4. The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 8-1. MC9S08RC/RD/RE/RG Block Diagram

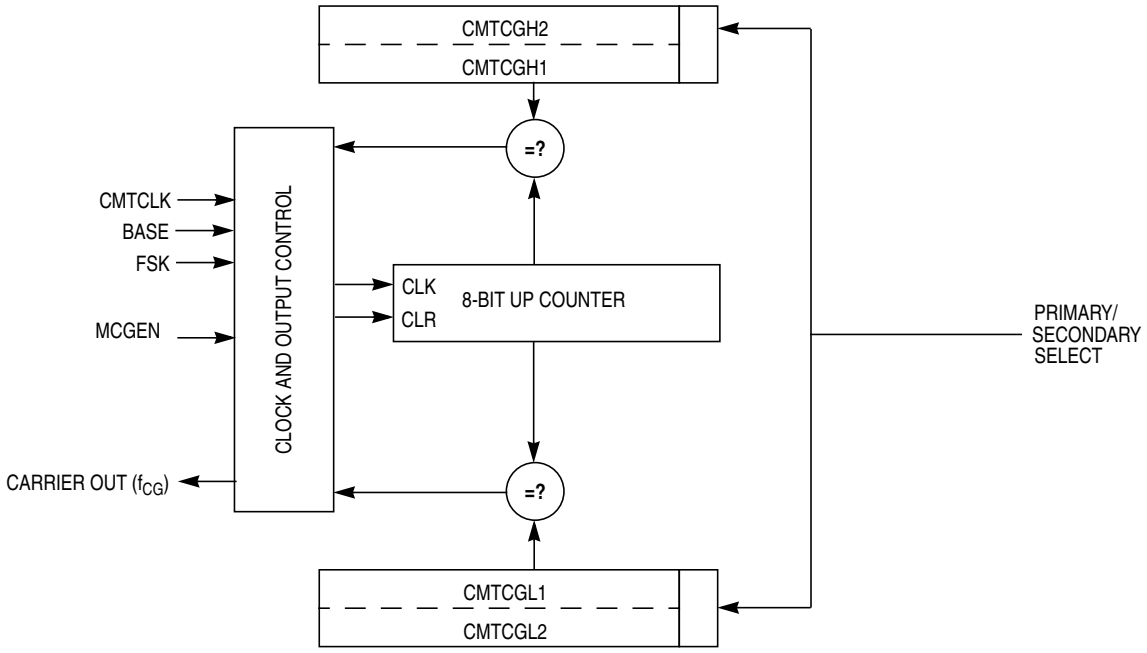


Figure 8-3. Carrier Generator Block Diagram

The high/low time counter is an 8-bit up counter. After each increment, the contents of the counter are compared with the appropriate high or low count value register. When the compare value is reached, the counter is reset to a value of $01, and the compare is redirected to the other count value register.

Assuming that the high time count compare register is currently active, a valid compare will cause the carrier output to be driven low. The counter will continue to increment (starting at reset value of $01). When the value stored in the selected low count value register is reached, the counter will again be reset and the carrier output will be driven high.

The cycle repeats, automatically generating a periodic signal that is directed to the modulator. The lowest frequency (maximum period) and highest frequency (minimum period) that can be generated are defined as:

$$f_{max} = f_{CMTCLK} \div (2 \times 1) \text{ Hz} \qquad \textit{Eqn. 8-1}$$

$$f_{min} = f_{CMTCLK} \div (2 \times (2^8 - 1)) \text{ Hz} \qquad \textit{Eqn. 8-2}$$

In the general case, the carrier generator output frequency is:

$$f_{CG} = f_{CMTCLK} \div (\text{Highcount} + \text{Lowcount}) \text{ Hz} \qquad \textit{Eqn. 8-3}$$

Where: $0 < \textit{Highcount} < 256$ and
$0 < \textit{Lowcount} < 256$

Table 10-2. TPM Clock Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
0:0	No clock selected (TPM disabled)
0:1	Bus rate clock (BUSCLK)
1:0	Fixed system clock (XCLK)
1:1	External source (TPM1 Ext Clk)[1,2]

1. The maximum frequency that is allowed as an external clock is one-fourth of the bus frequency.
2. When the TPM1CH0 pin is selected as the TPM clock source, the corresponding ELS0B:ELS0A control bits should be set to 0:0 so channel 0 does not try to use the same pin for a conflicting function.

Table 10-3. Prescale Divisor Selection

PS2:PS1:PS0	TPM Clock Source Divided-By
0:0:0	1
0:0:1	2
0:1:0	4
0:1:1	8
1:0:0	16
1:0:1	32
1:1:0	64
1:1:1	128

10.7.2 Timer Counter Registers (TPM1CNTH:TPM1CNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPM1CNTH or TPM1CNTL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This allows coherent 16-bit reads in either order. The coherency mechanism is automatically restarted by an MCU reset, a write of any value to TPM1CNTH or TPM1CNTL, or any write to the timer status/control register (TPM1SC).

Reset clears the TPM counter registers.

	7	6	5	4	3	2	1	0
R	Bit 15	14	13	12	11	10	9	Bit 8
W	Any write to TPM1CNTH clears the 16-bit counter.							
Reset	0	0	0	0	0	0	0	0

Figure 10-6. Timer Counter Register High (TPM1CNTH)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	Any write to TPM1CNTL clears the 16-bit counter.							
Reset	0	0	0	0	0	0	0	0

Figure 10-7. Timer Counter Register Low (TPM1CNTL)

12.2.5 SCI Status Register 2 (SCI1S2)

This register has one read-only status flag. Writes have no effect.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RAF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-8. SCI Status Register 2 (SCI1S2)

Table 12-6. SCI1S2 Register Field Descriptions

Field	Description
0 RAF	**Receiver Active Flag** — RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

12.2.6 SCI Control Register 3 (SCI1C3)

	7	6	5	4	3	2	1	0
R	R8	T8	TXDIR	0	ORIE	NEIE	FEIE	PEIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-9. SCI Control Register 3 (SCI1C3)

Table 12-7. SCI1C3 Register Field Descriptions

Field	Description
7 R8	**Ninth Data Bit for Receiver** — When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the MSB of the buffered data in the SCI1D register. When reading 9-bit data, read R8 before reading SCI1D because reading SCI1D completes automatic flag clearing sequences which could allow R8 and SCI1D to be overwritten with new data.
6 T8	**Ninth Data Bit for Transmitter** — When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the MSB of the data in the SCI1D register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCI1D is written so T8 should be written (if it needs to change from its previous value) before SCI1D is written. If T8 does not need to change in the new value (such as when it is used to generate mark or space parity), it need not be written each time SCI1D is written.
5 TXDIR	**TxD Pin Direction in Single-Wire Mode** — When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.

13.3.1 SPI Clock Formats

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the SPI system has a clock polarity (CPOL) bit and a clock phase (CPHA) control bit to select one of four clock formats for data transfers. CPOL selectively inserts an inverter in series with the clock. CPHA chooses between two different clock phase relationships between the clock and data.

Figure 13-5 shows the clock formats when CPHA = 1. At the top of the figure, the eight bit times are shown for reference with bit 1 starting at the first SPSCK edge and bit 8 ending one-half SPSCK cycle after the sixteenth SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

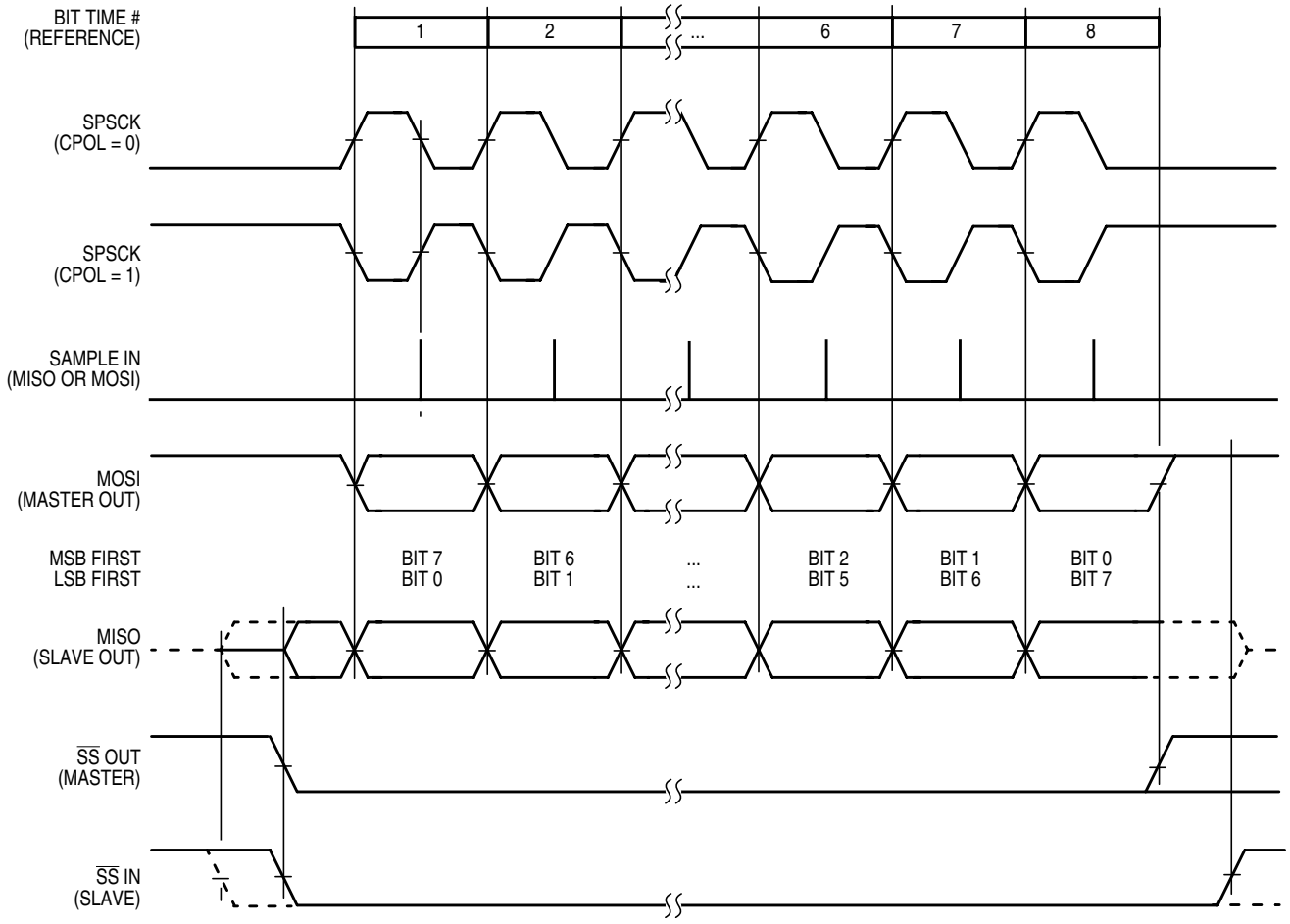


Figure 13-5. SPI Clock Formats (CPHA = 1)

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to Section 15.2.2, "Communication Details."

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Section 15.2.2, "Communication Details," for more detail.

When no debugger pod is connected to the 6-pin BDM interface connector, the internal pullup on BKGD chooses normal operating mode. When a development system is connected, it can pull both BKGD and $\overline{\text{RESET}}$ low, release $\overline{\text{RESET}}$ to select active background mode rather than normal operating mode, then release BKGD. It is not necessary to reset the target MCU to communicate with it through the background debug interface.

15.2.2 Communication Details

The BDC serial interface requires the external controller to generate a falling edge on the BKGD pin to indicate the start of each bit time. The external controller provides this falling edge whether data is transmitted or received.

BKGD is a pseudo-open-drain pin that can be driven either by an external controller or by the MCU. Data is transferred MSB first at 16 BDC clock cycles per bit (nominal speed). The interface times out if 512 BDC clock cycles occur between falling edges from the host. Any BDC command that was in progress when this timeout occurs is aborted without affecting the memory or operating mode of the target MCU system.

The custom serial protocol requires the debug pod to know the target BDC communication clock speed.

The clock switch (CLKSW) control bit in the BDC status and control register allows the user to select the BDC clock source. The BDC clock source can either be the bus or the alternate BDC clock source.

The BKGD pin can receive a high or low level or transmit a high or low level. The following diagrams show timing for each of these cases. Interface timing is synchronous to clocks in the target BDC, but asynchronous to the external host. The internal BDC clock signal is shown for reference in counting cycles.

The SYNC command is unlike other BDC commands because the host does not necessarily know the correct communications speed to use for BDC communications until after it has analyzed the response to the SYNC command.

To issue a SYNC command, the host:

- Drives the BKGD pin low for at least 128 cycles of the slowest possible BDC clock (The slowest clock is normally the reference oscillator/64 or the self-clocked rate/64.)
- Drives BKGD high for a brief speedup pulse to get a fast rise time (This speedup pulse is typically one cycle of the fastest clock in the system.)
- Removes all drive to the BKGD pin so it reverts to high impedance
- Monitors the BKGD pin for the sync response pulse

The target, upon detecting the SYNC request from the host (which is a much longer low time than would ever occur during normal BDC communications):

- Waits for BKGD to return to a logic high
- Delays 16 cycles to allow the host to stop driving the high speedup pulse
- Drives BKGD low for 128 BDC clock cycles
- Drives a 1-cycle high speedup pulse to force a fast rise time on BKGD
- Removes all drive to the BKGD pin so it reverts to high impedance

The host measures the low time of this 128-cycle sync response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

15.2.4 BDC Hardware Breakpoint

The BDC includes one relatively simple hardware breakpoint that compares the CPU address bus to a 16-bit match value in the BDCBKPT register. This breakpoint can generate a forced breakpoint or a tagged breakpoint. A forced breakpoint causes the CPU to enter active background mode at the first instruction boundary following any access to the breakpoint address. The tagged breakpoint causes the instruction opcode at the breakpoint address to be tagged so that the CPU will enter active background mode rather than executing that instruction if and when it reaches the end of the instruction queue. This implies that tagged breakpoints can only be placed at the address of an instruction opcode while forced breakpoints can be set at any address.

The breakpoint enable (BKPTEN) control bit in the BDC status and control register (BDCSCR) is used to enable the breakpoint logic (BKPTEN = 1). When BKPTEN = 0, its default value after reset, the breakpoint logic is disabled and no BDC breakpoints are requested regardless of the values in other BDC breakpoint registers and control bits. The force/tag select (FTS) control bit in BDCSCR is used to select forced (FTS = 1) or tagged (FTS = 0) type breakpoints.

The on-chip debug module (DBG) includes circuitry for two additional hardware breakpoints that are more flexible than the simple breakpoint in the BDC module.

15.4.3.9 Debug Status Register (DBGS)

This is a read-only status register.

	7	6	5	4	3	2	1	0
R	AF	BF	ARMF	0	CNT3	CNT2	CNT1	CNT0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-9. Debug Status Register (DBGS)

Table 15-6. DBGS Register Field Descriptions

Field	Description
7 AF	**Trigger Match A Flag** — AF is cleared at the start of a debug run and indicates whether a trigger match A condition was met since arming. 0 Comparator A has not matched 1 Comparator A match
6 BF	**Trigger Match B Flag** — BF is cleared at the start of a debug run and indicates whether a trigger match B condition was met since arming. 0 Comparator B has not matched 1 Comparator B match
5 ARMF	**Arm Flag** — While DBGEN = 1, this status bit is a read-only image of ARM in DBGC. This bit is set by writing 1 to the ARM control bit in DBGC (while DBGEN = 1) and is automatically cleared at the end of a debug run. A debug run is completed when the FIFO is full (begin trace) or when a trigger event is detected (end trace). A debug run can also be ended manually by writing 0 to ARM or DBGEN in DBGC. 0 Debugger not armed 1 Debugger armed
3:0 CNT[3:0]	**FIFO Valid Count** — These bits are cleared at the start of a debug run and indicate the number of words of valid data in the FIFO at the end of a debug run. The value in CNT does not decrement as data is read out of the FIFO. The external debug host is responsible for keeping track of the count as information is read out of the FIFO. 0000 Number of valid words in FIFO = No valid data 0001 Number of valid words in FIFO = 1 0010 Number of valid words in FIFO = 2 0011 Number of valid words in FIFO = 3 0100 Number of valid words in FIFO = 4 0101 Number of valid words in FIFO = 5 0110 Number of valid words in FIFO = 6 0111 Number of valid words in FIFO = 7 1000 Number of valid words in FIFO = 8

Table A-5. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Maximum low-voltage safe state re-arm[3]	V_{REARM}	—	—	3.0	V
Input high voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IH}	0.70 × V_{DD}		—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}		—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—		0.35 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—		0.30 × V_{DD}	V
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}		—	V
Input leakage current (Per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	$\lvert I_{In}\rvert$	—	0.025	1.0	µA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	$\lvert I_{OZ}\rvert$	—	0.025	1.0	µA
Internal pullup resistors[4] [5]	R_{PU}	17.5		52.5	κW
Internal pulldown resistor (IRQ)	R_{PD}	17.5		52.5	κW
Output high voltage (V_{DD} ≥ 1.8 V) I_{OH} = –2 mA (ports A, C, D and E)	V_{OH}	V_{DD} – 0.5		—	V
Output high voltage (port B and IRO) I_{OH} = –10 mA (V_{DD} ≥ 2.7 V) I_{OH} = –6 mA (V_{DD} ≥ 2.3 V) I_{OH} = –3 mA (V_{DD} ≥ 1.8 V)		V_{DD} – 0.5		— — —	
Maximum total I_{OH} for all port pins	$\lvert I_{OHT}\rvert$	—		60	mA
Output low voltage (V_{DD} ≥ 1.8 V) I_{OL} = 2.0 mA (ports A, C, D and E)	V_{OL}	—		0.5	V
Output low voltage (port B) I_{OL} = 10.0 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		0.5 0.5 0.5	
Output low voltage (IRO) I_{OL} = 16 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —		1.2 1.2 1.2	
Maximum total I_{OL} for all port pins	I_{OLT}	—		60	mA
dc injection current[2], [6], [7], [8],, [9] V_{IN} < V_{SS}, V_{IN} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins	$\lvert I_{IC}\rvert$	 — —		 0.2 5	 mA mA
Input capacitance (all non-supply pins)	C_{In}	—		7	pF

1. RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.
2. This parameter is characterized and not tested on each device.
3. If SAFE bit is set, V_{DD} must be above re-arm voltage to allow MCU to accept interrupts, refer to Section 5.6, “Low-Voltage Detect (LVD) System.”
4. Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.
5. The PTA0 pullup resistor may not pull up to the specified minimum V_{IH}. However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no dc load is present on the pin.
6. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.