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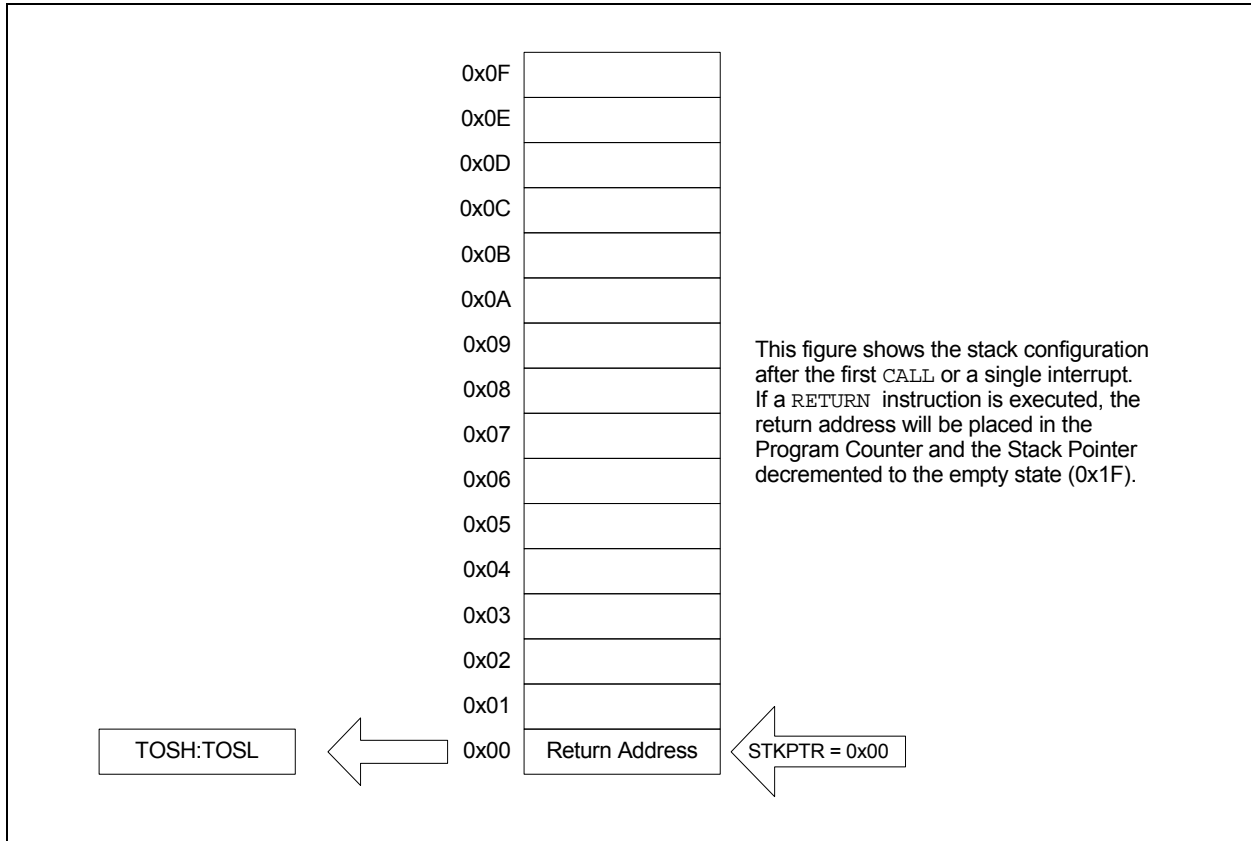
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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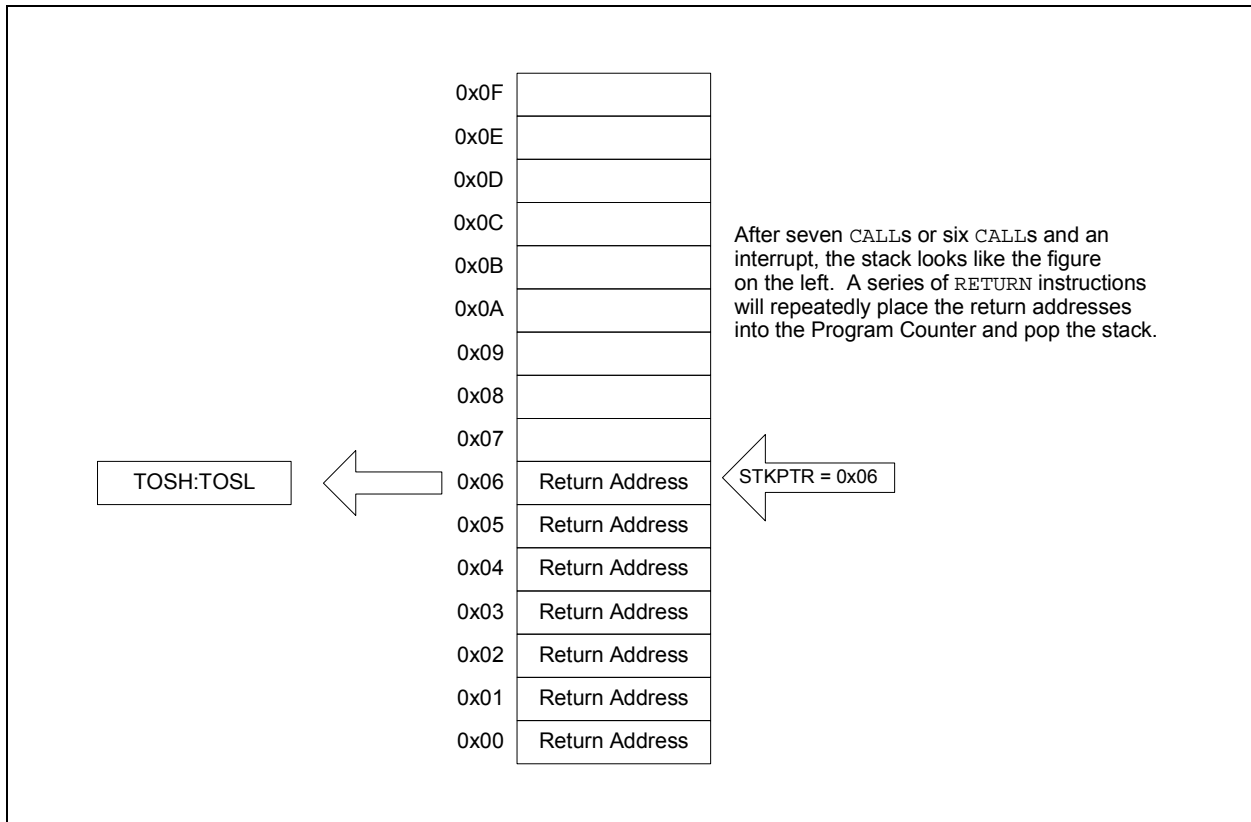
#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f1708-i-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic16f1708-i-ss</a>

**FIGURE 3-5: ACCESSING THE STACK EXAMPLE 2**



**FIGURE 3-6: ACCESSING THE STACK EXAMPLE 3**



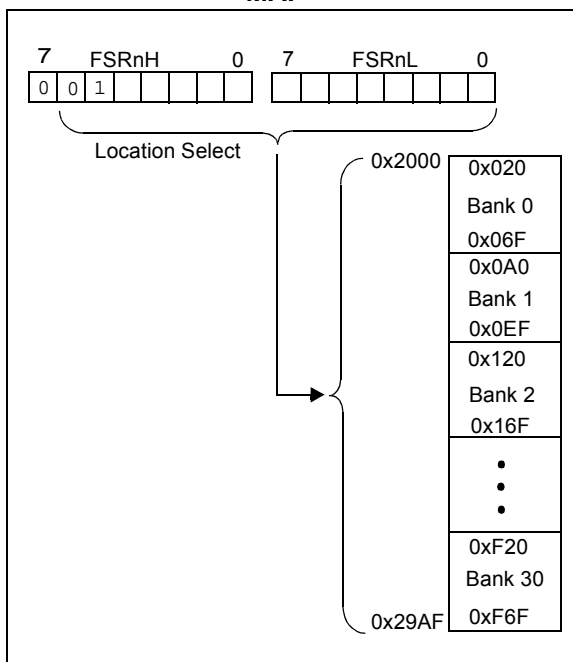
## 3.7.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

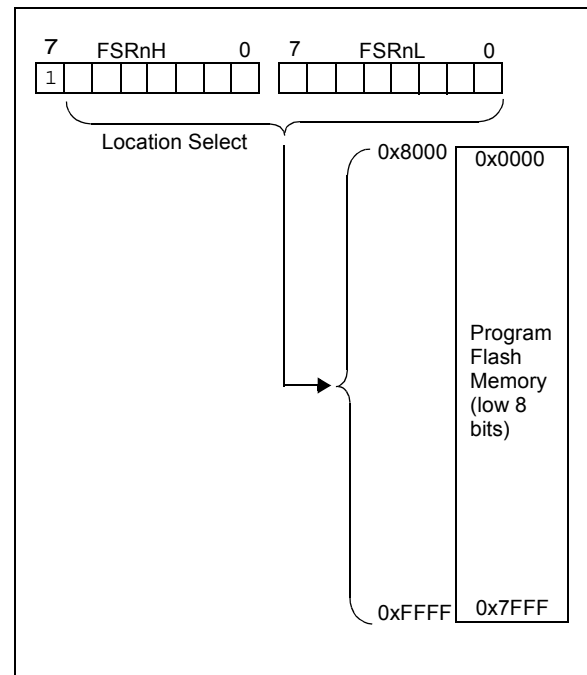
**FIGURE 3-10: LINEAR DATA MEMORY MAP**



## 3.7.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire Program Flash Memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower eight bits of each memory location is accessible via INDF. Writing to the Program Flash Memory cannot be accomplished via the FSR/INDF interface. All instructions that access Program Flash Memory via the FSR/INDF interface will require one additional instruction cycle to complete.

**FIGURE 3-11: PROGRAM FLASH MEMORY MAP**



# PIC16(L)F1704/8

## 8.1.1 WAKE-UP USING INTERRUPTS

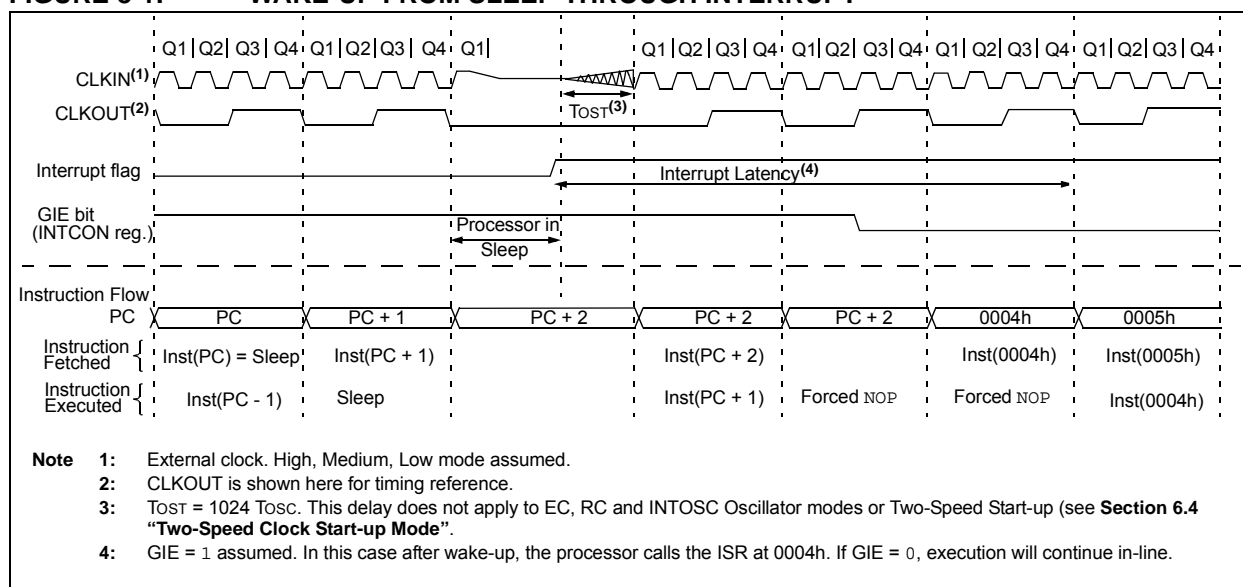
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a **SLEEP** instruction
  - **SLEEP** instruction will execute as a NOP
  - WDT and WDT prescaler will not be cleared
  - $\overline{TO}$  bit of the STATUS register will not be set
  - $\overline{PD}$  bit of the STATUS register will not be cleared

- If the interrupt occurs **during or after** the execution of a **SLEEP** instruction
  - **SLEEP** instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - $\overline{TO}$  bit of the STATUS register will be set
  - $\overline{PD}$  bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a **SLEEP** instruction, it may be possible for flag bits to become set before the **SLEEP** instruction completes. To determine whether a **SLEEP** instruction executed, test the  $\overline{PD}$  bit. If the  $\overline{PD}$  bit is set, the **SLEEP** instruction was executed as a NOP.

**FIGURE 8-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT**



## 11.1.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA register. Digital output functions may continue to control the pin when it is in Analog mode.

# PIC16(L)F1704/8

## REGISTER 11-12: ANSELB: PORTB ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
—	—	ANSB5	ANSB4	—	—	—	—
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **ANSB<5:4>:** Analog Select between Analog or Digital Function on pins RB<5:4>, respectively  
0 = Digital I/O. Pin is assigned to port or digital special function.  
1 = Analog input. Pin is assigned as analog input<sup>(1)</sup>. Digital input buffer disabled.

bit 3-0 **Unimplemented:** Read as '0'

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

## REGISTER 11-13: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **WPUB<7:4>:** Weak Pull-up Register bits  
1 = Pull-up enabled  
0 = Pull-up disabled

bit 3-0 **Unimplemented:** Read as '0'

**Note 1:** Global WPUEN bit of the OPTION\_REG register must be cleared for individual pull-ups to be enabled.  
**2:** The weak pull-up device is automatically disabled if the pin is configured as an output.

## 11.5 PORTC Registers

### 11.5.1 DATA REGISTER

PORTC is a 6-bit wide bidirectional port in the PIC16(L)F1704 device and 8-bit wide bidirectional port in the PIC16(L)F1708 device. The corresponding data direction register is TRISC (Register 11-18). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTC register (Register 11-17) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATC).

### 11.5.2 DIRECTION CONTROL

The TRISC register (Register 11-18) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

### 11.5.3 INPUT THRESHOLD CONTROL

The INLVLC register (Register 11-24) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 32-4: I/O Ports for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

### 11.5.4 OPEN-DRAIN CONTROL

The ODCONC register (Register 11-22) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONC bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONC bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

### 11.5.5 SLEW RATE CONTROL

The SLRCONC register (Register 11-23) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONC bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONC bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

### 11.5.6 ANALOG CONTROL

The ANSEL register (Register 11-20) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

**Note:** The ANSEL bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

### 11.5.7 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSEL register. Digital output functions may continue to control the pin when it is in Analog mode.

# PIC16(L)F1704/8

## REGISTER 11-22: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODC7 <sup>(1)</sup>	ODC6 <sup>(1)</sup>	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0                      **ODC<7:0>:** PORTC Open-Drain Enable bits<sup>(1)</sup>  
For RC<7:0> pins, respectively  
1 = Port pin operates as open-drain drive (sink current only)  
0 = Port pin operates as standard push-pull drive (source and sink current)

**Note 1:** ODC<7:6> are available on PIC16(L)F1708 only.

## REGISTER 11-23: SLRCONC: PORTC SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRC7 <sup>(1)</sup>	SLRC6 <sup>(1)</sup>	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0                      **SLRC<7:0>:** PORTC Slew Rate Enable bits<sup>(1)</sup>  
For RC<7:0> pins, respectively  
1 = Port pin slew rate is limited  
0 = Port pin slews at maximum rate

**Note 1:** SLRC<7:6> are available on PIC16(L)F1708 only.

## REGISTER 11-24: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLC7 <sup>(1)</sup>	INLVLC6 <sup>(1)</sup>	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

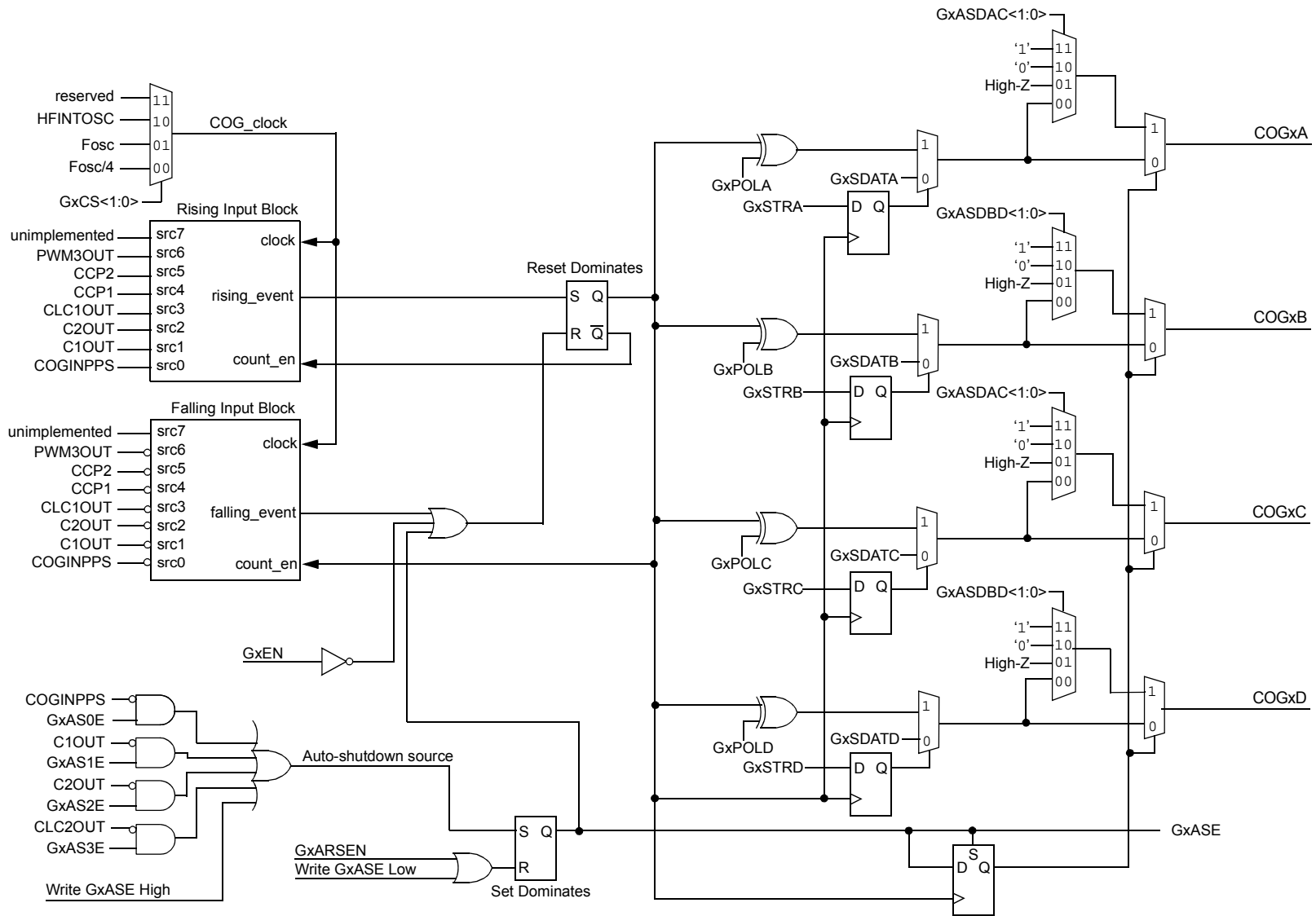
### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

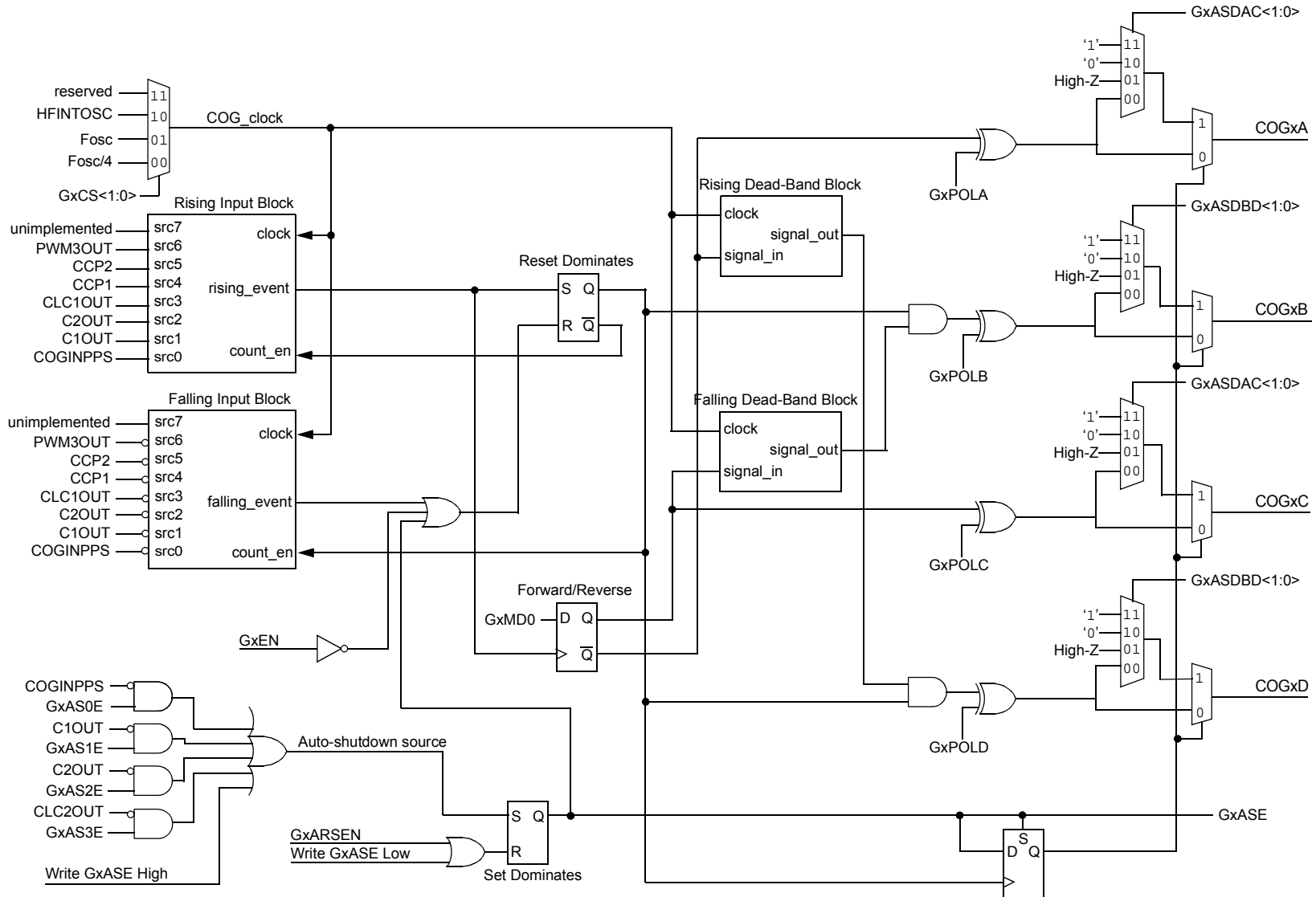
bit 7-0                      **INLVLC<7:0>:** PORTC Input Level Select bits<sup>(1)</sup>  
For RC<7:0> pins, respectively  
1 = ST input used for PORT reads and interrupt-on-change  
0 = TTL input used for PORT reads and interrupt-on-change

**Note 1:** INLVLC<7:6> are available on PIC16(L)F1708 only.



**FIGURE 18-3: SIMPLIFIED COG BLOCK DIAGRAM (SYNCHRONOUS STEERED PWM MODE, GXMD = 1)**

**FIGURE 18-4: SIMPLIFIED COG BLOCK DIAGRAM (FULL-BRIDGE MODES, FORWARD: GXMD = 2, REVERSE: GXMD = 3)**



## 18.9 Buffer Updates

Changes to the phase, dead band, and blanking count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the GxLD bit of the COGxCON0 register and double buffering of the phase, blanking, and dead-band count registers.

Before the COG module is enabled, writing the count registers loads the count buffers without need of the GxLD bit. However, when the COG is enabled, the count buffer updates are suspended after writing the count registers until after the GxLD bit is set. When the GxLD bit is set, the phase, dead-band, and blanking register values are transferred to the corresponding buffers synchronous with COG operation. The GxLD bit is cleared by hardware when the transfer is complete.

## 18.10 Input and Output Pin Selection

The COG has one selection for an input from a device pin. That one input can be used as rising and falling event source or a fault source. The COG1PPS register is used to select the pin. Refer to Register 12-1 and Register 12-2.

The pin PPS control registers are used to enable the COG outputs. Any combination of outputs to pins is possible including multiple pins for the same output. See the RxyPPS control register and **Section 12.2 “PPS Outputs”** for more details.

## 18.11 Operation During Sleep

The COG continues to operate in Sleep provided that the COG\_clock, rising event, and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG\_clock source.

## 18.12 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

1. If a pin is to be used for the COG fault or event input, use the COGxPPS register to configure the desired pin.
2. Clear all ANSEL register bits associated with pins that are used for COG functions.
3. Ensure that the TRIS control bits corresponding to the COG outputs to be used are set so that all are configured as inputs. The COG module will enable the output drivers as needed later.
4. Clear the GxEN bit, if not already cleared.
5. Set desired dead-band times with the COGxDBR and COGxDBF registers and select the source with the COGxRDBS and COGxFDBS bits of the COGxCON1 register.
6. Set desired blanking times with the COGxBLKR and COGxBLKF registers.
7. Set desired phase delay with the COGxPHR and COGxPHF registers.
8. Select the desired shutdown sources with the COGxASD1 register.
9. Setup the following controls in COGxASD0 auto-shutdown register:
  - Select both output override controls to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
  - Set the GxASE bit and clear the GxARSEN bit.
10. Select the desired rising and falling event sources with the COGxRIS and COGxFIS registers.
11. Select the desired rising and falling event modes with the COGxRSIM and COGxFSIM registers.
12. Configure the following controls in the COGxCON1 register:
  - Select the desired clock source
  - Select the desired dead-band timing sources
13. Configure the following controls in the COGxSTR register:
  - Set the steering bits of the outputs to be used.
  - Set the static levels.
14. Set the polarity controls in the COGxCON1 register.
15. Set the GxEN bit.
16. Set the pin PPS controls to direct the COG outputs to the desired pins.
17. If auto-restart is to be used, set the GxARSEN bit and the GxASE will be cleared automatically. Otherwise, clear the GxASE bit to start the COG.

The pull-up and pull-down resistor values are significantly affected by small variations of ZCPINV. Measuring ZCPINV can be difficult, especially when the waveform is relative to VDD. However, by combining Equations 23-2 and 23-3, the resistor value can be determined from the time difference between the ZCDx\_output high and low periods. Note that the time difference,  $\Delta T$ , is  $4 \cdot T_{OFFSET}$ . The equation for determining the pull-up and pull-down resistor values from the high and low ZCDx\_output periods is shown in Equation 23-4. The ZCDx\_output signal can be directly observed on a pin by routing the ZCDx\_output signal through one of the CLCs.

**EQUATION 23-4:**

$$R = R_{SERIES} \left( \frac{V_{BIAS}}{V_{PEAK} \left( \sin \left( \pi Freq \frac{(\Delta T)}{2} \right) \right)} - 1 \right)$$

R is pull-up or pull-down resistor.

VBIAS is VPULLUP when R is pull-up or VDD when R is pull-down.

$\Delta T$  is the ZCDOUT high and low period difference.

## 23.6 Handling VPEAK Variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of  $\pm 600 \mu A$  and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed  $\pm 600 \mu A$  and the minimum is at least  $\pm 100 \mu A$ , compute the series resistance as shown in Equation 23-5. The compensating pull-up for this series resistance can be determined with Equation 23-3 because the pull-up value is independent from the peak voltage.

**EQUATION 23-5: SERIES R FOR V RANGE**

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

## 23.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

## 23.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-On-Reset (POR). When the ZCDDIS Configuration bit is cleared, the ZCD circuit will be active at POR. When the ZCDDIS Configuration bit is set, the ZCDxEN bit of the ZCDxCON register must be set to enable the ZCD module.

## 28.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit of the SSPCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

### 28.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 28-7 shows the block diagram of a typical daisy-chain connection when operating in SPI mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPCON3 register will enable writes to the SSPBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

## 28.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The  $\overline{SS}$  pin allows a Synchronous Slave mode. The SPI must be in Slave mode with  $\overline{SS}$  pin control enabled ( $SSPCON1<3:0> = 0100$ ).

When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the SDO pin is driven.

When the  $\overline{SS}$  pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

- |  |
|--|
| <p><b>Note 1:</b> When the SPI is in Slave mode with <math>\overline{SS}</math> pin control enabled (<math>SSPCON1&lt;3:0&gt; = 0100</math>), the SPI module will reset if the <math>\overline{SS}</math> pin is set to VDD.</p> <p><b>2:</b> When the SPI is used in Slave mode with CKE set; the user must enable <math>\overline{SS}</math> pin control.</p> <p><b>3:</b> While operated in SPI Slave mode the SMP bit of the SSPSTAT register must remain clear.</p> |
|--|

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the  $\overline{SS}$  pin to a high level or clearing the SSPEN bit.

# PIC16(L)F1704/8

## 28.6.10 SLEEP OPERATION

While in Sleep mode, the I<sup>2</sup>C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

## 28.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

## 28.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I<sup>2</sup>C bus may be taken when the P bit of the SSPSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

## 28.6.13 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I<sup>2</sup>C port to its Idle state (Figure 28-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a Start condition.

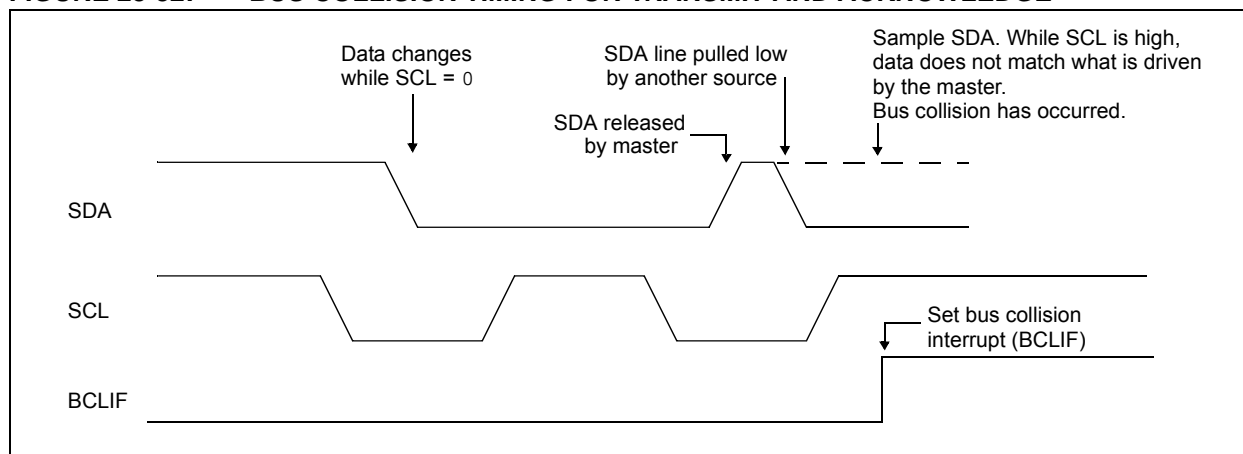
If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I<sup>2</sup>C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is Idle and the S and P bits are cleared.

**FIGURE 28-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE**



## 29.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

**Note:** If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

## 29.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

**Note:** If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

## 29.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters

will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

## 29.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

## 29.5.1.9 Synchronous Master Reception Set-up:

1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

# PIC16(L)F1704/8

**TABLE 32-3: POWER-DOWN CURRENTS (IPD)<sup>(1,2)</sup>**

PIC16LF1704/8			Standard Operating Conditions (unless otherwise stated) Low-Power Sleep Mode					
PIC16F1704/8			Low-Power Sleep Mode, VREGPM = 1					
Param. No.	Device Characteristics	Min.	Typ. <sup>†</sup>	Max. +85°C	Max. +125°C	Units	Conditions	
							VDD	Note
D023	Base IPD	—	0.05	1.0	8.0	μA	1.8	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive
		—	0.08	2.0	9.0	μA	3.0	
D023	Base IPD	—	0.3	3.0	10	μA	2.3	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive, Low-Power Sleep mode
		—	0.4	4.0	12	μA	3.0	
		—	0.5	6.0	15	μA	5.0	
D023A	Base IPD	—	9.8	16	18	μA	2.3	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive, Normal-Power Sleep mode VREGPM = 0
		—	10.3	18	20	μA	3.0	
		—	11.5	21	26	μA	5.0	
D024		—	0.5	6	14	μA	1.8	WDT Current
		—	0.8	7	17	μA	3.0	
D024		—	0.8	6	15	μA	2.3	WDT Current
		—	0.9	7	20	μA	3.0	
		—	1.0	8	22	μA	5.0	
D025		—	15	28	30	μA	1.8	FVR Current
		—	18	30	33	μA	3.0	
D025		—	18	33	35	μA	2.3	FVR Current
		—	19	35	37	μA	3.0	
		—	20	37	39	μA	5.0	
D026		—	7.5	25	28	μA	3.0	BOR Current
D026		—	10	25	28	μA	3.0	BOR Current
		—	12	28	31	μA	5.0	
D027		—	0.5	4	10	μA	3.0	LPBOR Current
D027		—	0.8	6	14	μA	3.0	LPBOR Current
		—	1	8	17	μA	5.0	
D028		—	0.5	5	9	μA	1.8	SOSC Current
		—	0.8	8.5	12	μA	3.0	
D028		—	1.1	6	10	μA	2.3	SOSC Current
		—	1.3	8.5	20	μA	3.0	
		—	1.4	10	25	μA	5.0	
D029		—	0.05	2	9	μA	1.8	ADC Current ( <b>Note 3</b> ), no conversion in progress
		—	0.08	3	10	μA	3.0	
D029		—	0.3	4	12	μA	2.3	ADC Current ( <b>Note 3</b> ), no conversion in progress
		—	0.4	5	13	μA	3.0	
		—	0.5	7	16	μA	5.0	

\* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VSS.
- Note 3:** ADC oscillator source is FRC.



# PIC16(L)F1704/8

**TABLE 32-11: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	μs	
31	TWDTLP	Low-Power Watchdog Timer Time-out Period	10	16	27	ms	3.3V ≤ VDD ≤ 5.0V 1:512 Prescaler used
32	TOST	Oscillator Start-up Timer Period <sup>(1,2)</sup>	—	1024	—	TOSC	
33*	TPWRT	Power-up Timer Period, PWRTE = 0	40	65	140	ms	
34*	TIOZ	I/O high-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage <sup>(3)</sup>	2.55	2.70	2.85	V	BORV = 0
			2.30	2.45	2.60	V	BORV = 1 (PIC16F1704/8)
			1.80	1.90	2.10	V	BORV = 1 (PIC16LF1704/8)
35A	VLPBOR	Low-Power Brown-out <sup>(3)</sup>	1.80	2.1	2.5	V	LPBOR = 1
36*	VHYST	Brown-out Reset Hysteresis <sup>(3)</sup>	0	25	75	mV	-40°C ≤ TA ≤ +85°C
37*	TBORDC	Brown-out Reset DC Response Time	1	3	35	μs	VDD ≤ VBOR

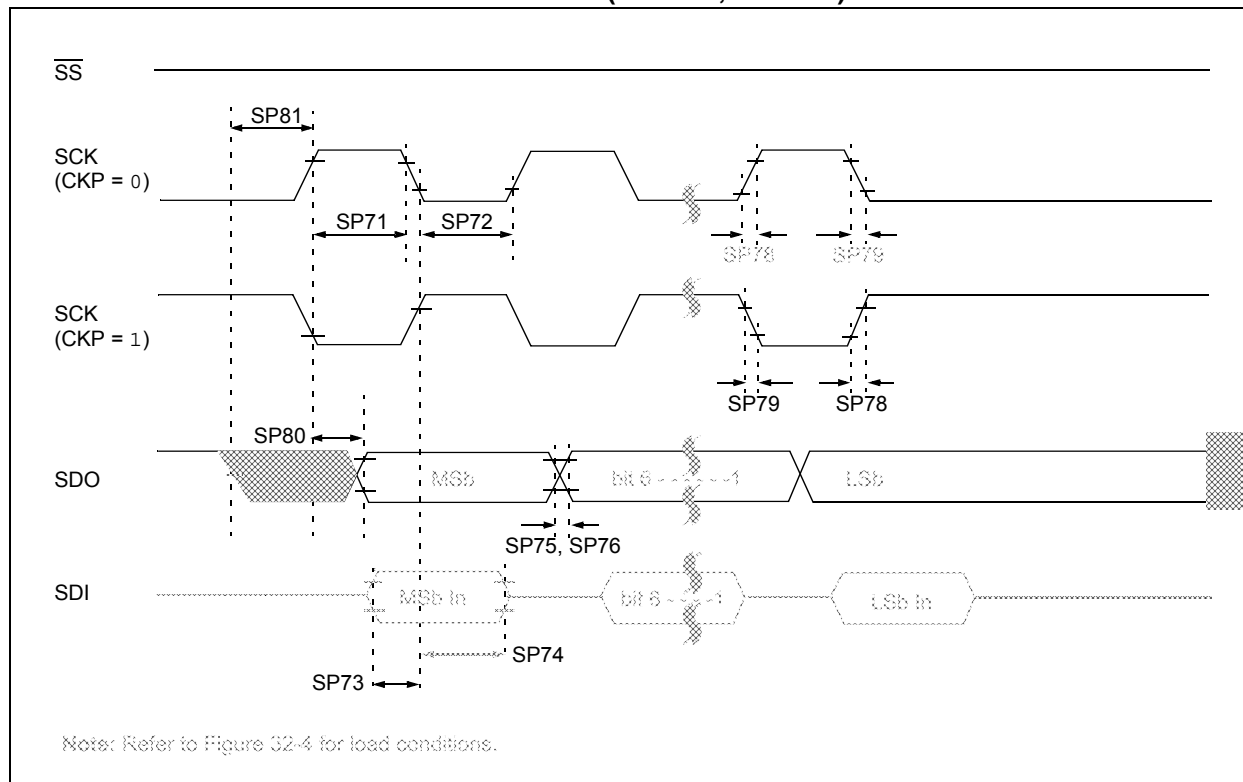
\* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

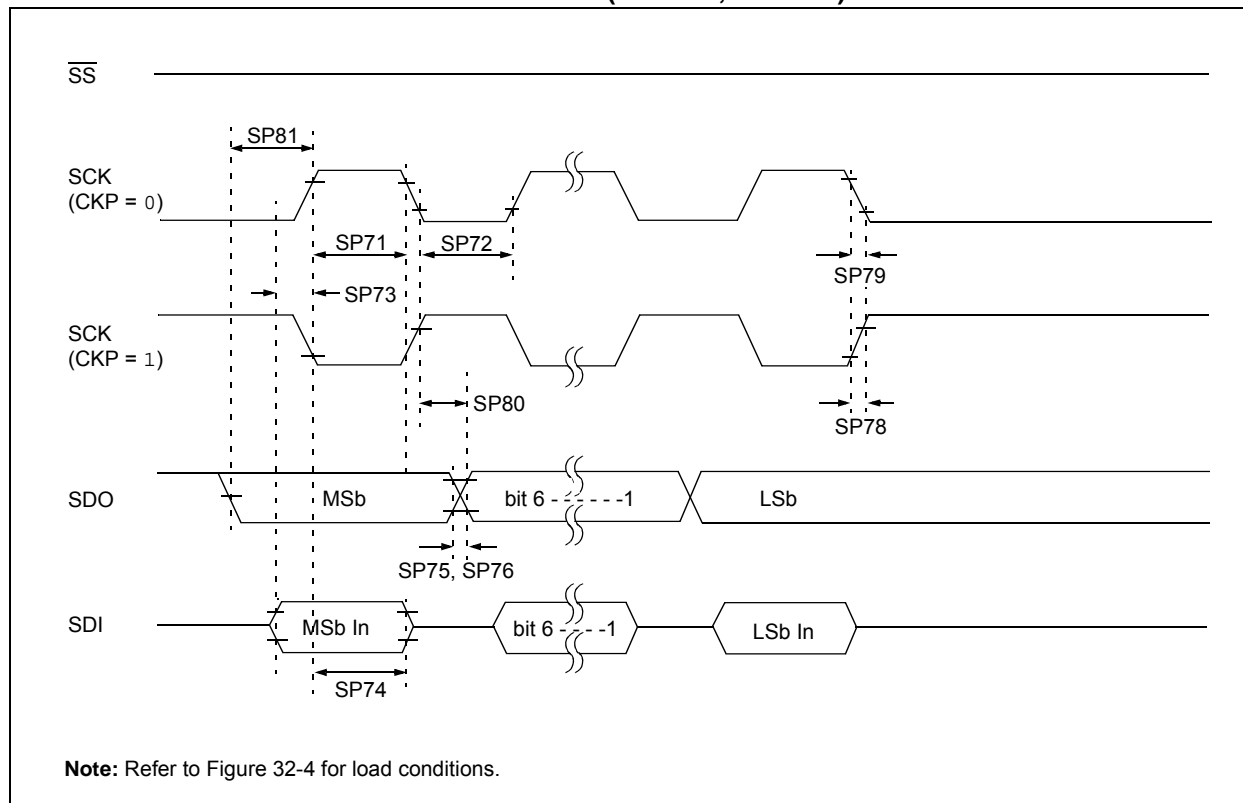
- Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
- 2:** Period of the slower clock.
- 3:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

# PIC16(L)F1704/8

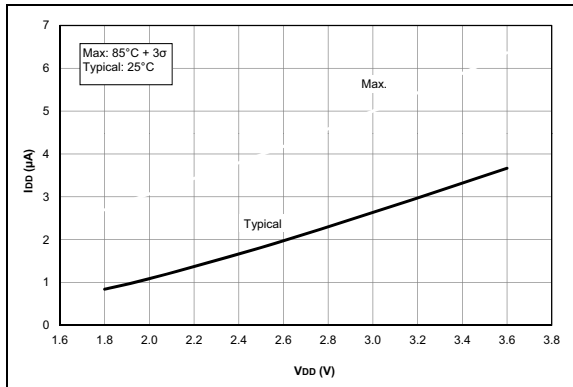
**FIGURE 32-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)**



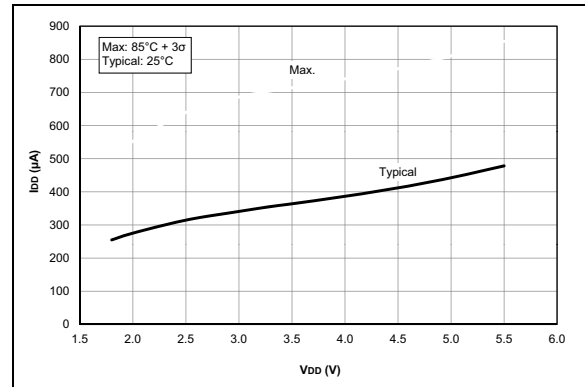
**FIGURE 32-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)**



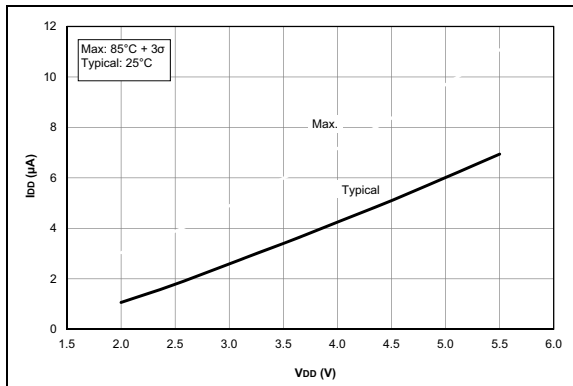
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 500\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu\text{F}$ ,  $T_A = 25^\circ\text{C}$ .



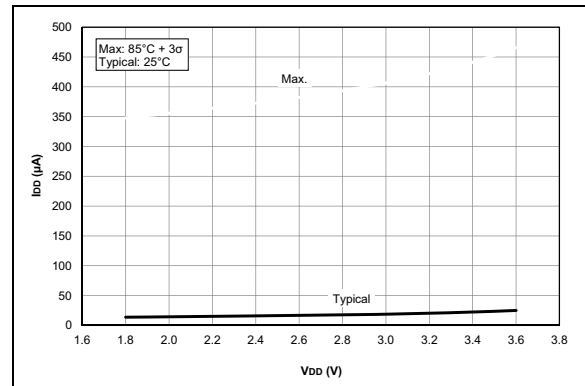
**FIGURE 33-43:**  $I_{PD}$ , Timer1 Oscillator,  $F_{OSC} = 32\text{ kHz}$ . PIC16LF1704/8 Only.



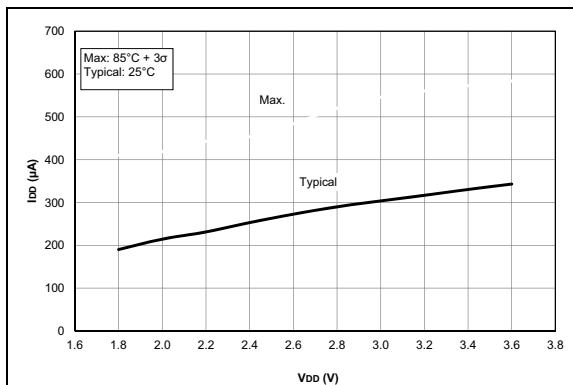
**FIGURE 33-46:**  $I_{PD}$ , Op Amp, High GBWP Mode ( $OPAxSP = 1$ ). PIC16F1704/8 Only.



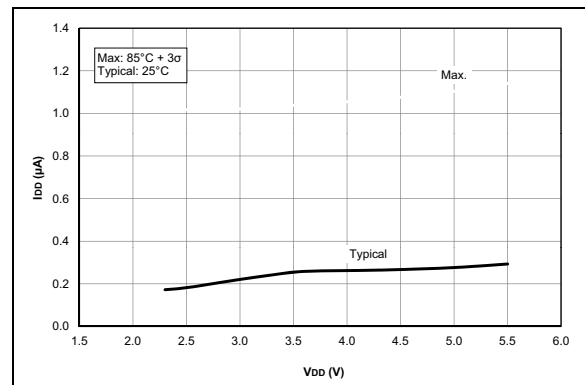
**FIGURE 33-44:**  $I_{PD}$ , Timer1 Oscillator,  $F_{OSC} = 32\text{ kHz}$ . PIC16F1704/8 Only.



**FIGURE 33-47:**  $I_{PD}$ , ADC Non-Converting. PIC16LF1704/8 Only.



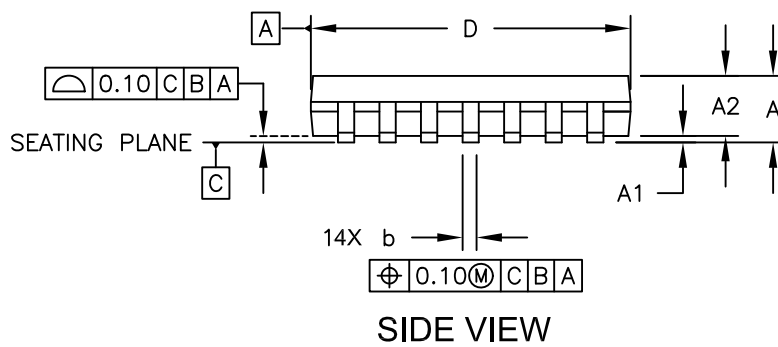
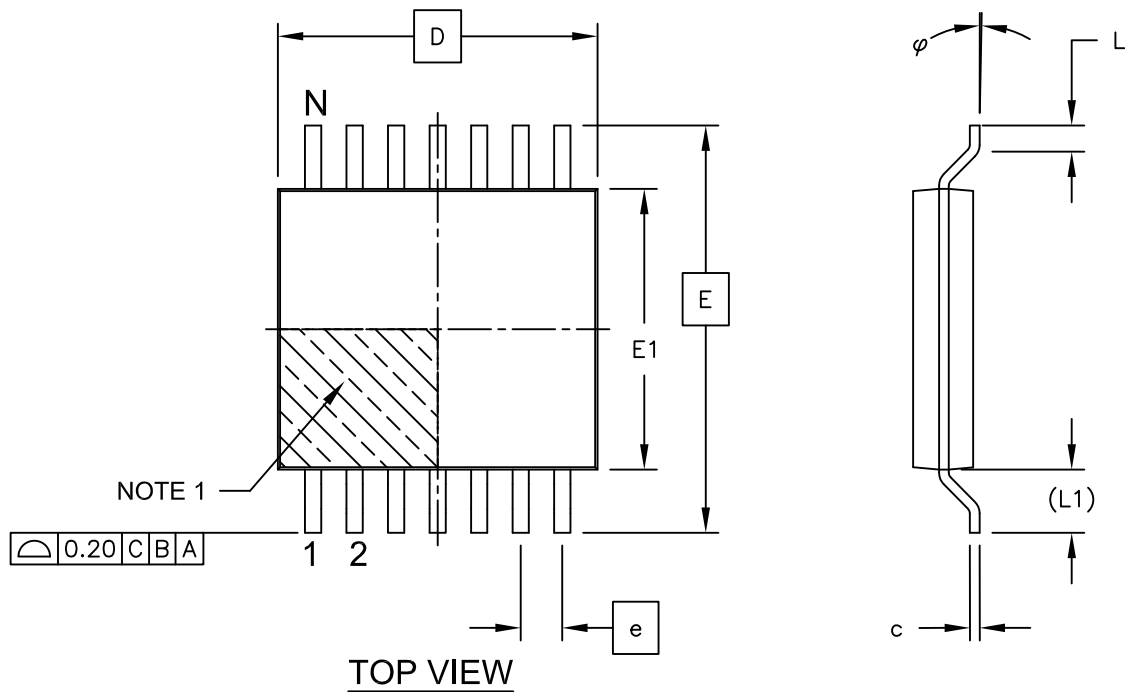
**FIGURE 33-45:**  $I_{PD}$ , Op Amp, High GBWP Mode ( $OPAxSP = 1$ ). PIC16LF1704/8 Only.



**FIGURE 33-48:**  $I_{PD}$ , ADC Non-Converting. PIC16F1704/8 Only.

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

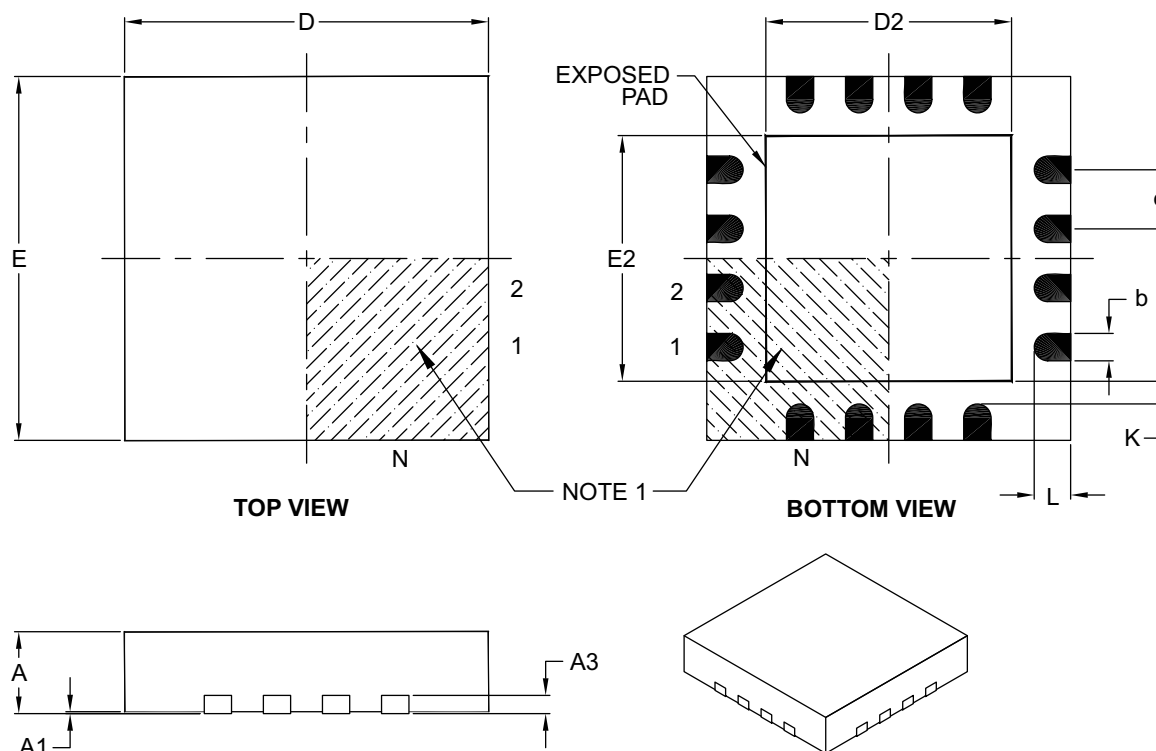
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



# PIC16(L)F1704/8

## 16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		16		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		4.00 BSC		
Exposed Pad Width	E2		2.50	2.65	2.80
Overall Length	D		4.00 BSC		
Exposed Pad Length	D2		2.50	2.65	2.80
Contact Width	b		0.25	0.30	0.35
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	–	–

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B