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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1704t-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1704t-i-ml</a>



# PIC16(L)F1704/8

**TABLE 1-2: PIC16(L)F1704 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RC1/AN5/C1IN1-/C2IN1-/OPA1IN-/SDI <sup>(1)</sup> /SDA <sup>(3)</sup> /CLCIN2 <sup>(1)</sup>	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	SDI	CMOS	—	SPI data input.
	SDA	I <sup>2</sup> C	—	I <sup>2</sup> C data input.
RC2/AN6/C1IN2-/C2IN2-/OPA1OUT	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RC3/AN7/C1IN3-/C2IN3-/OPA2OUT/CCP2 <sup>(1)</sup> /SS <sup>(1)</sup> /CLCIN0 <sup>(1)</sup>	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
	CCP2	TTL/ST	CMOS	Capture/Compare/PWM2.
	SS	TTL/ST	—	Slave Select input.
RC4/OPA2IN-/CK <sup>(1)</sup> /CLCIN1 <sup>(1)</sup>	CLCIN0	TTL/ST	—	Configurable Logic Cell source input.
	RC4	TTL/ST	CMOS	General purpose I/O.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CK	TTL/ST	CMOS	USART synchronous clock.
RC5/OPA2IN+/CCP1 <sup>(1)</sup> /RX <sup>(1)</sup>	CLCIN1	TTL/ST	—	Configurable Logic Cell source input.
	RC5	TTL/ST	CMOS	General purpose I/O.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP1	TTL/ST	CMOS	Capture/Compare/PWM1.
VDD	RX	TTL/ST	—	USART asynchronous input.
	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage    XTAL = Crystal levels

- Note** 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.  
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.  
3: These I<sup>2</sup>C functions are bidirectional. The output pin selections must be the same as the input pin selections.



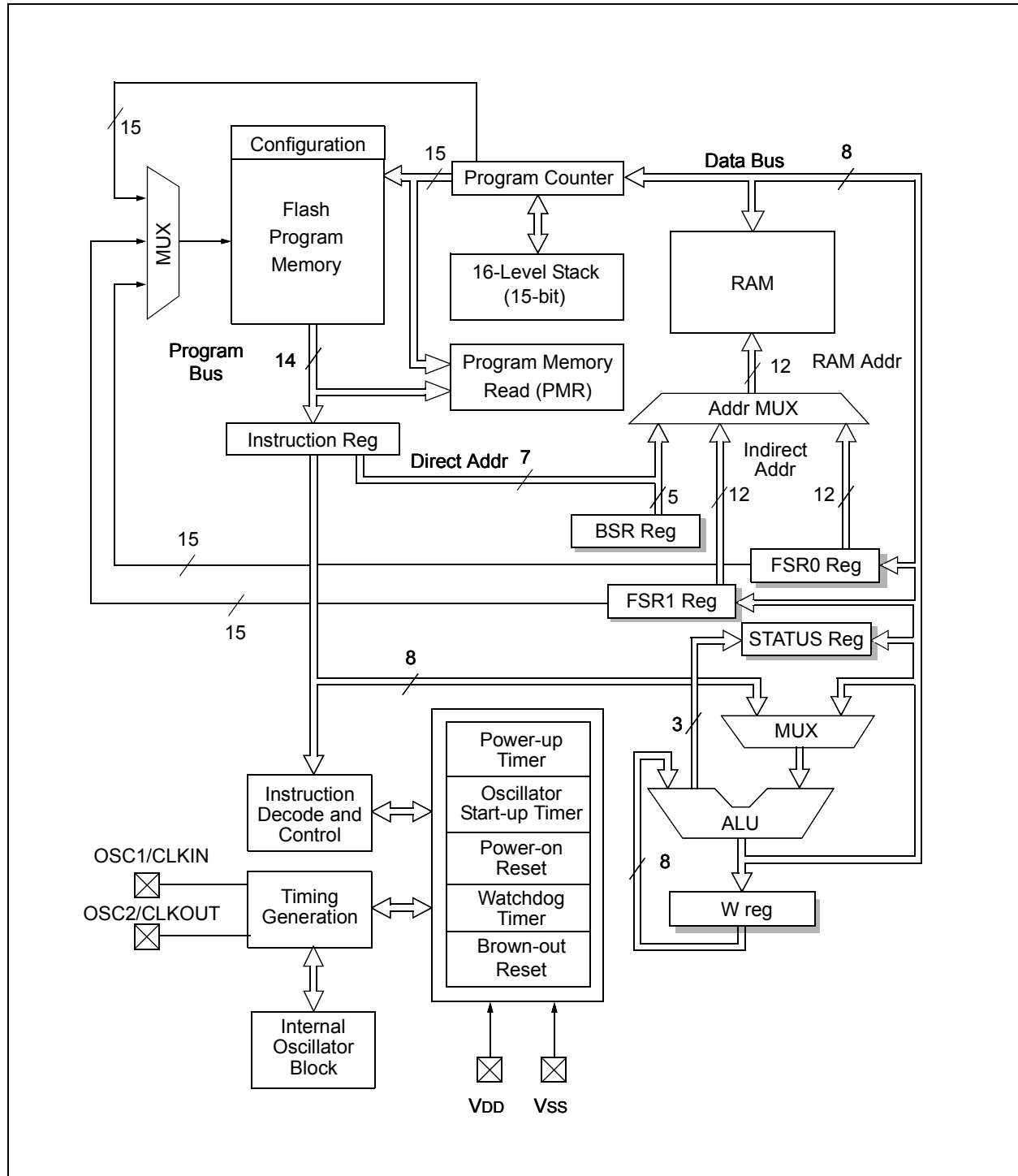
## 2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and

Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

**FIGURE 2-1: CORE BLOCK DIAGRAM**





# PIC16(L)F1704/8

**TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 4											
20Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111
20Dh	WPUB <sup>(3)</sup>	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	1111 ----	1111 ----
20Eh	WPUC	WPUC7 <sup>(3)</sup>	WPUC6 <sup>(3)</sup>	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	1111 1111	1111 1111
20Fh	—	Unimplemented								—	—
210h	—	Unimplemented								—	—
211h	SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
212h	SSP1ADD	ADD<7:0>								0000 0000	0000 0000
213h	SSP1MSK	MSK<7:0>								1111 1111	1111 1111
214h	SSP1STAT	SMP	CKE	D/ $\overline{A}$	P	S	$\overline{R/\overline{W}}$	UA	BF	0000 0000	0000 0000
215h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				0000 0000	0000 0000
216h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
217h	SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	0000 0000
218h — 21Fh	—	Unimplemented								—	—
Bank 5											
28Ch	ODCONA	—	—	ODA5	ODA4	—	ODA2	ODA1	ODA0	--00 -000	--00 -000
28Dh	ODCONB <sup>(3)</sup>	ODB7	ODB6	ODB5	ODB4	—	—	—	—	0000 ----	0000 ----
28Eh	ODCONC	ODC7 <sup>(3)</sup>	ODC6 <sup>(3)</sup>	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	0000 0000	0000 0000
28Fh	—	Unimplemented								—	—
290h	—	Unimplemented								—	—
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
293h	CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>			--00 0000	--00 0000	
294h — 297h	—	Unimplemented								—	—
298h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
299h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
29Ah	CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>			--00 0000	--00 0000	
29Bh — 29Dh	—	Unimplemented								—	—
29Eh	CCPTMRS	P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		0000 0000	0000 0000
29Fh	—	Unimplemented								—	—
Bank 6											
30Ch	SLRCONA	—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0	--00 -000	--00 -000
30Dh	SLRCONB <sup>(3)</sup>	SLRB7	SLRB6	SLRB5	SLRB4	—	—	—	—	0000 ----	0000 ----
30Eh	SLRCONC	SLRC7 <sup>(3)</sup>	SLRC6 <sup>(3)</sup>	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	0000 0000	0000 0000
30Fh — 31Fh	—	Unimplemented								—	—

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
Shaded locations are unimplemented, read as '0'.

- Note**
- 1: Unimplemented, read as '1'.
  - 2: PIC16(L)F1704 only.
  - 3: PIC16(L)F1708 only.
  - 4: Unimplemented on PIC16LF1704/8.



# PIC16(L)F1704/8

## REGISTER 10-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

U-1	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q <sup>(2)</sup>	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
— <sup>(1)</sup>	CFGFS	LWLO <sup>(3)</sup>	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7	<b>Unimplemented:</b> Read as '1'
bit 6	<b>CFGFS:</b> Configuration Select bit 1 = Access Configuration, User ID and Device ID Registers 0 = Access Flash program memory
bit 5	<b>LWLO:</b> Load Write Latches Only bit <sup>(3)</sup> 1 = Only the addressed program memory write latch is loaded/updated on the next WR command 0 = The addressed program memory write latch is loaded/updated and a write of all program memory write latches will be initiated on the next WR command
bit 4	<b>FREE:</b> Program Flash Erase Enable bit 1 = Performs an erase operation on the next WR command (hardware cleared upon completion) 0 = Performs a write operation on the next WR command
bit 3	<b>WRERR:</b> Program/Erase Error Flag bit 1 = Condition indicates an improper program or erase sequence attempt or termination (bit is set automatically on any set attempt (write '1') of the WR bit). 0 = The program or erase operation completed normally
bit 2	<b>WREN:</b> Program/Erase Enable bit 1 = Allows program/erase cycles 0 = Inhibits programming/erasing of program Flash
bit 1	<b>WR:</b> Write Control bit 1 = Initiates a program Flash program/erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete. The WR bit can only be set (not cleared) in software. 0 = Program/erase operation to the Flash is complete and inactive
bit 0	<b>RD:</b> Read Control bit 1 = Initiates a program Flash read. Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. 0 = Does not initiate a program Flash read

- Note** 1: Unimplemented bit, read as '1'.  
2: The WRERR bit is automatically set by hardware when a program memory write or erase operation is started (WR = 1).  
3: The LWLO bit is ignored during a program memory erase operation (FREE = 1).



## 11.1 PORTA Registers

### 11.1.1 DATA REGISTER

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 11-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input-only and its TRIS bit will always read as '1'. Example 11-1 shows how to initialize PORTA.

Reading the PORTA register (Register 11-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

### 11.1.2 DIRECTION CONTROL

The TRISA register (Register 11-2) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

### 11.1.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 11-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

### 11.1.4 SLEW RATE CONTROL

The SLRCONA register (Register 11-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

### 11.1.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 11-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 32-4: I/O Ports for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

### 11.1.6 ANALOG CONTROL

The ANSELA register (Register 11-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

**Note:** The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

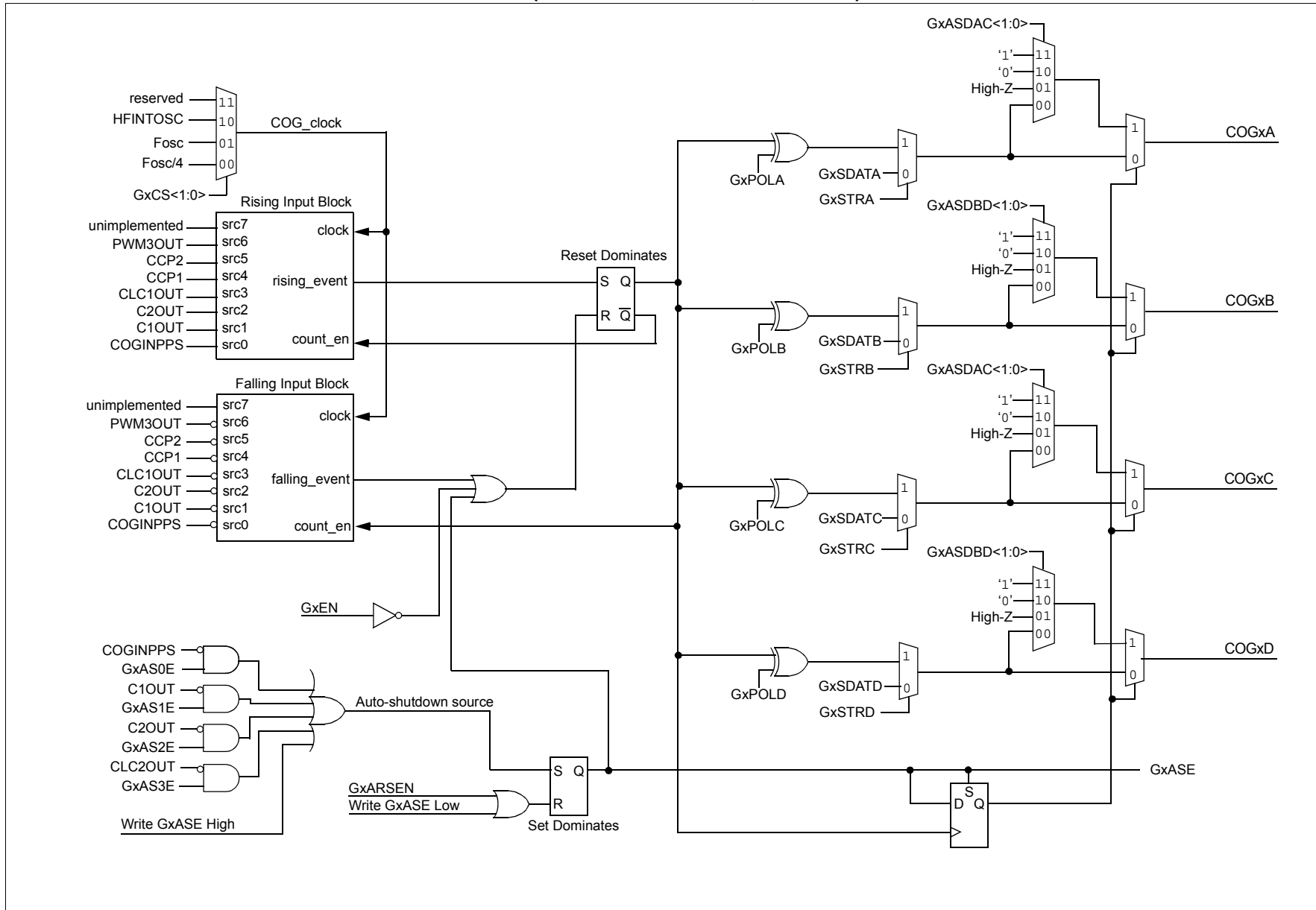
#### EXAMPLE 11-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL PORTA      ;
CLRF PORTA          ;Init PORTA
BANKSEL LATA        ;Data Latch
CLRF LATA           ;
BANKSEL ANSELA      ;
CLRF ANSELA         ;digital I/O
BANKSEL TRISA       ;
MOVLW B'00111000'  ;Set RA<5:3> as inputs
MOVWF TRISA         ;and set RA<2:0> as
                   ;outputs
```



**FIGURE 18-2: SIMPLIFIED COG BLOCK DIAGRAM (STEERED PWM MODE, GXMD = 0)**





# PIC16(L)F1704/8

REGISTER 19-6: CLCxSEL3: GENERIC CLCx DATA 4 SELECT REGISTER

U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	LCxD4S<4:0>				
bit 7							
							bit 0

**Legend:**  
R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                      '0' = Bit is cleared

bit 7-5

**Unimplemented:** Read as '0'

bit 4-0

**LCxD4S<4:0>:** CLCx Data 4 Input Selection bits  
See Table 19-1.



# PIC16(L)F1704/8

**TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx**

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
ANSELB <sup>(1)</sup>	—	—	ANSB5	ANSB4	—	—	—	—	128
ANSELC	ANSC7 <sup>(1)</sup>	ANSC6 <sup>(1)</sup>	ANSC5 <sup>(2)</sup>	ANSC4 <sup>(2)</sup>	ANSC3	ANSC2	ANSC1	ANSC0	133
CLC1CON	LC1EN	—	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			207
CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	LC2MODE<2:0>			207
CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			207
CLCDATA	—	—	—	—	—	MLC3OUT	MLC2OUT	MLC1OUT	215
CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	211
CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	212
CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	213
CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	214
CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	208
CLC1SEL0	—	—	—	LC1D1S<4:0>					209
CLC1SEL1	—	—	—	LC1D2S<4:0>					209
CLC1SEL2	—	—	—	LC1D3S<4:0>					209
CLC1SEL3	—	—	—	LC1D4S<4:0>					210
CLC2GLS0	LC2G1D4T	LC2G1D4N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	211
CLC2GLS1	LC2G2D4T	LC2G2D4N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	212
CLC2GLS2	LC2G3D4T	LC2G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	213
CLC2GLS3	LC2G4D4T	LC2G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	214
CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	208
CLC2SEL0	—	—	—	LC2D1S<4:0>					209
CLC2SEL1	—	—	—	LC2D2S<4:0>					209
CLC2SEL2	—	—	—	LC2D3S<4:0>					209
CLC2SEL3	—	—	—	LC2D4S<4:0>					210
CLC3GLS0	LC3G1D4T	LC3G1D4N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	211
CLC3GLS1	LC3G2D4T	LC3G2D4N	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	212
CLC3GLS2	LC3G3D4T	LC3G3D4N	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	213
CLC3GLS3	LC3G4D4T	LC3G4D4N	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	214
CLC3POL	LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	208
CLC3SEL0	—	—	—	LC3D1S<4:0>					209
CLC3SEL1	—	—	—	LC3D2S<4:0>					209
CLC3SEL2	—	—	—	LC3D3S<4:0>					209
CLC3SEL3	—	—	—	LC3D4S<4:0>					210
CLCxPPS	—	—	—	CLCxPPS<4:0>					138, 139
INTCON	GIE	PEIE	TMR0IE	INTE	IOCF	TMR0IF	INTF	IOCF	85
PIE3	—	—	COGIE	ZCDIE	—	CLC3IE	CLC2IE	CLC1IE	88
PIR3	—	—	COGIF	ZCDIF	—	CLC3IF	CLC2IF	CLC1IF	91
RxyPPS	—	—	—	RxyPPS<4:0>					140
TRISA	—	—	TRISA5	TRISA4	— <sup>(3)</sup>	TRISA2	TRISA1	TRISA0	121
TRISB <sup>(4)</sup>	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	127
TRISC	TRISC7 <sup>(4)</sup>	TRISC6 <sup>(4)</sup>	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132

**Legend:** — = unimplemented read as '0'. Shaded cells are not used for CLC module.

- Note**
- 1: PIC16(L)F1708 only.
  - 2: PIC16(L)F1704 only.
  - 3: Unimplemented, read as '1'.



# PIC16(L)F1704/8

## REGISTER 20-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<9:2>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0      **ADRES<9:2>**: ADC Result Register bits  
Upper eight bits of 10-bit conversion result

## REGISTER 20-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<1:0>		—	—	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6      **ADRES<1:0>**: ADC Result Register bits  
Lower two bits of 10-bit conversion result

bit 5-0      **Reserved**: Do not use.



## 24.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION\_REG register.

**Note:** The Watchdog Timer (WDT) uses its own independent prescaler.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION\_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION\_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

## 24.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

**Note:** The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

## 24.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in Table 32-12: Timer0 and Timer1 External Clock Requirements.

## 24.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.



**TABLE 25-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				267
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				267
INTCON	GIE	PEIE	TMR0IE	INTE	IOCFE	TMR0IF	INTF	IOCF	85
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	86
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	89
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								245*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								245*
TRISA	—	—	TRISA5	TRISA4	— <sup>(1)</sup>	TRISA2	TRISA1	TRISA0	121
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR1ON	253
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS<1:0>		254

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

\* Page provides register information.

**Note 1:** Unimplemented, read as '1'.



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## 27.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

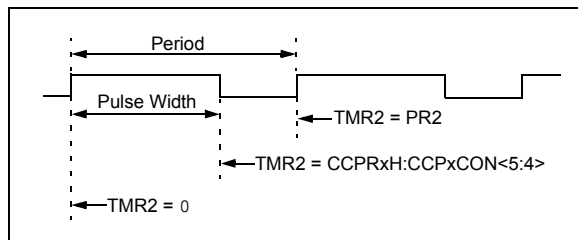
The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

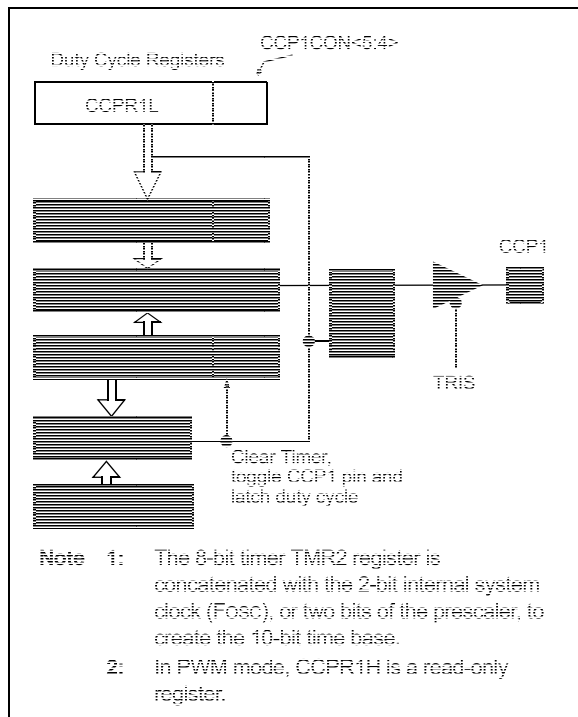
Figure 27-4 shows a simplified block diagram of PWM operation.

**Note:** The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

**FIGURE 27-3: CCP PWM OUTPUT SIGNAL**



**FIGURE 27-4: SIMPLIFIED PWM BLOCK DIAGRAM**



## 27.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Use the desired output pin RxyPPS control to select CCPx as the source and disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the PIRx register. See Note below.
  - Configure the T2CKPS bits of the T2CON register with the Timer prescale value.
  - Enable the Timer by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
  - Wait until the Timer overflows and the TMR2IF bit of the PIR1 register is set. See Note below.
  - Enable the CCPx pin output driver by clearing the associated TRIS bit.

**Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

## 27.3.3 TIMER2 TIMER RESOURCE

The PWM standard mode makes use of the 8-bit Timer2 timer resources to specify the PWM period.

## 27.3.4 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 27-1.

### EQUATION 27-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

**Note 1:**  $TOSC = 1/FOSC$



## 28.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I<sup>2</sup>C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ( $\overline{\text{ACK}}$ ) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an  $\overline{\text{ACK}}$  is placed in the ACKSTAT bit of the SSPCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the  $\overline{\text{ACK}}$  value sent back to the transmitter. The ACKDT bit of the SSPCON2 register is set/cleared to determine the response.

Slave hardware will generate an  $\overline{\text{ACK}}$  response if the AHEN and DHEN bits of the SSPCON3 register are clear.

There are certain conditions where an  $\overline{\text{ACK}}$  will not be sent by the slave. If the BF bit of the SSPSTAT register or the SSPOV bit of the SSPCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

## 28.5 I<sup>2</sup>C SLAVE MODE OPERATION

The MSSP Slave mode operates in one of four modes selected by the SSPM bits of SSPCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes with SSPIF additionally getting set upon detection of a Start, Restart, or Stop condition.

### 28.5.1 SLAVE MODE ADDRESSES

The SSPADD register (Register 28-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 28-5) affects the address matching process. See **Section 28.5.9 “SSP Mask Register”** for more information.

#### 28.5.1.1 I<sup>2</sup>C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

#### 28.5.1.2 I<sup>2</sup>C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of ‘1 1 1 0 A9 A8 0’. A9 and A8 are the two MSb’s of the 10-bit address and stored in bits 2 and 1 of the SSPADD register.

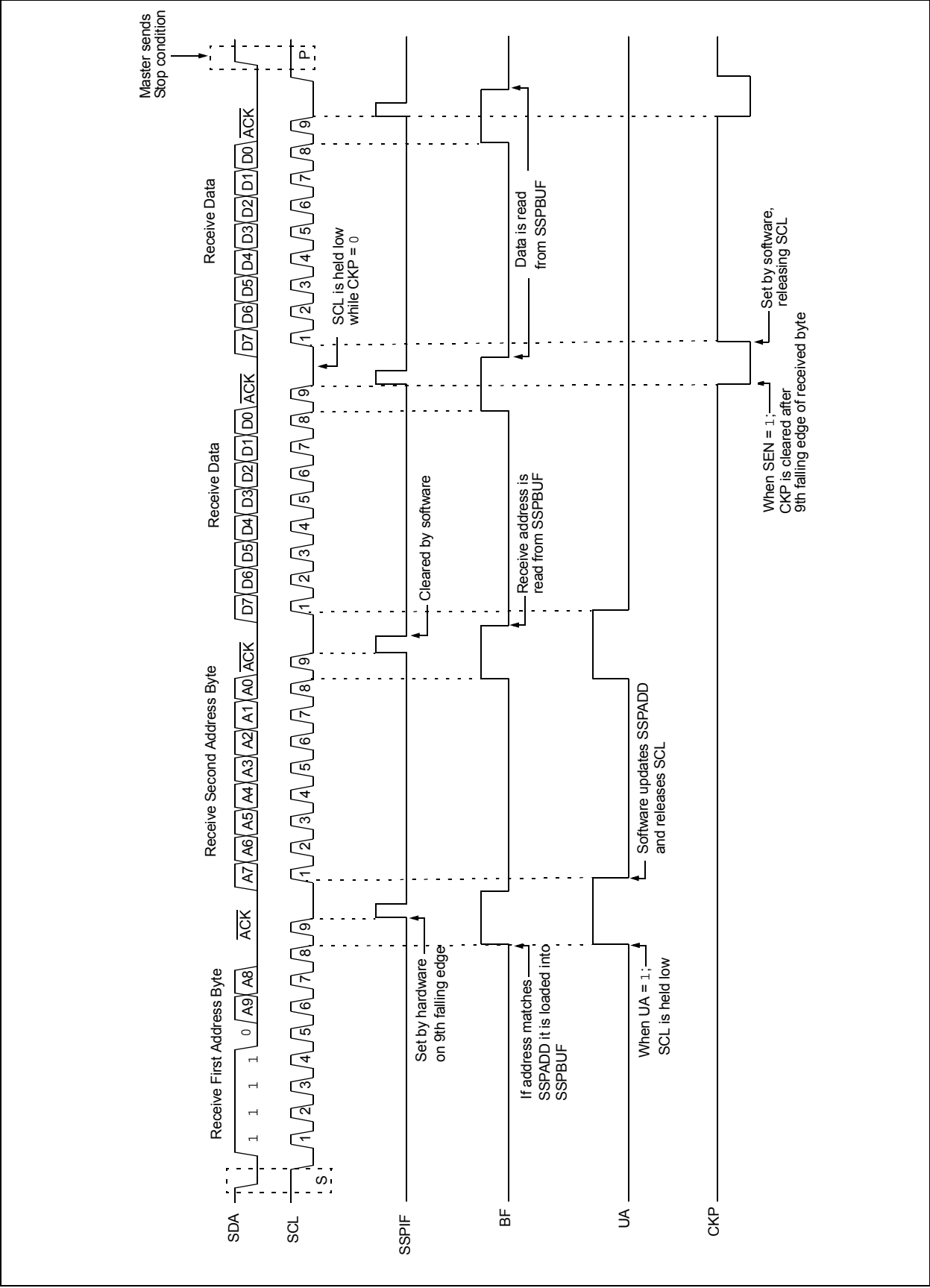
After the acknowledge of the high byte the UA bit is set and SCL is held low until the user updates SSPADD with the low address. The low address byte is clocked in and all eight bits are compared to the low address value in SSPADD. Even if there is not an address match; SSPIF and UA are set, and SCL is held low until SSPADD is updated to receive a high byte again. When SSPADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.



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FIGURE 28-20: I<sup>2</sup>C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)





**TABLE 28-3: SUMMARY OF REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
ANSELB <sup>(1)</sup>	—	—	ANSB5	ANSB4	—	—	—	—	128
ANSELC	ANSC7 <sup>(1)</sup>	ANSC6 <sup>(1)</sup>	ANSC5 <sup>(2)</sup>	ANSC4 <sup>(2)</sup>	ANSC3	ANSC2	ANSC1	ANSC0	133
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	85
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	86
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	TMR6IE	TMR4IE	CCP2IE	87
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	89
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	TMR6IF	TMR4IF	CCP2IF	90
RxyPPS	—	—	—	RxyPPS<4:0>					140
SSPCLKPPS	—	—	—	SSPCLKPPS<4:0>					138, 139
SSPDATPPS	—	—	—	SSPDATPPS<4:0>					138, 139
SSPSSPPS	—	—	—	SSPSSPPS<4:0>					138, 139
SSP1ADD	ADD<7:0>								323
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								272*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				319
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	321
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	322
SSP1MSK	MSK<7:0>								323
SSP1STAT	SMP	CKE	D/ $\bar{A}$	P	S	R/ $\bar{W}$	UA	BF	317
TRISA	—	—	TRISA5	TRISA4	— <sup>(3)</sup>	TRISA2	TRISA1	TRISA0	121
TRISB <sup>(1)</sup>	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	127
TRISC	TRISC7 <sup>(1)</sup>	TRISC6 <sup>(1)</sup>	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISA0	132

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I<sup>2</sup>C mode.

\* Page provides register information.

- Note** 1: PIC16(L)F1708 only.  
2: PIC16(L)F1704 only.  
3: Unimplemented, read as '1'.



## 30.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- VSS

In Program/Verify mode the program memory, user IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the “PIC16(L)F170X Memory Programming Specification” (DS41683).

### 30.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VIH.

### 30.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to ‘1’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

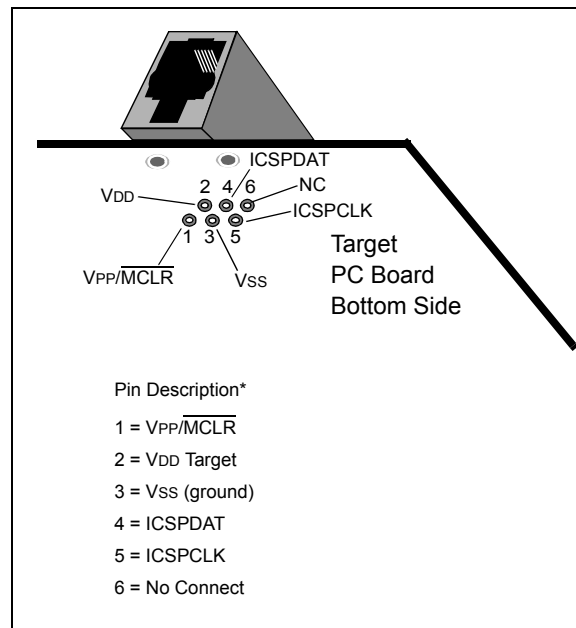
If low-voltage programming is enabled (LVP = 1), the MCLR Reset function is automatically enabled and cannot be disabled. See **Section 5.5 “MCLR”** for more information.

The LVP bit can only be reprogrammed to ‘0’ by using the High-Voltage Programming mode.

## 30.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 30-1.

**FIGURE 30-1: ICD RJ-11 STYLE CONNECTOR INTERFACE**



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 30-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 30-3 for more information.



## RRF Rotate Right f through Carry

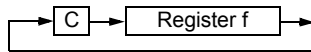
**Syntax:** [ *label* ] RRF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:** See description below

**Status Affected:** C

**Description:** The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



## SUBLW Subtract W from literal

**Syntax:** [ *label* ] SUBLW k

**Operands:**  $0 \leq k \leq 255$

**Operation:**  $k - (W) \rightarrow (W)$

**Status Affected:** C, DC, Z

**Description:** The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

## SLEEP Enter Sleep mode

**Syntax:** [ *label* ] SLEEP

**Operands:** None

**Operation:** 00h  $\rightarrow$  WDT,  
 $0 \rightarrow$  WDT prescaler,  
 $1 \rightarrow \overline{TO}$ ,  
 $0 \rightarrow \overline{PD}$

**Status Affected:**  $\overline{TO}$ ,  $\overline{PD}$

**Description:** The power-down Status bit,  $\overline{PD}$  is cleared. Time-out Status bit,  $\overline{TO}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

## SUBWF Subtract W from f

**Syntax:** [ *label* ] SUBWF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) - (W) \rightarrow (\text{destination})$

**Status Affected:** C, DC, Z

**Description:** Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	$W > f$
C = 1	$W \leq f$
DC = 0	$W<3:0> > f<3:0>$
DC = 1	$W<3:0> \leq f<3:0>$

## SUBWFB Subtract W from f with Borrow

**Syntax:** SUBWFB f {,d}

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) - (W) - (\overline{B}) \rightarrow \text{dest}$

**Status Affected:** C, DC, Z

**Description:** Subtract W and the BORROW flag (CARRY) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.



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**TABLE 32-23: SPI MODE REQUIREMENTS**

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic	Min.	Typ.†	Max.	Units	Conditions
SP70*	TssL2sch, TssL2scl	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	2.25 Tcy	—	—	ns	
SP71*	Tsch	SCK input high time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	Tscl	SCK input low time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdIV2sch, TdIV2scl	Setup time of SDI data input to SCK edge	100	—	—	ns	
SP74*	Tsch2diL, Tscl2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
SP75*	TdoR	SDO data output rise time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO data output fall time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output high-impedance	10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK output fall time (Master mode)	—	10	25	ns	
SP80*	Tsch2doV, Tscl2doV	SDO data output valid after SCK edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2sch, TdoV2scl	SDO data output setup to SCK edge	Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	—	—	50	ns	
SP83*	Tsch2ssH, Tscl2ssH	$\overline{SS}\uparrow$ after SCK edge	1.5 Tcy + 40	—	—	ns	

\* These parameters are characterized but not tested.

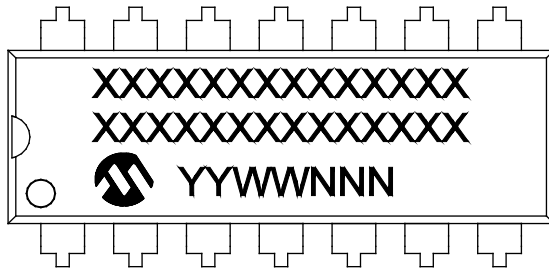
† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



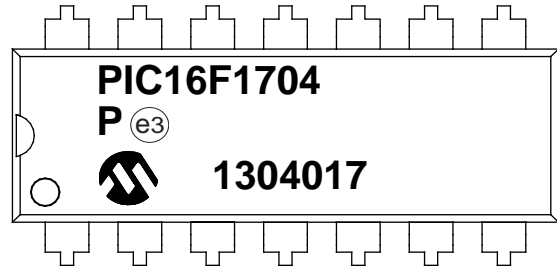
## 35.0 PACKAGING INFORMATION

### 35.1 Package Marking Information

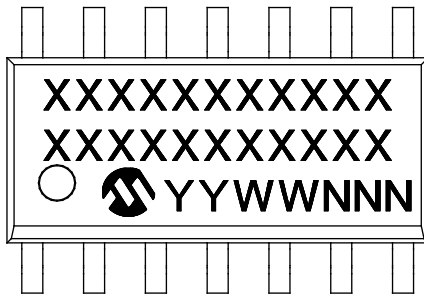
14-Lead PDIP (300 mil)



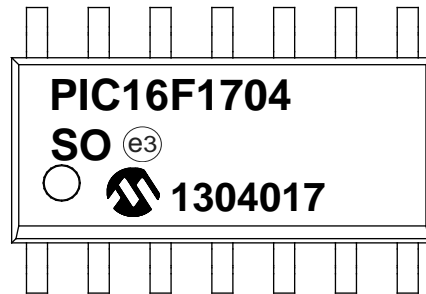
Example



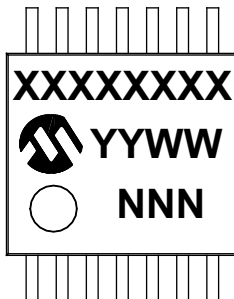
14-Lead SOIC (3.90 mm)



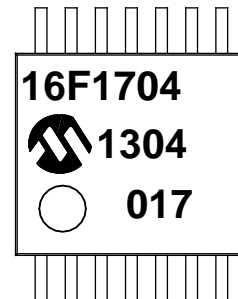
Example



14-Lead TSSOP (4.4 mm)



Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC® designator (e3) can be found on the outer packaging for this package.

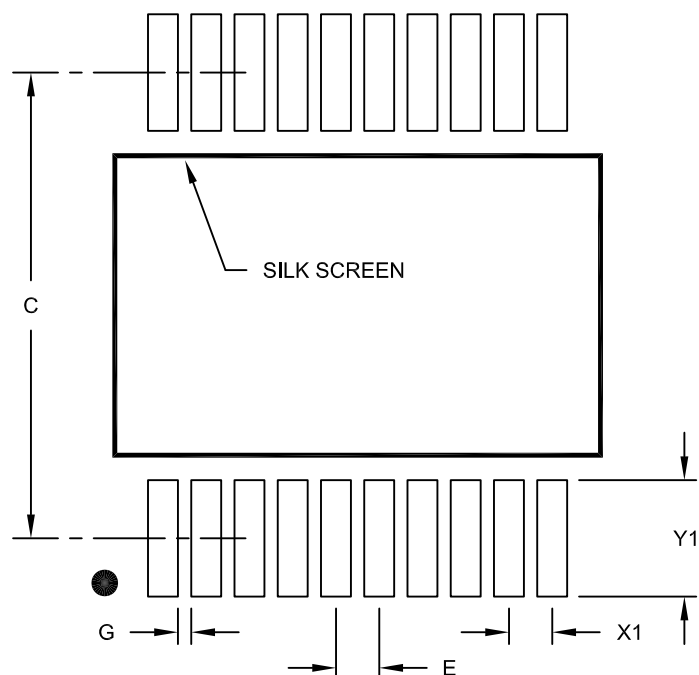
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



# PIC16(L)F1704/8

## 20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A