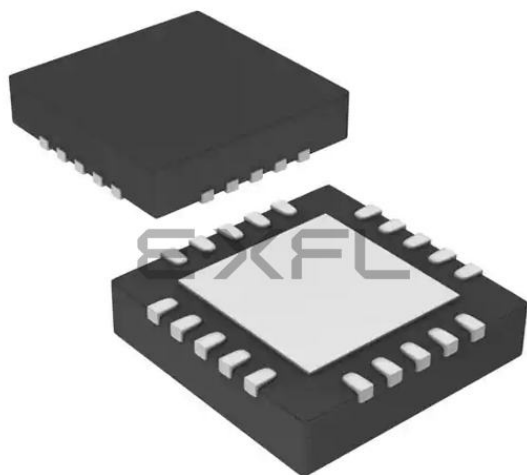




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1708-e-ml

TABLE 1-2: PIC16(L)F1704 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT ⁽²⁾	C1OUT	—	CMOS	Comparator output.
	C2OUT	—	CMOS	Comparator output.
	CCP1	—	CMOS	Capture/Compare/PWM1 output.
	CCP2	—	CMOS	Capture/Compare/PWM2 output.
	PWM3OUT	—	CMOS	PWM3 output.
	PWM4OUT	—	CMOS	PWM4 output.
	COGA	—	CMOS	Complementary Output Generator Output A.
	COGB	—	CMOS	Complementary Output Generator Output B.
	COGC	—	CMOS	Complementary Output Generator Output C.
	COGD	—	CMOS	Complementary Output Generator Output D.
	SDA ⁽³⁾	—	OD	I ² C data input/output.
	SDO	—	CMOS	SPI data output.
	SCK	—	CMOS	SPI clock output.
	SCL ⁽³⁾	—	OD	I ² C clock output.
	TX/CK	—	CMOS	USART asynchronous TX data/synchronous clock output.
	DT	—	CMOS	USART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note** 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.
3: These I²C functions are bidirectional. The output pin selections must be the same as the input pin selections.

4.2 Register Definitions: Configuration Words

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>	—	
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP ⁽¹⁾	MCLRE	PWRT	WDTE<1:0>	FOSC<2:0>			
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'
 '0' = Bit is cleared '1' = Bit is set -n = Value when blank or after Bulk Erase

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor and internal/external switchover are both enabled.
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
If FOSC configuration bits are set to LP, XT, HS modes:
 This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
All other FOSC modes:
 1 = CLKOUT function is disabled. I/O function on the CLKOUT pin.
 0 = CLKOUT function is enabled on the CLKOUT pin
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the BORCON register
 00 = BOR disabled
- bit 8 **Unimplemented:** Read as '1'
- bit 7 **CP:** Code Protection bit⁽¹⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
If LVP bit = 1:
 This bit is ignored.
If LVP bit = 0:
 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUE3 bit.
- bit 5 **PWRT:** Power-up Timer Enable bit
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep
 01 = WDT controlled by the SWDTEN bit in the WDTCON register
 00 = WDT disabled

PIC16(L)F1704/8

7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

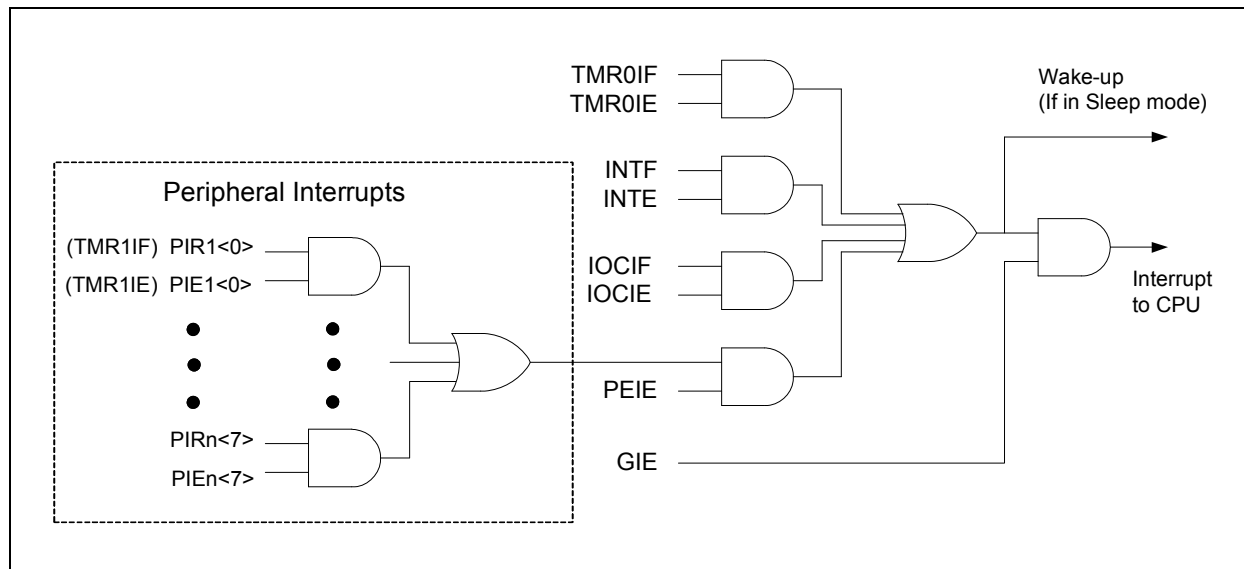
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: INTERRUPT LOGIC



REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

U-0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	COGIF	ZCDIF	—	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6	Unimplemented: Read as '0'
bit 5	COGIF: COG Auto-Shutdown Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 4	ZCDIF: Zero-Cross Detection Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 3	Unimplemented: Read as '0'
bit 2	CLC3IF: CLC3 Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 1	CLC2IF: CLC2 Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 0	CLC1IF: CLC1 Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

13.6 Register Definitions: Interrupt-on-Change Control

REGISTER 13-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAP<5:0>:** Interrupt-on-Change PORTA Positive Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared HS - Bit is set in hardware

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin.

Set when IOCAPx = 1 and a rising edge was detected on RAX, or when IOCANx = 1 and a falling edge was detected on RAX.

0 = No change was detected, or the user cleared the detected change.

16.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and Fixed Voltage Reference

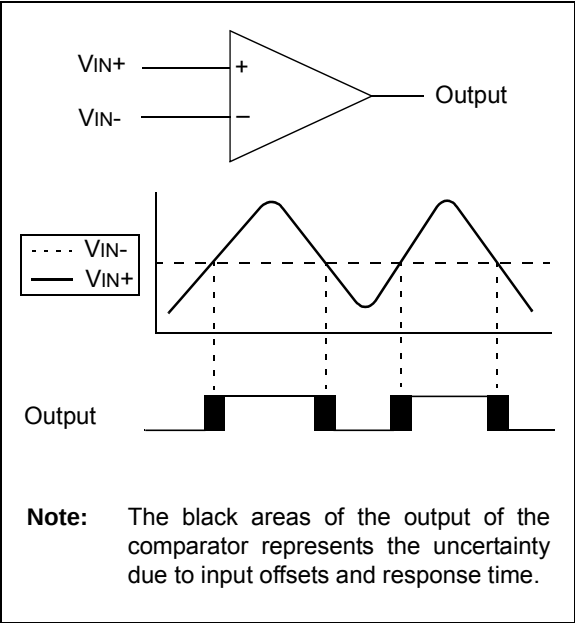
16.1 Comparator Overview

A single comparator is shown in Figure 16-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level. The comparators available for this device are located in Table 16-1.

TABLE 16-1: AVAILABLE COMPARATORS

Device	C1	C2
PIC16(L)F1704/8	•	•

FIGURE 16-1: SINGLE COMPARATOR



PIC16(L)F1704/8

19.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

19.1.1 DATA SELECTION

There are 32 signals available as inputs to the configurable logic. Four 32-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 19-2. Data inputs in the figure are identified by a generic numbered input name.

Table 19-1 correlates the generic input name to the actual signal for each CLC module. The column labeled *lcxdy* indicates the MUX selection code for the selected data input. *DxS* is an abbreviation for the MUX select input codes: LCxD1S<4:0> through LCxD4S<4:0>.

Data inputs are selected with CLCxSEL0 through CLCxSEL3 registers (Register 19-3 through Register 19-6).

Note: Data selections are undefined at power-up.

TABLE 19-1: CLCx DATA INPUT SELECTION

Data Input	lcxdy DxS	CLCx
LCx_in[31]	11111	Fosc
LCx_in[30]	11110	HFINTOSC
LCx_in[29]	11101	LFINTOSC
LCx_in[28]	11100	ADC FRC
LCx_in[27]	11011	IOCIF set signal (bit?)
LCx_in[26]	11010	T2_match
LCx_in[25]	11001	T1_overflow
LCx_in[24]	11000	T0_overflow
LCx_in[23]	10111	T6_match
LCx_in[22]	10110	T4_match
LCx_in[21]	10101	DT from EUSART
LCx_in[20]	10100	TX/CK from EUSART
LCx_in[19]	10011	ZCDx_out from Zero-Cross Detect
LCx_in[18]	10010	SDO from MSSP
LCx_in[17]	10001	Reserved
LCx_in[16]	10000	SCK from MSSP
LCx_in[15]	01111	PWM4_out
LCx_in[14]	01110	PWM3_out
LCx_in[13]	01101	CCP2 output
LCx_in[12]	01100	CCP1 output
LCx_in[11]	01011	COG1B
LCx_in[10]	01010	COG1A
LCx_in[9]	01001	C2OUT
LCx_in[8]	01000	C1OUT
LCx_in[7]	00111	Reserved
LCx_in[6]	00110	LC3_out from the CLC3
LCx_in[5]	00101	LC2_out from the CLC2
LCx_in[4]	00100	LC1_out from the CLC1
LCx_in[3]	00011	CLCIN3 pin input selected in CLCIN3PPS register
LCx_in[2]	00010	CLCIN2 pin input selected in CLCIN2PPS register
LCx_in[1]	00001	CLCIN1 pin input selected in CLCIN1PPS register
LCx_in[0]	00000	CLCIN0 pin input selected in CLCIN0PPS register

REGISTER 19-3: CLCxSEL0: GENERIC CLCx DATA 1 SELECT REGISTER

U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	LCxD1S<4:0>				
bit 7							
							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **LCxD1S<4:0>**: CLCx Data1 Input Selection bits
See Table 19-1.

REGISTER 19-4: CLCxSEL1: GENERIC CLCx DATA 2 SELECT REGISTER

U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	LCxD2S<4:0>				
bit 7							
							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **LCxD2S<4:0>**: CLCx Data 2 Input Selection bits
See Table 19-1.

REGISTER 19-5: CLCxSEL2: GENERIC CLCx DATA 3 SELECT REGISTER

U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	LCxD3S<4:0>				
bit 7							
							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **LCxD3S<4:0>**: CLCx Data 3 Input Selection bits
See Table 19-1.

FIGURE 22-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

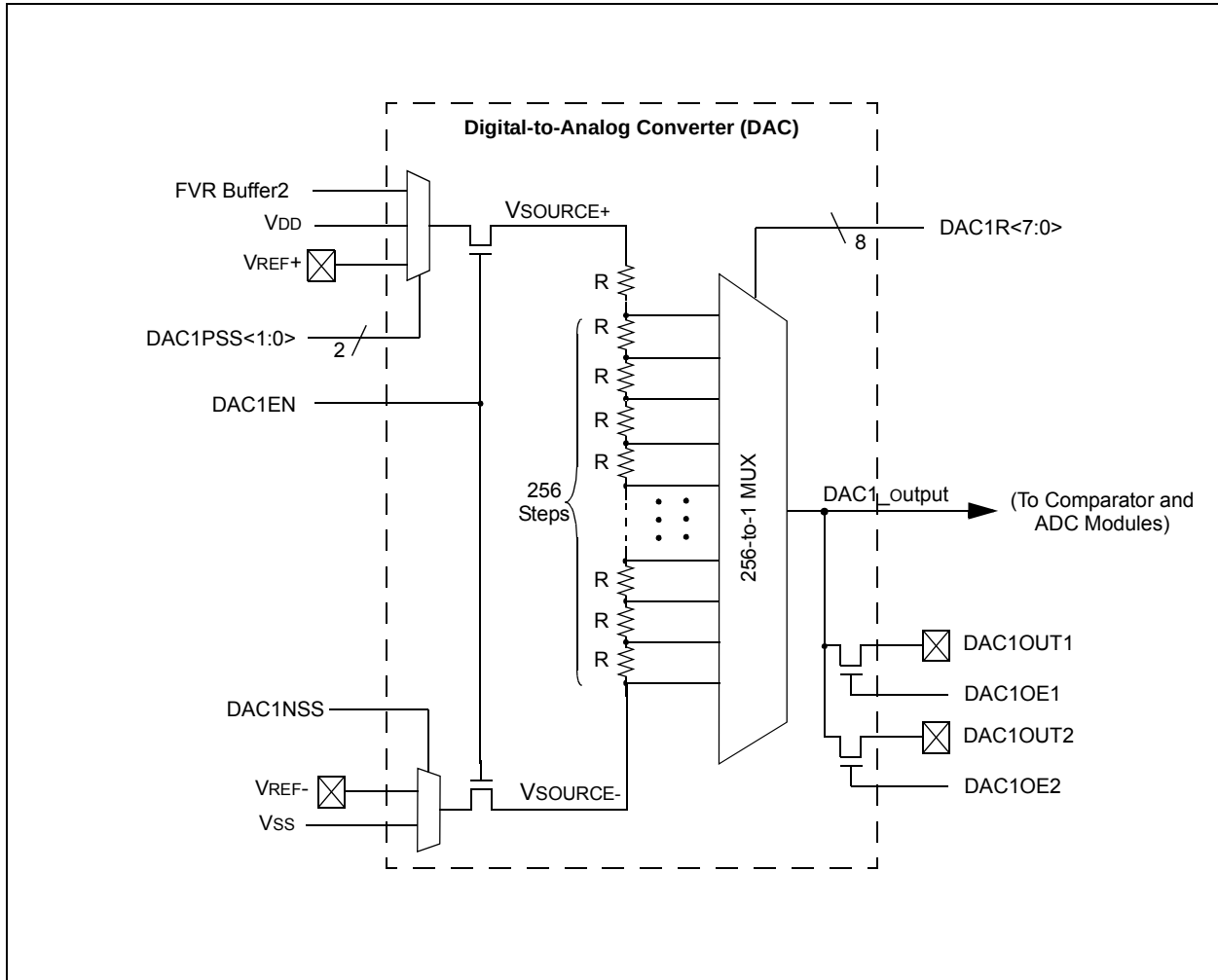
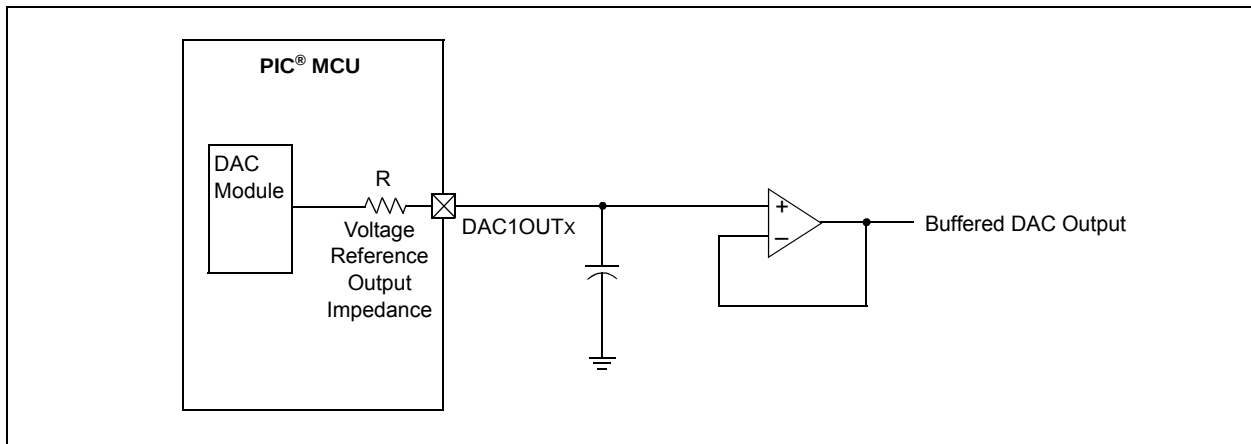


FIGURE 22-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



PIC16(L)F1704/8

26.5 Register Definitions: Timer2 Control

REGISTER 26-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **T2OUTPS<3:0>:** Timer2 Output Postscaler Select bits

1111 = 1:16 Postscaler

1110 = 1:15 Postscaler

1101 = 1:14 Postscaler

1100 = 1:13 Postscaler

1011 = 1:12 Postscaler

1010 = 1:11 Postscaler

1001 = 1:10 Postscaler

1000 = 1:9 Postscaler

0111 = 1:8 Postscaler

0110 = 1:7 Postscaler

0101 = 1:6 Postscaler

0100 = 1:5 Postscaler

0011 = 1:4 Postscaler

0010 = 1:3 Postscaler

0001 = 1:2 Postscaler

0000 = 1:1 Postscaler

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

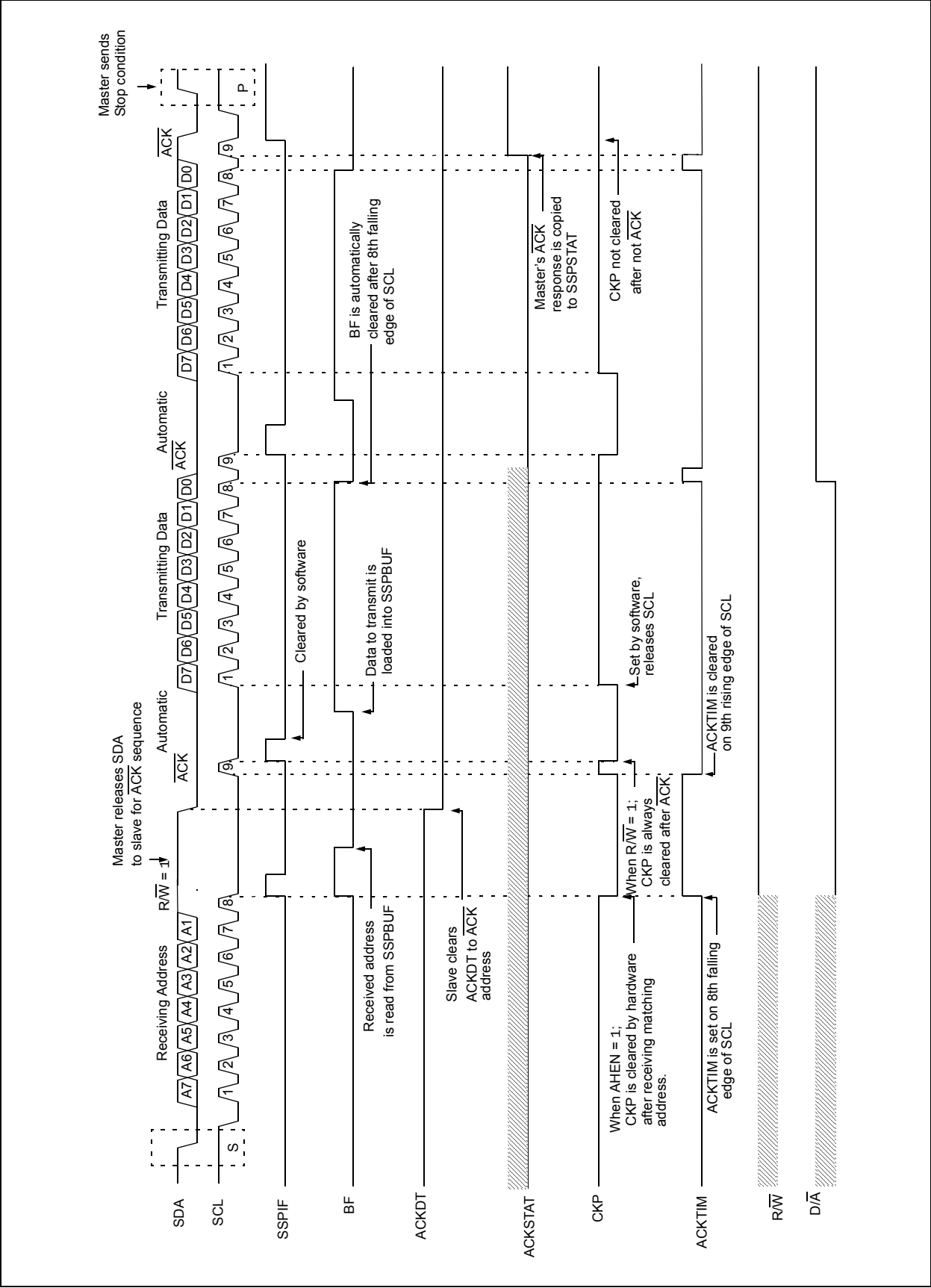
11 = Prescaler is 64

10 = Prescaler is 16

01 = Prescaler is 4

00 = Prescaler is 1

FIGURE 28-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)



29.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.
--

29.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

29.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

29.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

29.5 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

29.5.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

29.5.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

29.5.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock.

Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

29.5.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

29.5.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 29.4 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

LSLF Logical Left Shift

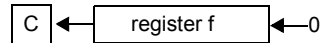
Syntax: `[label] LSLF f{,d}`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<7>) \rightarrow C$
 $(f<6:0>) \rightarrow \text{dest}<7:1>$
 $0 \rightarrow \text{dest}<0>$

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



LSRF Logical Right Shift

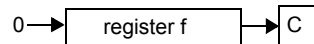
Syntax: `[label] LSRF f{,d}`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $0 \rightarrow \text{dest}<7>$
 $(f<7:1>) \rightarrow \text{dest}<6:0>$,
 $(f<0>) \rightarrow C$,

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



MOVF Move f

Syntax: `[label] MOVF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) \rightarrow (\text{dest})$

Status Affected: Z

Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: `MOVF FSR, 0`

After Instruction
 $W = \text{value in FSR register}$
 $Z = 1$

MOVWI Move W to INDFn

Syntax: [*label*] MOVWI ++FSRn
[*label*] MOVWI --FSRn
[*label*] MOVWI FSRn++
[*label*] MOVWI FSRn--
[*label*] MOVWI k[FSRn]

Operands: n ∈ [0,1]
mm ∈ [00,01, 10, 11]
-32 ≤ k ≤ 31

Operation: W → INDFn
Effective address is determined by

- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:

- FSR + 1 (all increments)
- FSR - 1 (all decrements)

Unchanged

Status Affected: None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

NOP No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example: NOP

OPTION Load OPTION_REG Register with W

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION_REG

Status Affected: None

Description: Move data from W register to OPTION_REG register.

Words: 1

Cycles: 1

Example: OPTION

Before Instruction
OPTION_REG = 0xFF
W = 0x4F

After Instruction
OPTION_REG = 0x4F
W = 0x4F

RESET Software Reset

Syntax: [*label*] RESET

Operands: None

Operation: Execute a device Reset. Resets the $\overline{RI}$ flag of the PCON register.

Status Affected: None

Description: This instruction provides a way to execute a hardware Reset by software.

FIGURE 32-11: CAPTURE/COMPARE/PWM TIMINGS (CCP)

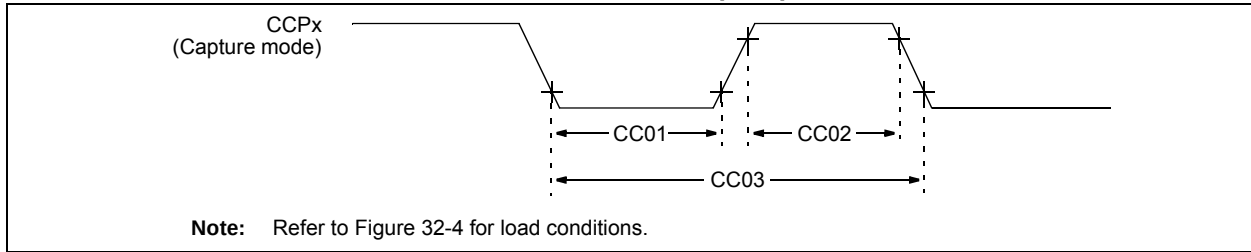


TABLE 32-13: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic		Min.	Typ.†	Max.	Units	Conditions
CC01*	TccL	CCPx Input Low Time	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCPx Input High Time	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCPx Input Period		$\frac{3 T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 500\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$.

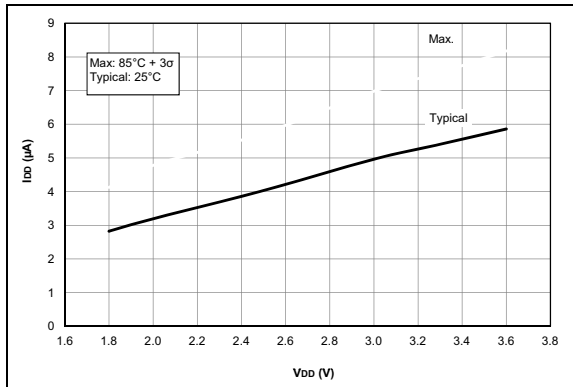


FIGURE 33-19: I_{DD} , LFINTOSC Mode, $F_{osc} = 31\text{ kHz}$. PIC16LF1704/8 Only.

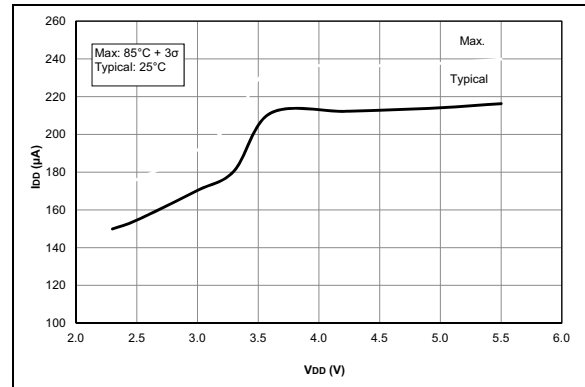


FIGURE 33-22: I_{DD} , MFINTOSC Mode, $F_{osc} = 500\text{ kHz}$. PIC16F1704/8 Only.

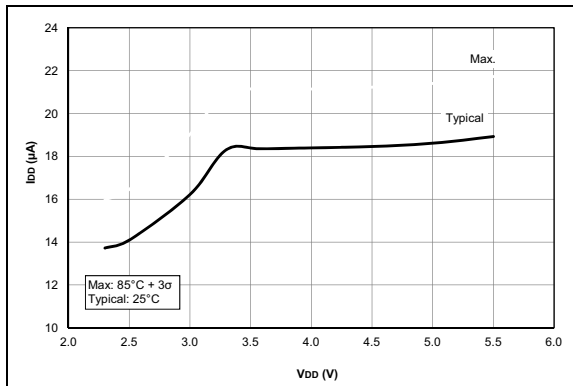


FIGURE 33-20: I_{DD} , LFINTOSC Mode, $F_{osc} = 31\text{ kHz}$. PIC16F1704/8 Only.

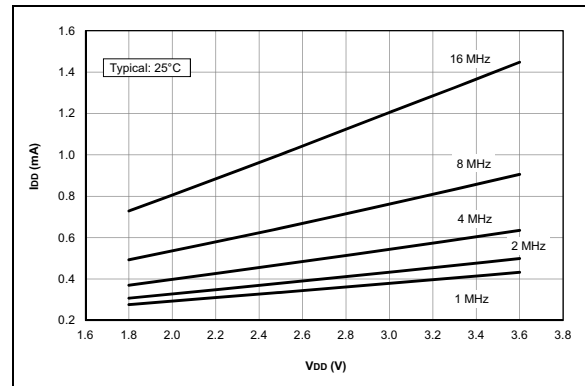


FIGURE 33-23: I_{DD} Typical, HFINTOSC Mode. PIC16LF1704/8 Only.

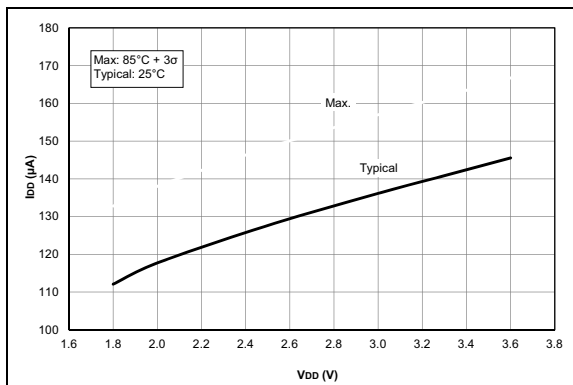


FIGURE 33-21: I_{DD} , MFINTOSC Mode, $F_{osc} = 500\text{ kHz}$. PIC16LF1704/8 Only.

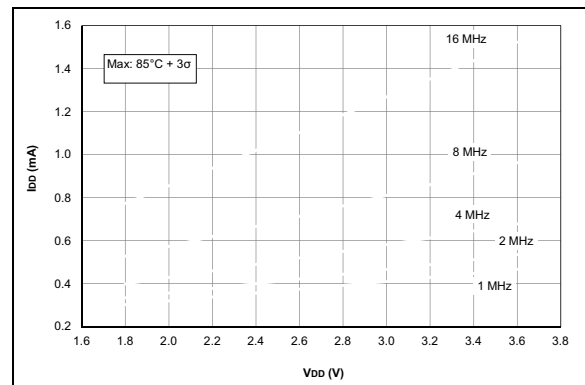
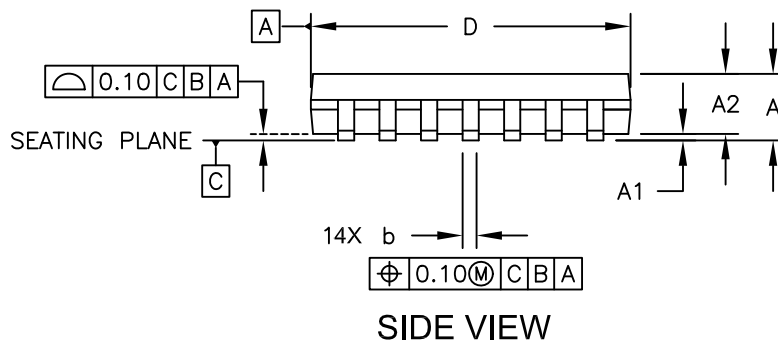
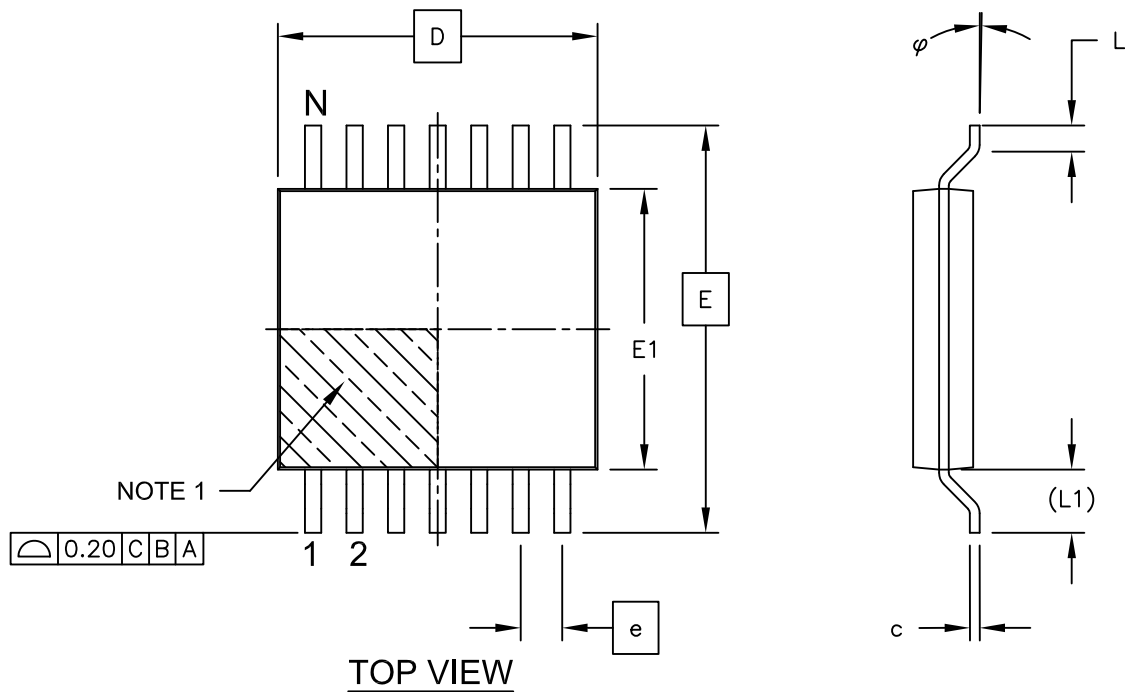


FIGURE 33-24: I_{DD} Maximum, HFINTOSC Mode. PIC16LF1704/8 Only.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

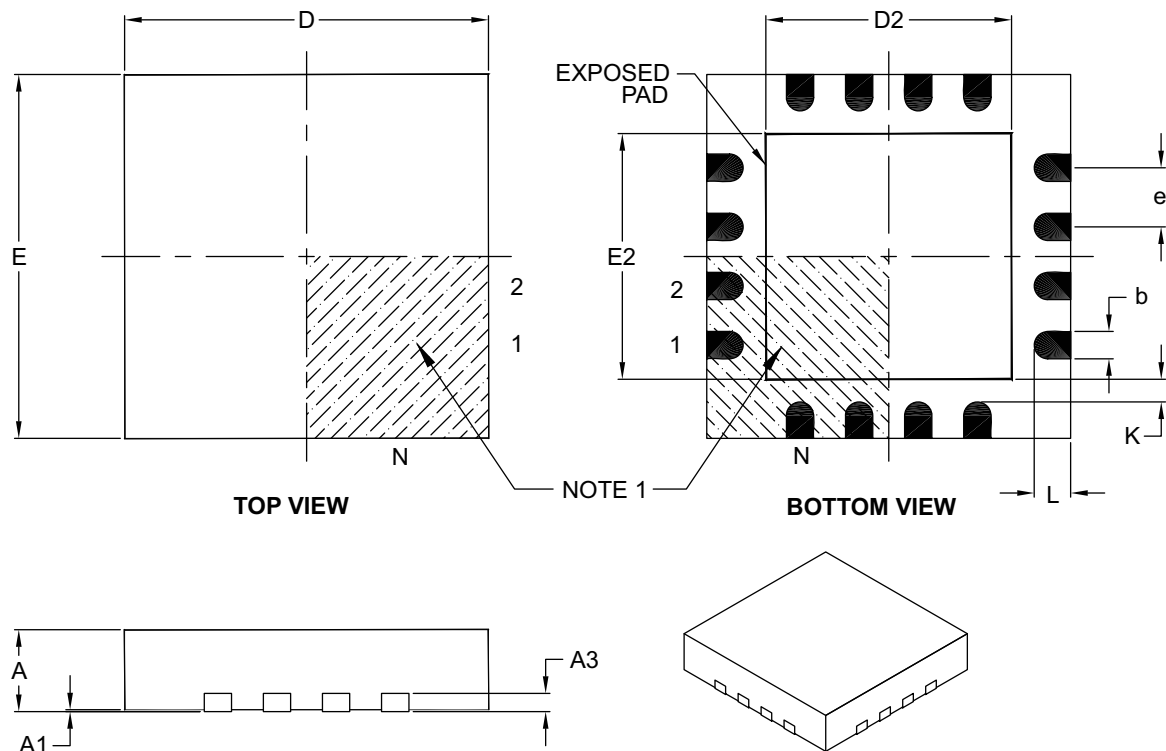
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		16		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		4.00 BSC		
Exposed Pad Width	E2		2.50	2.65	2.80
Overall Length	D		4.00 BSC		
Exposed Pad Length	D2		2.50	2.65	2.80
Contact Width	b		0.25	0.30	0.35
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

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