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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9af344nbpqc-g-jne2

HDMI-CEC/Remote Control Receiver (Up to 2 channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter

The Watch counter is used for wake up from sleep and timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (2channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC, Deep Standby Stop modes.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- Built-in high-speed CR Clock : 4 MHz
- Built-in low-speed CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Contents

1. Product Lineup

Memory size

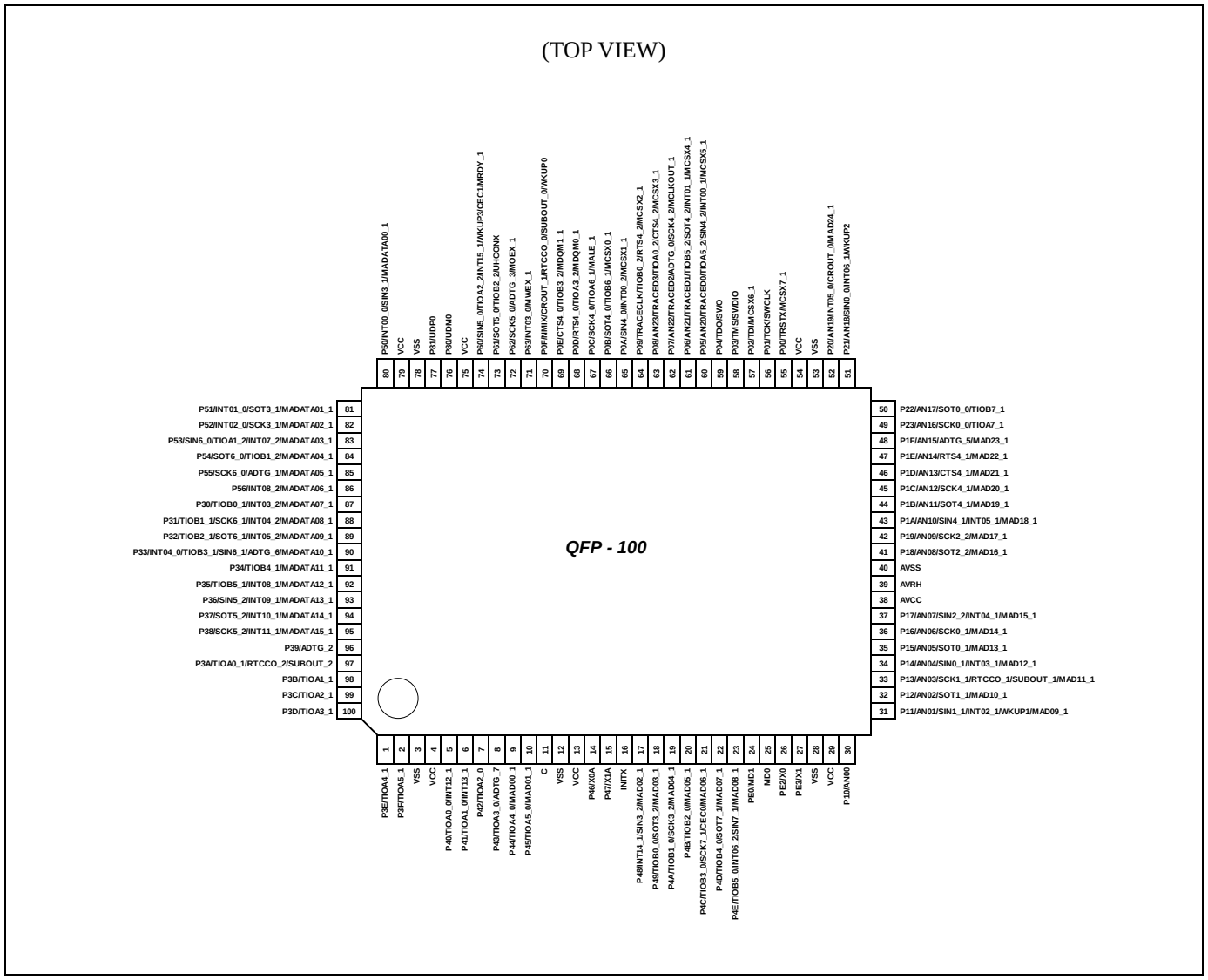
Product name		MB9AF341LB/MB/NB	MB9AF342LB/MB/NB	MB9AF344LB/MB/NB
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

Function

Product name		MB9AF341LB MB9AF342LB MB9AF344LB	MB9AF341MB MB9AF342MB MB9AF344MB	MB9AF341NB MB9AF342NB MB9AF344NB
Pin count		64	80/96	100/112
CPU		Cortex-M3		
	Freq.	40 MHz		
Power supply voltage range		1.65 V to 3.6 V		
USB2.0 (Function/Host)		1ch.		
DMAC		8ch.		
External Bus Interface		-	Addr: 21-bit (Max) R/W Data: 8-bit (Max) CS: 4 (Max) Support: SRAM, NOR Flash memory	Addr: 25-bit (Max) R/W Data: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash memory
Multi-function Serial Interface (UART/CSIO/I^{2}C)		8ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)		8ch. (Max)		
Dual Timer		1 unit		
HDMI-CEC/ Remote Control Receiver		2ch. (Max)		
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		8 pins (Max) + NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O ports		51 pins (Max)	66 pins (Max)	83 pins (Max)
12-bit A/D converter		12ch. (2 units)	17ch. (2 units)	24ch. (2 units)
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP		SWJ-DP/ETM
Unique ID		Yes		

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the I/O port according to your function use.
See Electrical Characteristics 12.4 AC Characteristics (12.4.3)Built-in CR Oscillation Characteristics for accuracy of built-in CR.

FPT-100P-M36



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
96	74	C4	76	C4	60	P60	I	T
						SIN5_0		
						TIOA2_2		
						INT15_1		
						WKUP3		
						CEC1		
					-	MRDY_1		
97	75	A4	77	A4	61	VCC	-	
98	76	A3	78	A3	62	P80	H	H
						UDM0		
99	77	A2	79	A2	63	P81	H	H
						UDP0		
100	78	A1	80	A1	64	VSS	-	

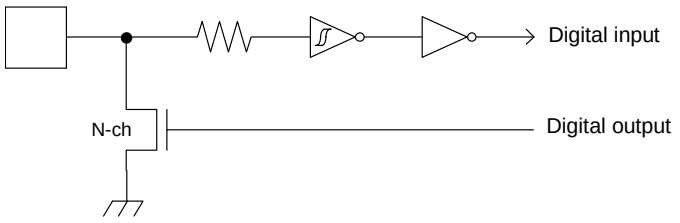
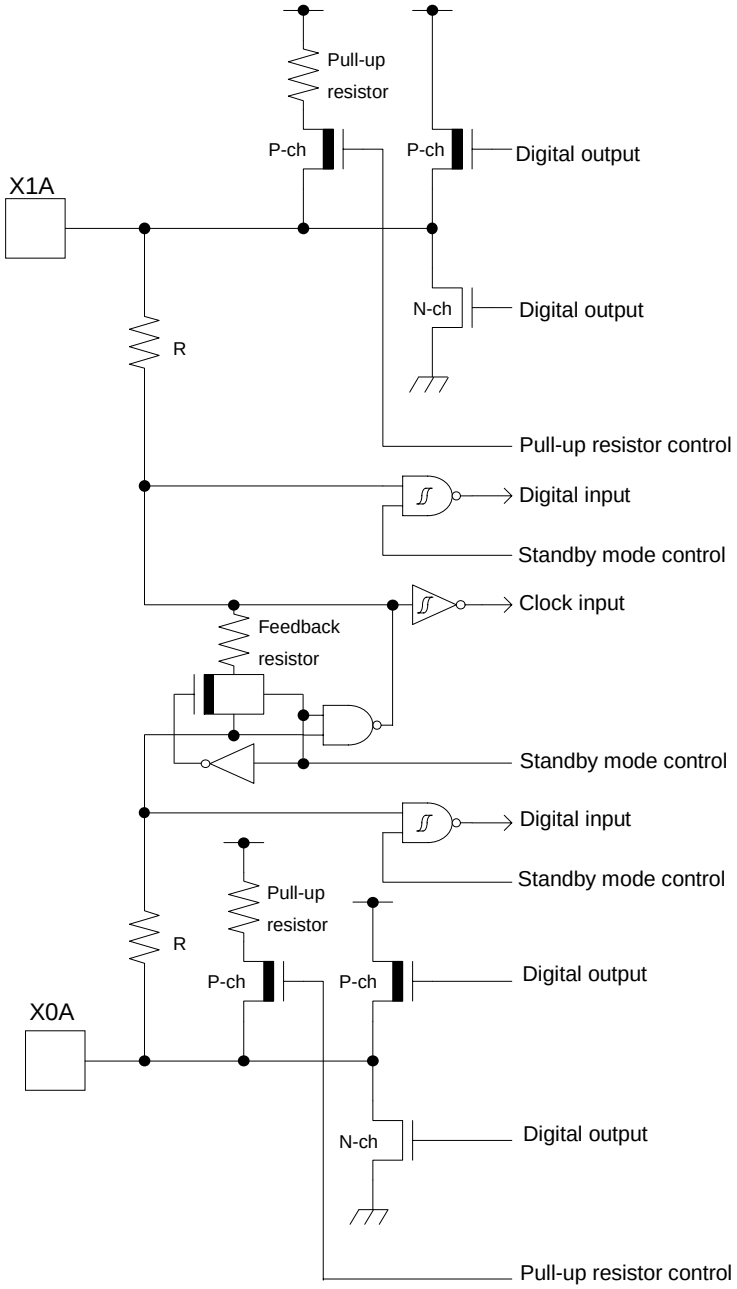
List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/ QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	A8	-
	ADTG_1		7	85	D3	7	D3	-
	ADTG_2		18	96	F4	13	G3	9
	ADTG_3		94	72	C5	74	C5	58
	ADTG_4		-	-	-	-	-	-
	ADTG_5		70	48	D11	-	-	-
	ADTG_6		12	90	E4	12	G2	8
	ADTG_7		30	8	J5	-	-	-
	ADTG_8		-	-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	30	J11	42	J11	34
	AN01		53	31	J10	43	J10	35
	AN02		54	32	J8	44	J8	36
	AN03		55	33	H10	45	H10	37
	AN04		56	34	H9	46	H9	38
	AN05		57	35	H7	47	G10	39
	AN06		58	36	G10	48	G9	-
	AN07		59	37	G9	49	F10	40
	AN08		63	41	G8	53	F9	44
	AN09		64	42	F10	54	E11	45
	AN10		65	43	F9	55	E10	-
	AN11		66	44	E11	56	E9	-
	AN12		67	45	E10	-	-	-
	AN13		68	46	F8	-	-	-
	AN14		69	47	E9	-	-	-
	AN15		70	48	D11	-	-	-
	AN16		71	49	D10	57	D10	46
	AN17		72	50	E8	58	D9	47
	AN18		73	51	C11	59	C11	48
	AN19		74	52	C10	60	C10	-
	AN20		82	60	C8	-	-	-
	AN21		83	61	D9	-	-	-
	AN22		84	62	A7	66	A8	-
	AN23		85	63	B7	-	-	-

Pin Function	Pin Name	Function Description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/ QFN-64
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-	-
	TIOA0_1		19	97	G3	14	H1	10
	TIOA0_2		85	63	B7	-	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	K6	22
	TIOB0_1		9	87	E1	9	E2	5
	TIOB0_2		86	64	C7	-	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-	-
	TIOA1_1		20	98	H1	15	H2	11
	TIOA1_2		5	83	D1	5	D1	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	J6	23
	TIOB1_1		10	88	E2	10	E3	6
	TIOB1_2		6	84	D2	6	D2	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	7	K5	-	-	-
	TIOA2_1		21	99	H2	16	H3	12
	TIOA2_2		96	74	C4	76	C4	60
	TIOB2_0	Base timer ch.2 TIOB pin	42	20	K7	32	L7	24
	TIOB2_1		11	89	E3	11	G1	7
	TIOB2_2		95	73	B4	75	B4	59
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	30	8	J5	-	-	-
	TIOA3_1		22	100	G4	17	J1	13
	TIOA3_2		90	68	C6	70	B6	-
	TIOB3_0	Base timer ch.3 TIOB pin	43	21	H6	33	K7	25
	TIOB3_1		12	90	E4	12	G2	8
	TIOB3_2		91	69	A5	71	C6	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	31	9	H5	21	L5	-
	TIOA4_1		23	1	H3	18	J2	14
	TIOA4_2		-	-	-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	44	22	J7	34	J7	26
	TIOB4_1		13	91	F1	-	-	-
	TIOB4_2		-	-	-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	32	10	L6	22	K5	-
	TIOA5_1		24	2	J2	19	J4	15
	TIOA5_2		82	60	C8	-	-	-
	TIOB5_0	Base timer ch.5 TIOB pin	45	23	K8	35	K8	27
	TIOB5_1		14	92	F2	-	-	-
	TIOB5_2		83	61	D9	-	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	89	67	B6	69	B7	56
	TIOB6_1	Base timer ch.6 TIOB pin	88	66	A6	68	C7	55
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-	-	-
	TIOA7_1		71	49	D10	57	D10	46
	TIOA7_2		-	-	-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-	-	-
	TIOB7_1		72	50	E8	58	D9	47
	TIOB7_2		-	-	-	-	-	-

Pin Function	Pin Name	Function Description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	83	D1	5	D1	-
	SIN6_1		12	90	E4	12	G2	8
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	6	84	D2	6	D2	-
	SOT6_1 (SDA6_1)		11	89	E3	11	G1	7
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	85	D3	7	D3	-
	SCK6_1 (SCL6_1)		10	88	E2	10	E3	6
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	45	23	K8	35	K8	27
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	44	22	J7	34	J7	26
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	43	21	H6	33	K7	25

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With Standby mode control • Pull-up resistor : Approximately 33 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby RTC mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
Q	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

12.4.4 Operating Conditions of Main and USB PLL (In the case of using main clock for input of PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	40	MHz	
USB clock frequency*3	$f_{CLKSPLL}$	-	-	48	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

*3: For more information about USB clock, see Chapter 2-2: USB Clock Generation in FM3 Family Peripheral Manual Communication Macro Part.

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for the input clock of the Main PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	40	MHz	

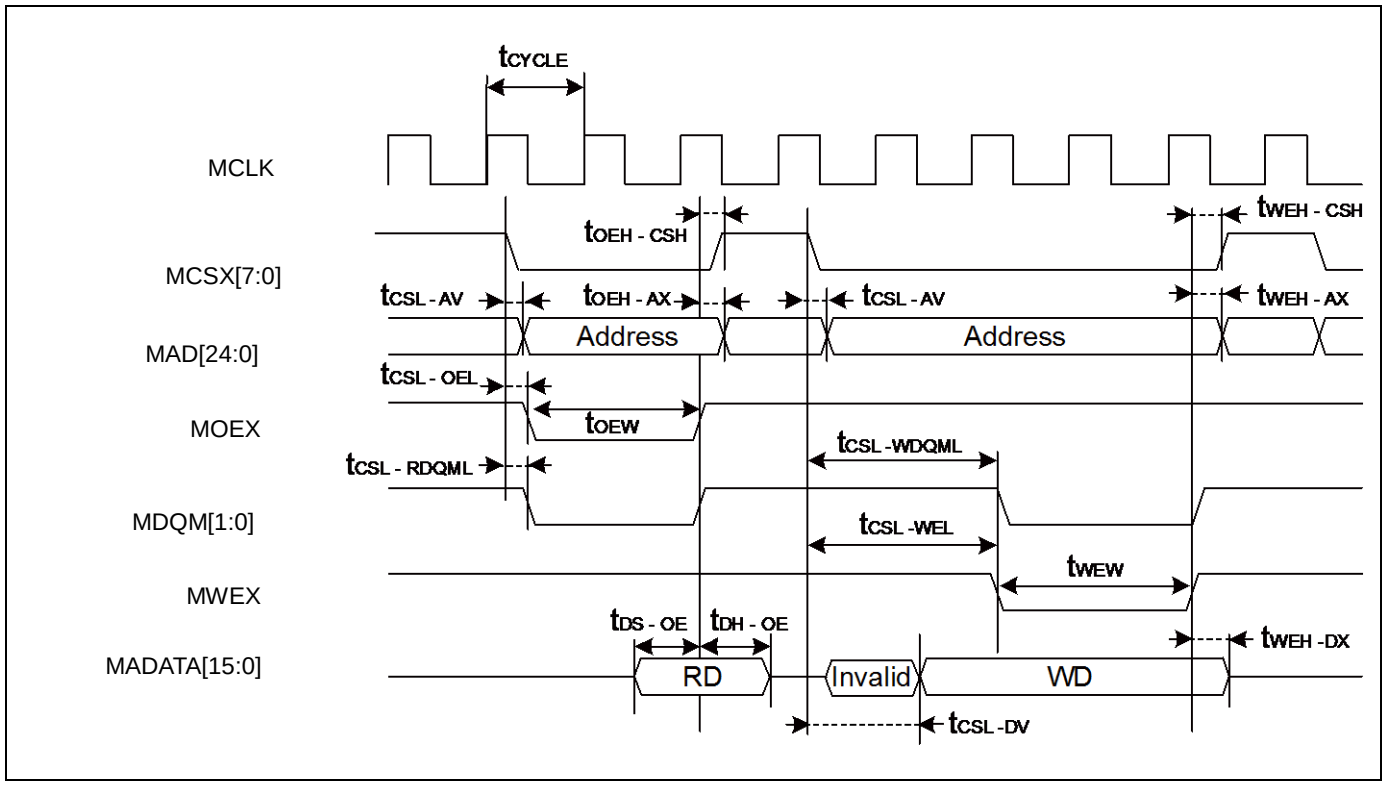
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

Note:

Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.

When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

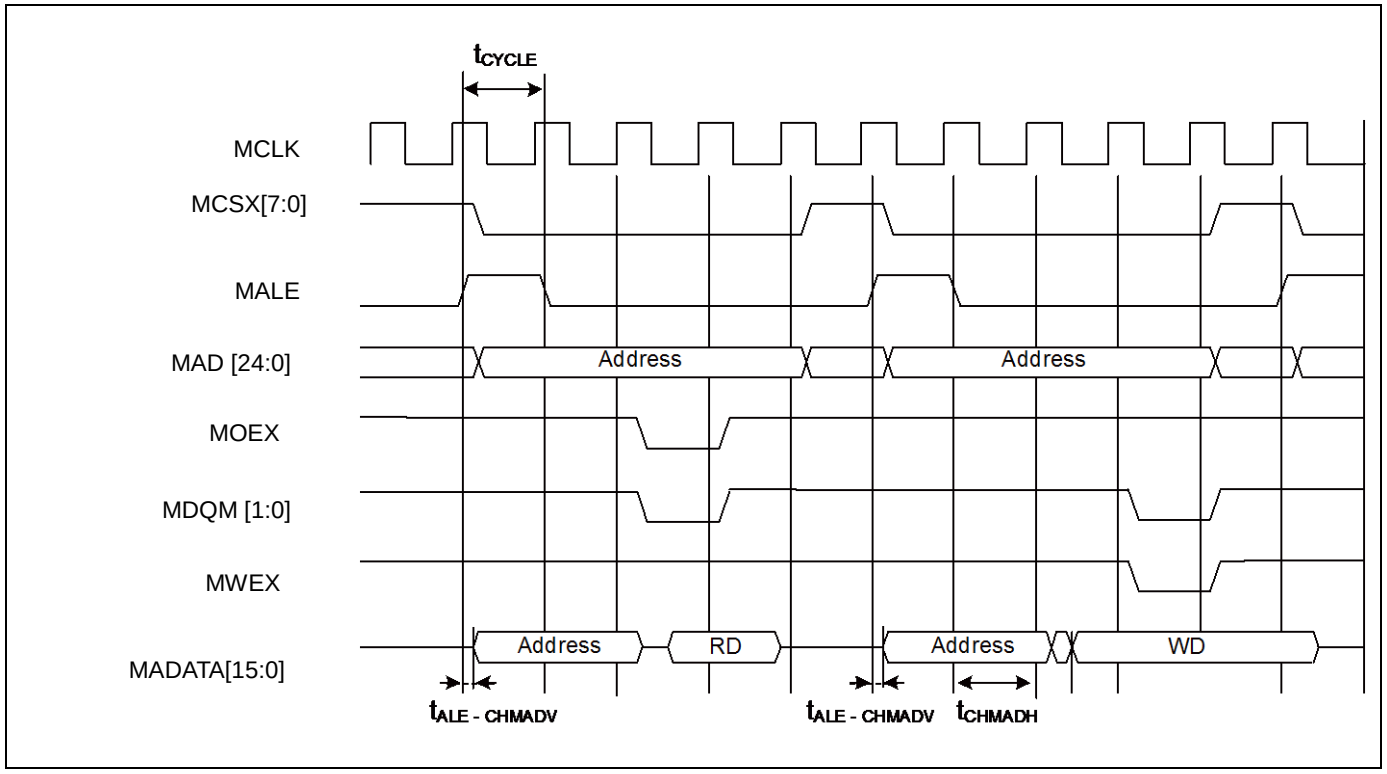

tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH - CSH
tWEH - CSH
tCSL - AV
tOEH - AX
tCSL - AV
tWEH - AX
Address
Address
tCSL - OEL
tOEW
tCSL - RDQML
tCSL -WDQML
tCSL -WEL
tWEW
tDS - OE
tDH - OE
tWEH -DX
RD
Invalid
WD
tCSL -DV

Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 2.7$ V	-2	+10	ns
			$V_{CC} < 2.7$ V		+20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 2.7$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 2.7$ V	MCLK×n+0	MCLK×n+20	

Note: When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).



12.4.11 External Input Timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		INTxx, NMIX	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt NMI
			*3	500	-	ns	
		WKUPx	*4	600	-	ns	Deep standby wake up

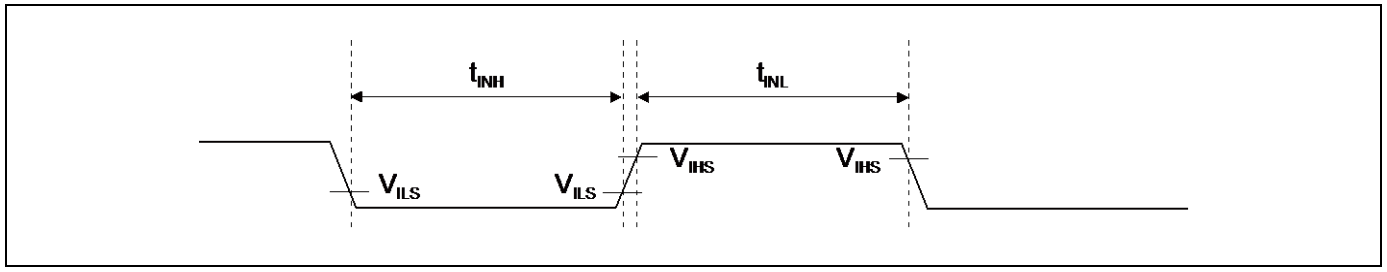
*1 : t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Multi-function Timer is connected to, see Block Diagram in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in Timer mode, in RTC mode, in Stop mode.

*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.

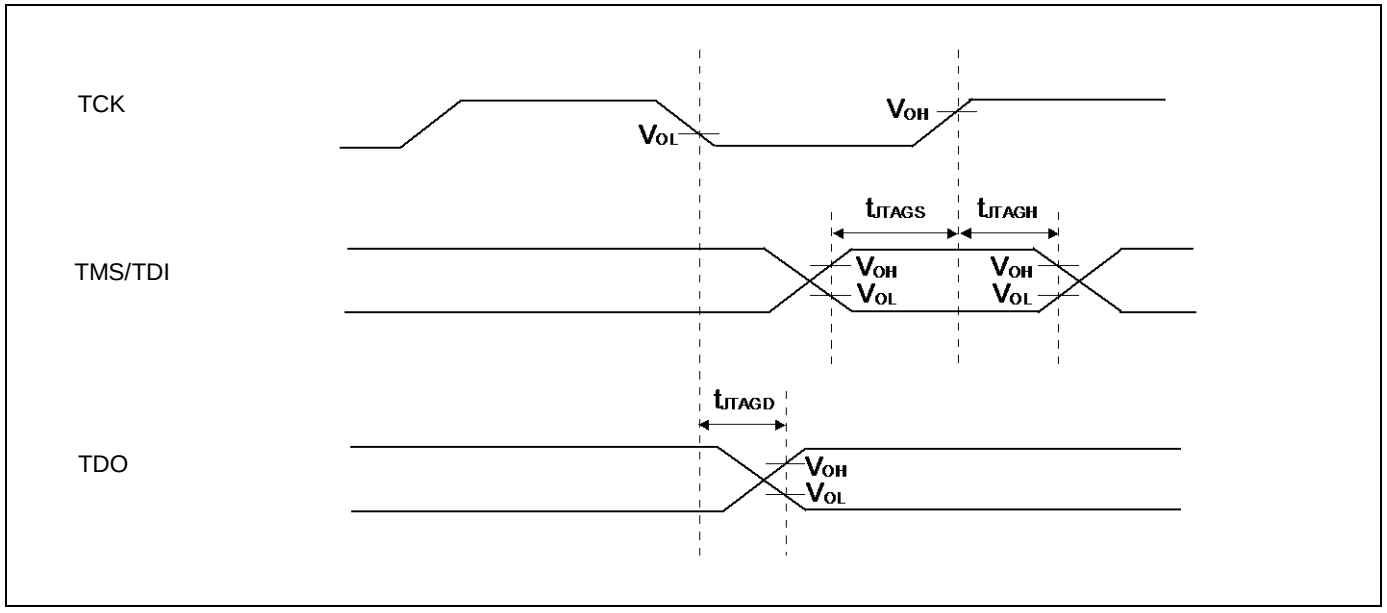


12.4.14 JTAG Timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 2.7$ V	15	-	ns	
			$V_{CC} < 2.7$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 2.7$ V	15	-	ns	
			$V_{CC} < 2.7$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 2.7$ V	-	25	ns	
			$V_{CC} < 2.7$ V	-	45		

Note: When the external load capacitance C_L = 30 pF.



12.8 Flash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(V_{CC} = 1.65V to 3.6V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		30	528	µs	Not including system-level overhead time
Chip erase time		6.8	18	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximam value is guarantee value under 10,000 cycle of erase/write.

12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

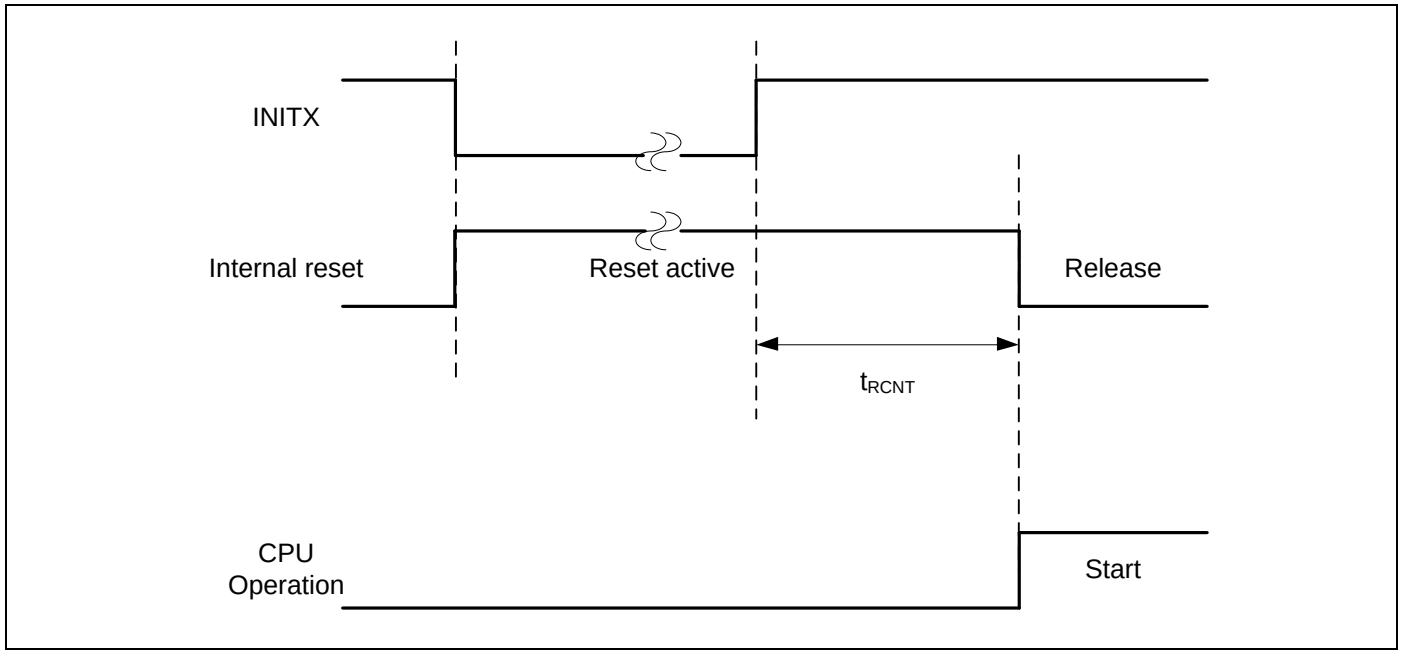
Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{DDI} = 1.1V to 1.3V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

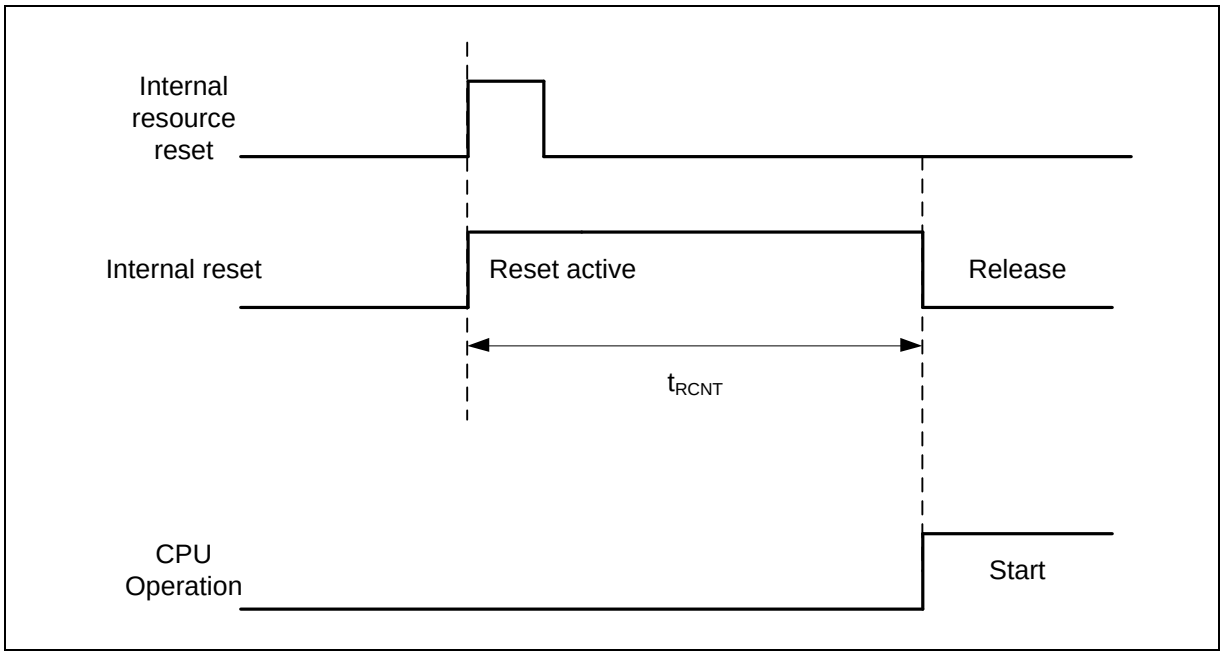
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	148	263	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		148	263	µs	
Low-speed CR Timer mode		258	483	µs	
Sub Timer mode		322	516	µs	
RTC/Stop mode		278	523	µs	
Deep Standby RTC mode		318	603	µs	When RAM is off
Deep Standby Stop mode		278	523	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



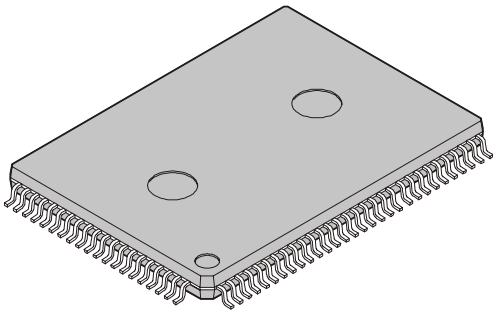
Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

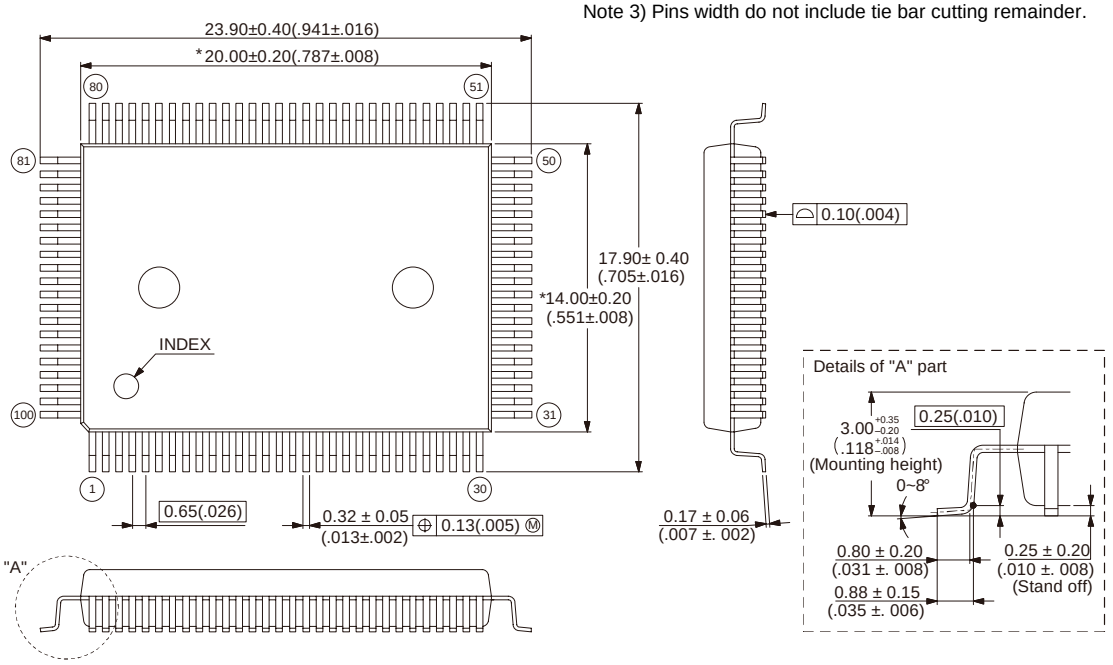
Notes:
- The return factor is different in each Low-Power consumption modes.
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.
- The time during the power-on reset/low-voltage detection reset is excluded. See (6) Power-on Reset Timing in 4. AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.
- When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF341NBPQC-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・QFP 100-pin (0.65mm pitch), (FPT-100P-M36)	Tray
MB9AF342NBPQC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9AF344NBPQC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9AF341NBBGL-GE1	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・PFBGA 112-pin (0.8mm pitch), (BGA-112P-M04)	
MB9AF342NBBGL-GE1	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9AF344NBBGL-GE1	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		

100-pin plastic QFP		
 (FPT-100P-M36)	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14 × 20-0.65

100-pin plastic QFP
(FPT-100P-M36)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The valuesin parentheses are reference values.