Renesas Electronics America Inc - R5F61665D50FPV Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SmartCard, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	92
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61665d50fpv

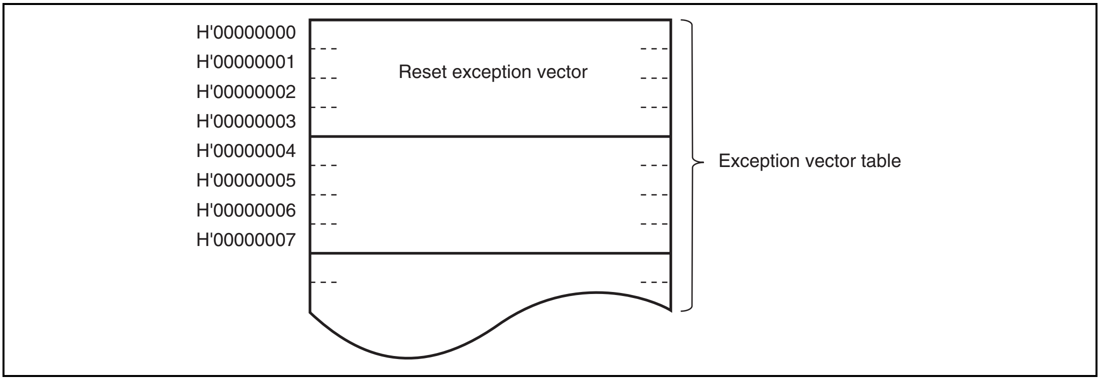


Figure 2.6 Exception Vector Table (Maximum Modes)

The memory indirect (@@aa:8) and extended memory indirect (@@vec:7) addressing modes are used in the JMP and JSR instructions. An 8-bit absolute address included in the instruction code specifies a memory location. Execution branches to the contents of the memory location.

In maximum mode, an operand is a 32-bit (longword) operand, providing a 32-bit branch address.

- Stack Structure

The stack structure of PC at a subroutine branch and that of PC and CCR at an exception handling are shown in figure 2.7. The PC contents are saved or restored in 32-bit units. The EXR contents are saved or restored regardless of whether or not EXR is in use.

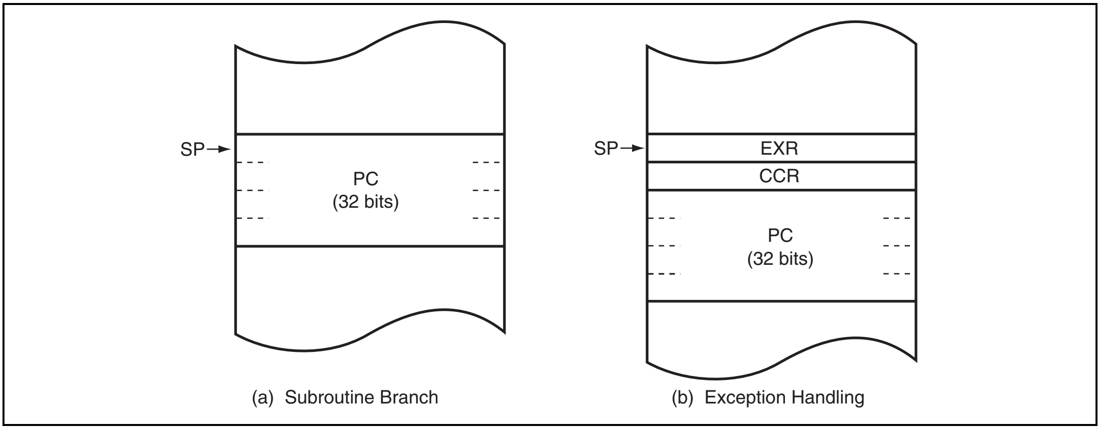


Figure 2.7 Stack Structure (Maximum Mode)

2.8 Addressing Modes and Effective Address Calculation

The H8SX CPU supports the 11 addressing modes listed in table 2.12. Each instruction uses a subset of these addressing modes.

Bit manipulation instructions use register direct, register indirect, or absolute addressing mode to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.12 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:2,ERn)/@(d:16,ERn)/@(d:32,ERn)
4	Index register indirect with displacement	@(d:16, RnL.B)/@(d:16,Rn.W)/@(d:16,ERn.L) @(d:32, RnL.B)/@(d:32,Rn.W)/@(d:32,ERn.L)
5	Register indirect with post-increment	@ERn+
	Register indirect with pre-decrement	@–ERn
	Register indirect with pre-increment	@+ERn
	Register indirect with post-decrement	@ERn–
6	Absolute address	@aa:8/@aa:16/@aa:24/@aa:32
7	Immediate	#xx:3/#xx:4/#xx:8/#xx:16/#xx:32
8	Program-counter relative	@(d:8,PC)/@(d:16,PC)
9	Program-counter relative with index register	@(RnL.B,PC)/@(Rn.W,PC)/@(ERn.L,PC)
10	Memory indirect	@@aa:8
11	Extended memory indirect	@@vec:7

2.8.1 Register Direct—Rn

The operand value is the contents of an 8-, 16-, or 32-bit general register which is specified by the register field in the instruction code.

R0H to R7H and R0L to R7L can be specified as 8-bit registers.

R0 to R7 and E0 to E7 can be specified as 16-bit registers.

ER0 to ER7 can be specified as 32-bit registers.

			Vector Address Offset*1				
Classification	Interrupt Source	Vector Number	Advanced Mode, Middle Mode, Maximum Mode	IPR	Priority	DTC Activation	DMAC Activation
TPU_11	TGI11A	188	H'02F0	IPRO10 to IPRO8	High	O	O
	TGI11B	189	H'02F4		↑	O	—
	TCI11V	190	H'02F8	IPRO6 to IPRO4		—	—
	TCI11U	191	H'02FC			—	—
—	Reserved for system use	192 | 215	H'0300 | H'035C	—		— | —	— | —
IIC2_0	IICI0	216	H'0360	IPRQ6 to IPRQ4		—	—
—	Reserved for system use	217	H'0364			—	—
IIC2_1	IICI1	218	H'0368			—	—
—	Reserved for system use	219	H'036C			—	—
SCI_5	RXI5	220	H'0370	IPRQ2 to IPRQ0		—	O
	TXI5	221	H'0374			—	O
	ERI5	222	H'0378			—	—
	TEI5	223	H'037C			—	—
SCI_6	RXI6	224	H'0380	IPRR14 to IPRR12		—	O
	TXI6	225	H'0384			—	O
	ERI6	226	H'0388			—	—
	TEI6	227	H'038C			—	—
TMR_4	CMIA4 or CMIB4	228	H'0390	IPRR10 to IPRR8		—	—
TMR_5	CMIA5 or CMIB5	229	H'0394			—	—
TMR_6	CMIA6 or CMIB6	230	H'0398			—	—
TMR_7	CMIA7 or CMIB7	231	H'039C		Low	—	—

9.10.6 Controlling Column Address Output Cycle

The number of column address output cycles can be changed from two to three clock cycles by setting the CAST bit in DRAMCR. Set the bit according to the DRAM to be used and the frequency of this LSI so that the $\overline{\text{CAS}}$ pulse width can be optimal.

Figure 9.39 shows a timing example when the number of column address output cycles is set to three clock cycles.

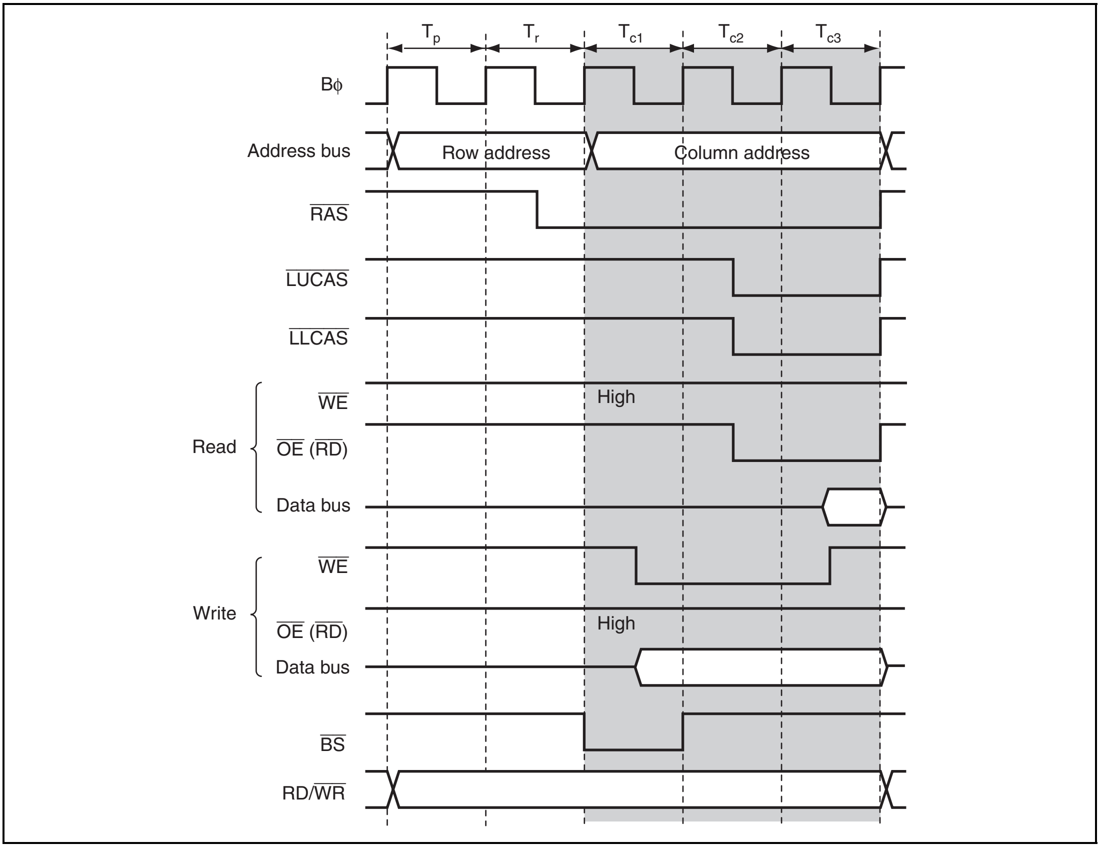
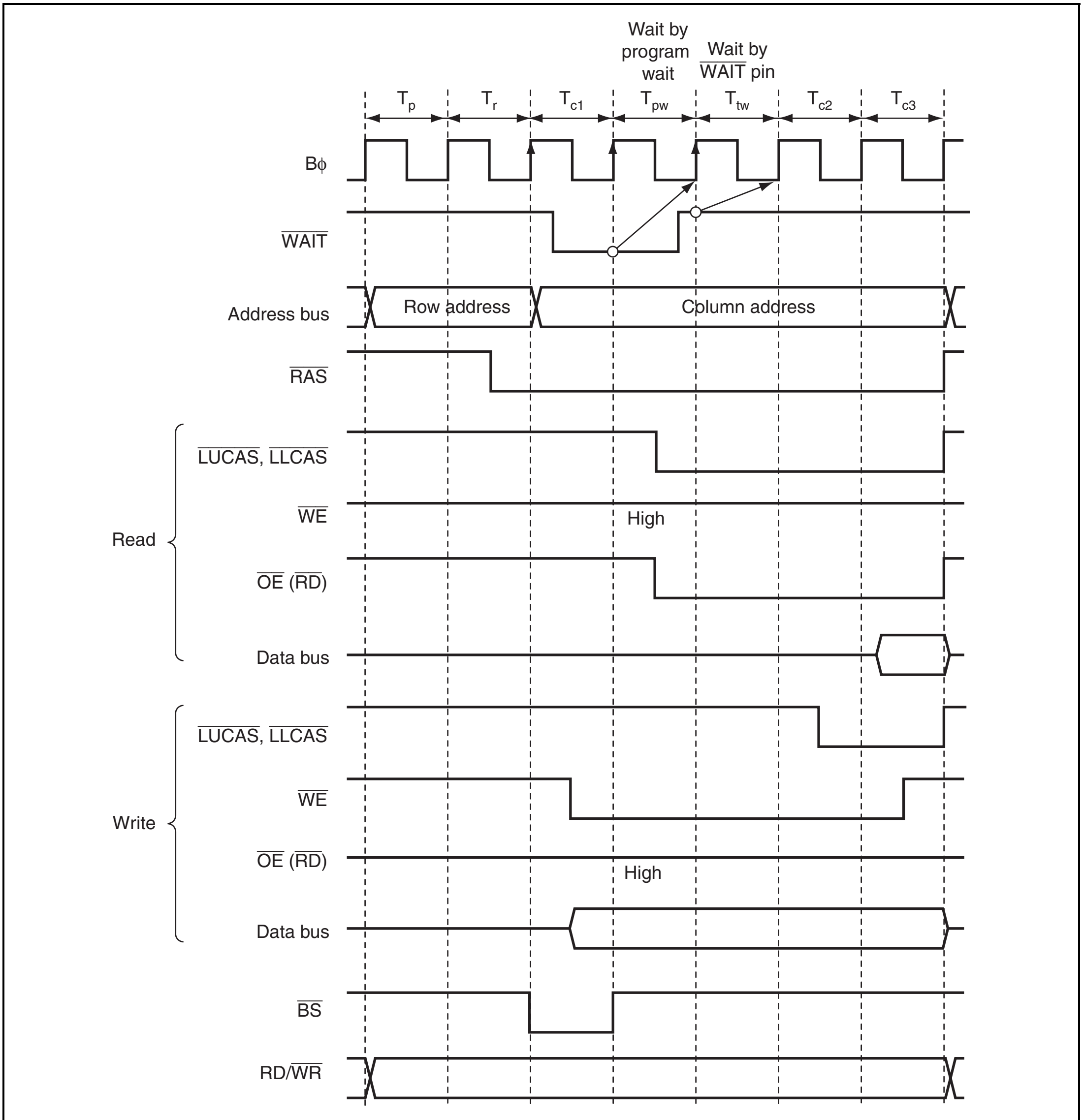


Figure 9.39 Access Timing Example of Column Address Output Cycles for 3 Clock Cycles (RAST = 0)


Wait by program wait
Wait by $\overline{\text{WAIT}}$ pin
T_p
T_r
T_{c1}
T_{pw}
T_{tw}
T_{c2}
T_{c3}
Bφ
$\overline{\text{WAIT}}$
Address bus
Row address
Column address
$\overline{\text{RAS}}$
Read
$\overline{\text{LUCAS}}$, $\overline{\text{LLCAS}}$
$\overline{\text{WE}}$
High
$\overline{\text{OE}}$ ($\overline{\text{RD}}$)
Data bus
Write
$\overline{\text{LUCAS}}$, $\overline{\text{LLCAS}}$
$\overline{\text{WE}}$
$\overline{\text{OE}}$ ($\overline{\text{RD}}$)
High
Data bus
$\overline{\text{BS}}$
RD/$\overline{\text{WR}}$

Note: Upward arrows indicate the timing of $\overline{\text{WAIT}}$ pin sampling.

Figure 9.44 Example of Wait Cycle Insertion Timing for 3-Cycle Column Address Output

10.3.7 DMA Address Control Register (DACR)

DACR specifies the operating mode and transfer method.

Bit	31	30	29	28	27	26	25	24
Bit Name	AMS	DIRS	—	—	—	RPTIE	ARS1	ARS0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Bit Name	—	—	SAT1	SAT0	—	—	DAT1	DAT0
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Bit Name	SARIE	—	—	SARA4	SARA3	SARA2	SARA1	SARA0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	DARIE	—	—	DARA4	DARA3	DARA2	DARA1	DARA0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	AMS	0	R/W	Address Mode Select Selects address mode from single or dual address mode. In single address mode, the $\overline{\text{DACK}}$ pin is enabled according to the DACKE bit. 0: Dual address mode 1: Single address mode
30	DIRS	0	R/W	Single Address Direction Select Specifies the data transfer direction in single address mode. This bit s ignored in dual address mode. 0: Specifies DSAR as source address 1: Specifies DDAR as destination address
29 to 27	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

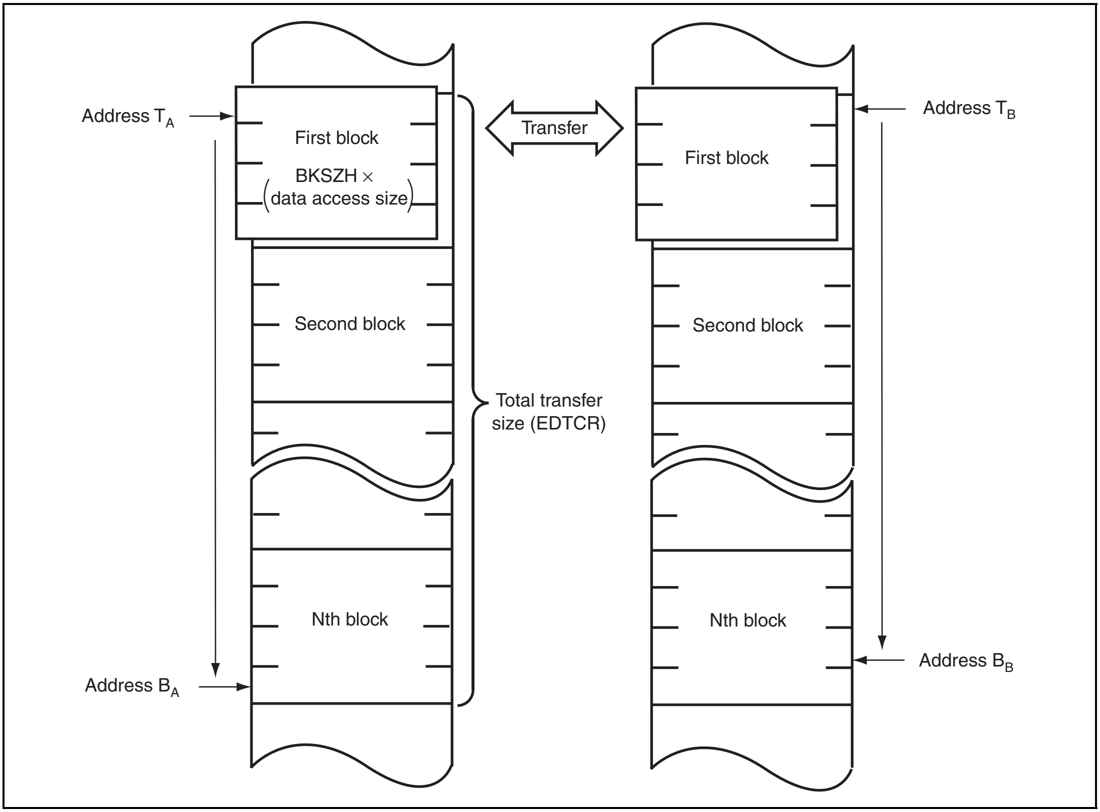


Figure 11.12 Block Transfer Mode Operation in Dual Address Mode (without Block Area Specified)

Table 14.15 TIORL_0

				Description	
Bit 7 IOD3	Bit 6 IOD2	Bit 5 IOD1	Bit 4 IOD0	TGRD_0 Function	TIOCD0 Pin Function*[3]
0	0	0	0	Output compare register*[2]	Output disabled
0	0	0	1		Initial output is 0 output 0 output at compare match
0	0	1	0		Initial output is 0 output 1 output at compare match
0	0	1	1		Initial output is 0 output Toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is 1 output 0 output at compare match
0	1	1	0		Initial output is 1 output 1 output at compare match
0	1	1	1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register*[2]	Capture input source is TIOCD0 pin Input capture at rising edge
1	0	0	1		Capture input source is TIOCD0 pin Input capture at falling edge
1	0	1	x		Capture input source is TIOCD0 pin Input capture at both edges
1	1	x	x		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down*[1]

[Legend]

x: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR_1 are set to B'000 and Pϕ/1 is used as the TCNT_1 count clock, this setting is invalid and input capture is not generated.

2. When the BFB bit in TMDR_0 is set to 1 and TGRD_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

3. In PWM mode 1, the IOD3 to IOD0 settings control output of the TIOCC0 pin functions.

14.3.6 Timer Counter (TCNT)

TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel.

TCNT is initialized to H'0000 by a reset or in hardware standby mode.

TCNT cannot be accessed in 8-bit units. TCNT must always be accessed in 16-bit units.

Bit	15	14	13	12	11	10	9	8
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.3.7 Timer General Register (TGR)

TGR is a 16-bit readable/writable register with a dual function as output compare and input capture registers. The TPU has 16 TGR registers, four each for channels 0 and 3 and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated for operation as buffer registers. The TGR registers cannot be accessed in 8-bit units; they must always be accessed in 16-bit units. TGR and buffer register combinations during buffer operations are TGRA−TGRC and TGRB−TGRD.

Bit	15	14	13	12	11	10	9	8
Bit Name								
Initial Value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name								
Initial Value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 14.5 illustrates periodic counter operation.

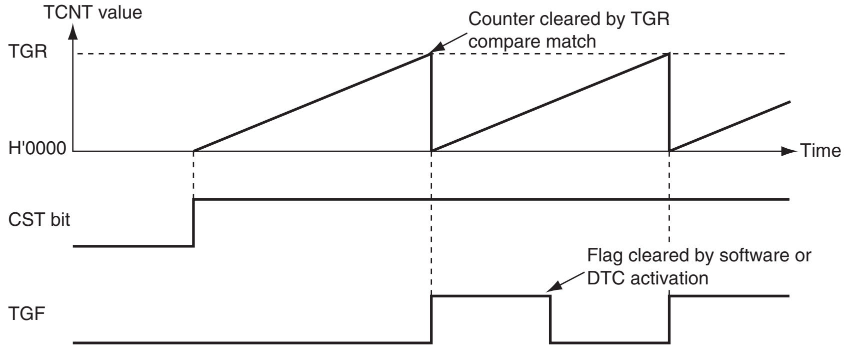

TCNT value
TGR
H'0000
Time
Counter cleared by TGR compare match
CST bit
Flag cleared by software or DTC activation
TGF

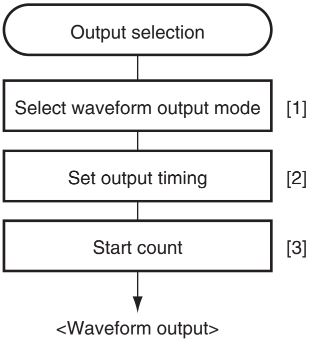
Figure 14.5 Periodic Counter Operation

(2) Waveform Output by Compare Match

The TPU can perform 0, 1, or toggle output from the corresponding output pin using a compare match.

(a) Example of setting procedure for waveform output by compare match

Figure 14.6 shows an example of the setting procedure for waveform output by a compare match.



[1] Select initial value from 0-output or 1-output, and compare match output value from 0-output, 1-output, or toggle-output, by means of TIOR. The set initial value is output on the TIOC pin until the first compare match occurs.

[2] Set the timing for compare match generation in TGR.

[3] Set the CST bit in TSTR to 1 to start the count operation.

Figure 14.6 Example of Setting Procedure for Waveform Output by Compare Match

Bit	Bit Name	Initial Value	R/W	Description
6	CMIEA	0	R/W	Compare Match Interrupt Enable A Selects whether CMFA interrupt requests (CMIA) are enabled or disabled when the CMFA flag in TCSR is set to 1. *[2] 0: CMFA interrupt requests (CMIA) are disabled 1: CMFA interrupt requests (CMIA) are enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable*[3] Selects whether OVF interrupt requests (OVI) are enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt requests (OVI) are disabled 1: OVF interrupt requests (OVI) are enabled
4	CCLR1	0	R/W	Counter Clear 1 and 0*[1]
3	CCLR0	0	R/W	These bits select the method by which TCNT is cleared. 00: Clearing is disabled 01: Cleared by compare match A 10: Cleared by compare match B 11: Cleared at rising edge (TMRIS in TCCR is cleared to 0) of the external reset input or when the external reset input is high (TMRIS in TCCR is set to 1) *[3]
2	CKS2	0	R/W	Clock Select 2 to 0*[1]
1	CKS1	0	R/W	These bits select the clock input to TCNT and count condition. See table 16.2.
0	CKS0	0	R/W	

Notes: 1. To use an external reset or external clock, the DDR and ICR bits in the corresponding pin should be set to 0 and 1, respectively. For details, see section 13, I/O Ports.

2. In unit 2 and unit 3, one interrupt signal is used for CMIEB or CMIEA. For details, see section 16.7, Interrupt Sources.

3. Available only in unit 0 and unit 1.

19.3.11 Serial Extended Mode Register 5 and 6 (SEMR_5 and SEMR_6)

SEMR_5 and SEMR_6 select the clock source in asynchronous mode of SCI_5 and SCI_6. The base clock is automatically specified when the average transfer rate operation is selected. TMO output in TMR unit 2 and unit 3 can also be set as the serial transfer base clock. Figure 19.3 describes the examples of base clock features when the average transfer rate operation is selected. Figure 19.4 describes the examples of base clock features when the TMO output in TMR is selected.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	ABCS	ACS3	ACS2	ACS1	ACS0
Initial Value	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	Undefined	R	Reserved These bits are always read as undefined and cannot be modified.
4	ABCS	0	R/W	Asynchronous Mode Base Clock Select (valid only in asynchronous mode) Selects the base clock for a 1-bit period. 0: The base clock has a frequency 16 times the transfer rate 1: The base clock has a frequency 8 times the transfer rate
3 2 1 0	ACS3 ACS2 ACS1 ACS0	0 0 0 0	R/W R/W R/W R/W	Asynchronous Mode Clock Source Select These bits select the clock source for the average transfer rate function in the asynchronous mode. When the average transfer rate function is enabled, the base clock is automatically specified regardless of the ABCS bit value. The average transfer rate only corresponds to 8MHz, 10.667MHz, 12MHz, 16MHz, 24MHz, and 32MHz. No other clock is available. Setting of ACS3 to ACS0 must be done in the asynchronous mode (the $C/\overline{A}$ bit in SMR = 0) and the external clock input mode (the CKE bit I SCR = 1). The setting examples are in figures 19.3 and 19.4. (Each number in the four-digit number below corresponds to the value in the bits ACS3 to ACS0 from left to right respectively.)

20.3.5 Interrupt Select Register 1 (ISR1)

ISR1 selects the vector numbers of the interrupt requests indicated in interrupt flag register 1 (IFR1). If the USB issues an interrupt request to the INTC when a bit in ISR1 is cleared to 0, the interrupt corresponding to the bit will be USBINTN2. If the USB issues an interrupt request to the INTC when a bit in ISR1 is set to 1, the corresponding interrupt will be USBINTN3.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	—	—	EP3 TR	EP3 TS	VBUSF
Initial Value	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	—	0	R	
5	—	0	R	
4	—	0	R	
3	—	0	R	
2	EP3 TR	1	R/W	EP3 Transfer Request
1	EP3 TS	1	R/W	EP3 Transmission Complete
0	VBUSF	1	R/W	USB Bus Connect

(b) Programming

FPFR indicates the return value of the programming result.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	MD	EE	FK	—	WD	WA	SF

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	—	Unused Returns 0.
6	MD	—	R/W	Programming Mode Related Setting Error Detect Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be confirmed with the FLER bit in FCCS. For conditions to enter the error protection state see section 25.9.3, Error Protection. 0: Normal operation (FLER = 0) 1: Error protection state, and programming cannot be performed (FLER = 1)
5	EE	—	R/W	Programming Execution Error Detect Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this bit is set to 1, there is a high possibility that the user MAT has been written to partially. In this case, after removing the error factor, erase the user MAT. If FMATS is set to H'AA and the user boot MAT is selected, an error occurs when programming is performed. In this case, both the user MAT and user boot MAT have not been written to. Programming the user boot MAT should be performed in boot mode or programmer mode. 0: Programming has ended normally 1: Programming has ended abnormally (programming result is not guaranteed)

3. Programming/erasing state

   Programming and erasure by the boot program take place in this state. The boot program is made to transfer the programming/erasing programs to the on-chip RAM by commands from the host. Sum checks and blank checks are executed by sending these commands from the host.

These boot program states are shown in figure 25.23.

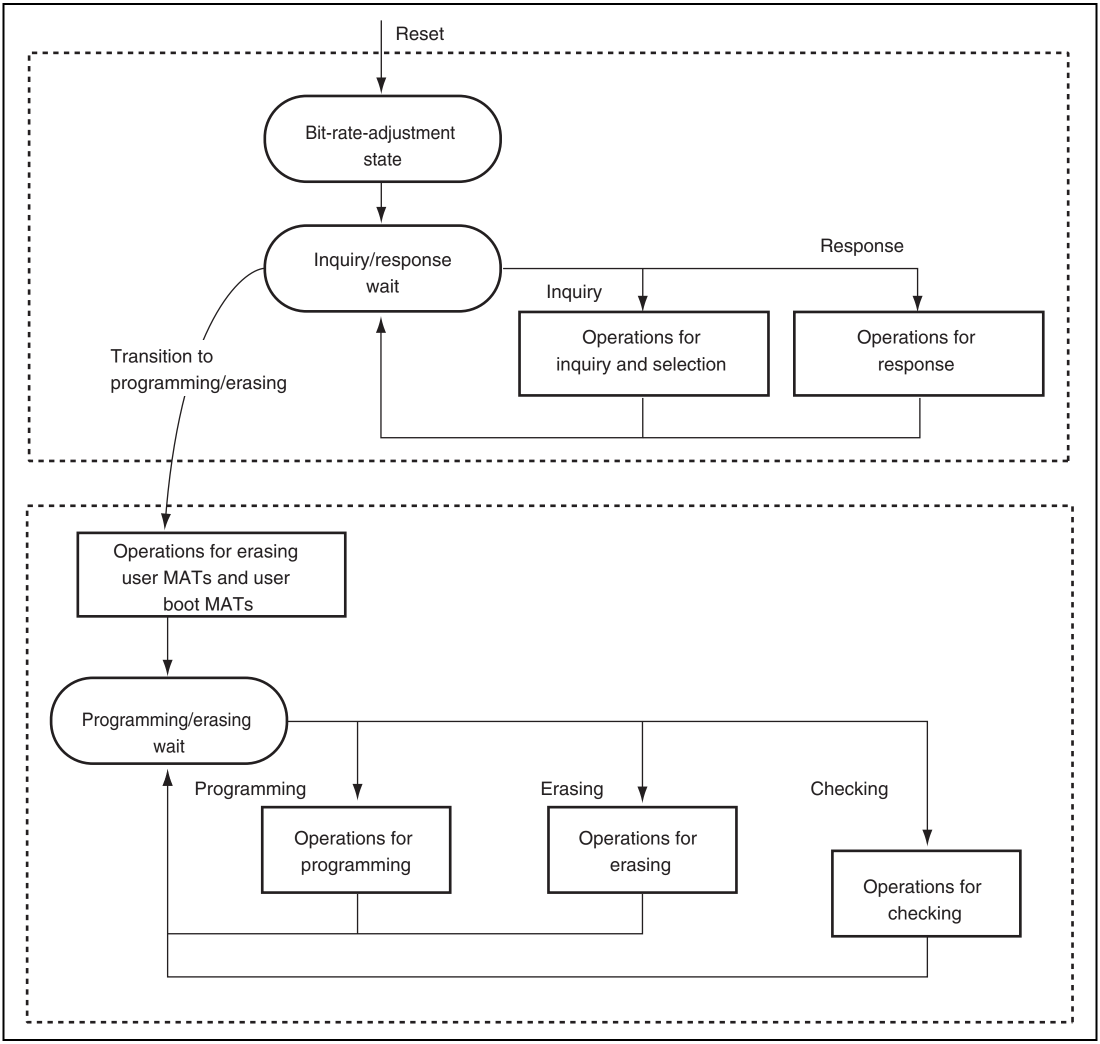

Reset
Bit-rate-adjustment state
Inquiry/response wait
Response
Inquiry
Operations for inquiry and selection
Operations for response
Transition to programming/erasing
Operations for erasing user MATs and user boot MATs
Programming/erasing wait
Programming
Erasing
Checking
Operations for programming
Operations for erasing
Operations for checking

Figure 25.23 Boot Program States

12. A programming/erasing program for the flash memory used in a conventional F-ZTAT H8, H8S microcomputer which does not support download of the on-chip program by setting the SCO bit in FCCS to 1 cannot run in this LSI. Be sure to download the on-chip program to execute programming/erasure of the flash memory in this F-ZTAT H8SX microcomputer.
13. Unlike a conventional F-ZTAT H8 or H8S microcomputers, measures against a program crash are not taken by WDT while programming/erasing and downloading a programming/erasing program. When needed, measures should be taken by user. A periodic interrupt generated by the WDT can be used as the measures, as an example. In this case, the interrupt generation period should take into consideration time to program/erase the flash memory.
14. When downloading the programming/erasing program, do not clear the SCO bit in FCCS to 0 immediately after setting it to 1. Otherwise, download cannot be performed normally. Immediately after executing the instruction to set the SCO bit to 1, dummy read of the FCCS must be executed twice.
15. The contents of general registers ER0 and ER1 are not saved during download of an on-chip program, initialization, programming, or erasure. When needed, save the general registers before a download request or before execution of initialization, programming, or erasure using the procedure program.

Note: * The oscillation settling time, which includes a period where the oscillation by an oscillator is not stable, depends on the resonator characteristics.
The above figures are for reference.

28.8.6 Deep Software Standby Mode Application Example

(1) Transition to and Exit from Deep Software Standby Mode

Figure 28.4 shows an example where the transition to deep software standby mode is initiated by a falling edge on the NMI pin and exit from deep software standby mode is initiated by a rising edge on the NMI pin.

In this example, falling-edge sensing of NMI interrupts has been specified by clearing the NMIEG bit in INTCR to 0 (not shown). After an NMI interrupt has been sensed, rising-edge sensing is specified by setting the DNMIEG bit to 1, the SSBY and DPSBY bits are set to 1, and the transition to deep software standby mode is triggered by execution of a SLEEP instruction.

After that, deep software standby mode is canceled at the rising edge on the NMI pin.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
SSR_0*[1]	TDRE	RDRF	ORER	FER (ERS)	PER	TEND	MPB	MPBT	SCI_0
RDR_0									
SCMR_0	—	—	—	—	SDIR	SINV	—	SMIF	
SMR_1*[1]	C/$\overline{A}$ (GM)	CHR (BLK)	PE (PE)	O/$\overline{E}$ (O/$\overline{E}$)	STOP (BCP1)	MP (BCP0)	CKS1	CKS0	SCI_1
BRR_1									
SCR_1*[1]	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_1									
SSR_1*[1]	TDRE	RDRF	ORER	FER (ERS)	PER	TEND	MPB	MPBT	
RDR_1									
SCMR_1	—	—	—	—	SDIR	SINV	—	SMIF	
ADDRA_0									A/D_0
ADDRB_0									
ADDRC_0									
ADDRD_0									
ADDRE_0									
ADDRF_0									
ADDRG_0									
ADDRH_0									

Item	Page	Revision (See Manual for Details)
Section 22 A/D Converter 22.4 Operation 22.4.2 Scan Mode	1082	Note amended (1) Continuous Scan Mode … Notes: 1. Only possible in unit 0. 2. As conversion start trigger, units 0 and 1 of TMR, and units 2 and 3 of TMR are available in unit 0, and unit 1, respectively. 3. Unit 0: The full-spec emulator (E6000H) should not be used, but the on-chip emulator (E10A-USB) is usable.
22.4.3 Input Sampling and A/D Conversion Time	1086 to 1088	The following tables replaced Table 22.3 Characteristics of A/D Conversion (Unit 0: when EXCKS* = 0, ICKSEL = 0, and ADSSTR* = H'0F) (1) Table 22.3 Characteristics of A/D Conversion (Unit 0: when EXCKS* = 1, ICKSEL = 0, and ADSSTR* = H'0F) (2) Table 22.4 Characteristics of A/D Conversion (Unit 1: when EXCKS = 0, ICKSEL = 0, and ADSSTR* = H'0F) (1) Table 22.4 Characteristics of A/D Conversion (Unit 1: when EXCKS = 1, ICKSEL = 0, and ADSSTR* = H'0F) (2) Table 22.5 Characteristics of A/D Conversion (When EXCKS*[1] = 1, ICKSEL*[1] = 0, and ADSSTR*[2] = H'19)
Table 22.6 Period of A/D Conversion (Scan Mode) (Units 0 and 1)	1089	Note deleted Notes: 1. Make the sampling setting15 (ADSSRT = D'15). 2. When Pϕ = Iϕ/2, make the sampling setting 25 (ADSSRT = D'25). 3. Unit 0: The full-spec emulator (E6000H) should not be used, but the on-chip emulator (E10A-USB) is usable. 4. ~~Unit 0: The full-spec emulator (E6000H) should not be used, but the on-chip emulator (E10A-USB) is usable.~~ Unit 1: Access to the full-spec emulator (E6000H) is prohibited but the on-chip emulator (E10A-USB) is usable.