Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SmartCard, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	92
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61665mn50fpv

Classification	Instruction	Size	Addressing Mode								
			#xx	Rn	@ERn	@(d,ERn)	@(d, RnL.B/ Rn.W/ ERn.L)	@–ERn/ @ERn+/ @ERn–/ @+ERn	@aa:8	@aa:16/ @aa:32	—
Bit manipulation	BFLD	B		D	S				S	S	
	BFST	B		S	D				D	D	
Branch	BRA/BS, BRA/BC*[8]	B			S				S	S	
	BSR/BS, BSR/BC*[8]	B			S				S	S	
System control	LDC (CCR, EXR)	B/W*[9]	S	S	S	S		S*[10]		S	
	LDC (VBR, SBR)	L		S							
	STC (CCR, EXR)	B/W*[9]		D	D	D		D*[11]		D	
	STC (VBR, SBR)	L		D							
	ANDC, ORC, XORC	B	S								
	SLEEP	—									O
	NOP	—									O

[Legend]

d: d:16 or d:32

S: Can be specified as a source operand.

D: Can be specified as a destination operand.

SD: Can be specified as either a source or destination operand or both.

S/D: Can be specified as either a source or destination operand.

S:4: 4-bit immediate data can be specified as a source operand.

Notes:
1. Only @aa:16 is available.
2. @ERn+ as a source operand and @–ERn as a destination operand
3. Specified by ER5 as a source address and ER6 as a destination address for data transfer.
4. Size of data to be added with a displacement
5. Only @ERn– is available
6. When the number of bits to be shifted is 1, 2, 4, 8, or 16
7. When the number of bits to be shifted is specified by 5-bit immediate data or a general register
8. Size of data to specify a branch condition
9. Byte when immediate or register direct, otherwise, word
10. Only @ERn+ is available
11. Only @–ERn is available
12. Only when the multiplier is available.

Table 2.9 Bit Manipulation Instructions

Instruction	Size	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in the contents of a general register or a memory location to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BSET/cc	B	if cc, 1 → (<bit-No.> of <EAd>) If the specified condition is satisfied, this instruction sets a specified bit in a memory location to 1. The bit number can be specified by 3-bit immediate data, or by the lower three bits of a general register. The Z flag status can be specified as a condition.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in the contents of a general register or a memory location to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR/cc	B	if cc, 0 → (<bit-No.> of <EAd>) If the specified condition is satisfied, this instruction clears a specified bit in a memory location to 0. The bit number can be specified by 3-bit immediate data, or by the lower three bits of a general register. The Z flag status can be specified as a condition.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in the contents of a general register or a memory location. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in the contents of a general register or a memory location and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the carry flag with a specified bit in the contents of a general register or a memory location and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BIAND	B	C ∧ [~ (<bit-No.> of <EAd>)] → C ANDs the carry flag with the inverse of a specified bit in the contents of a general register or a memory location and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in the contents of a general register or a memory location and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

9.10.5 Basic Timing

Figure 9.38 shows a basic access timing of the DRAM space.

A basic bus cycle consists of four clock cycles: one precharge cycle (Tp), one row address output cycle (Tr), and two column address output cycles (Tc1 and Tc2).

The $\overline{RD}$ signal is output to DRAM as an $\overline{OE}$ signal on a DRAM access. When DRAM with the EDO page mode function is in use, connect the $\overline{OE}$ signal to the $\overline{OE}$ pin of the DRAM.

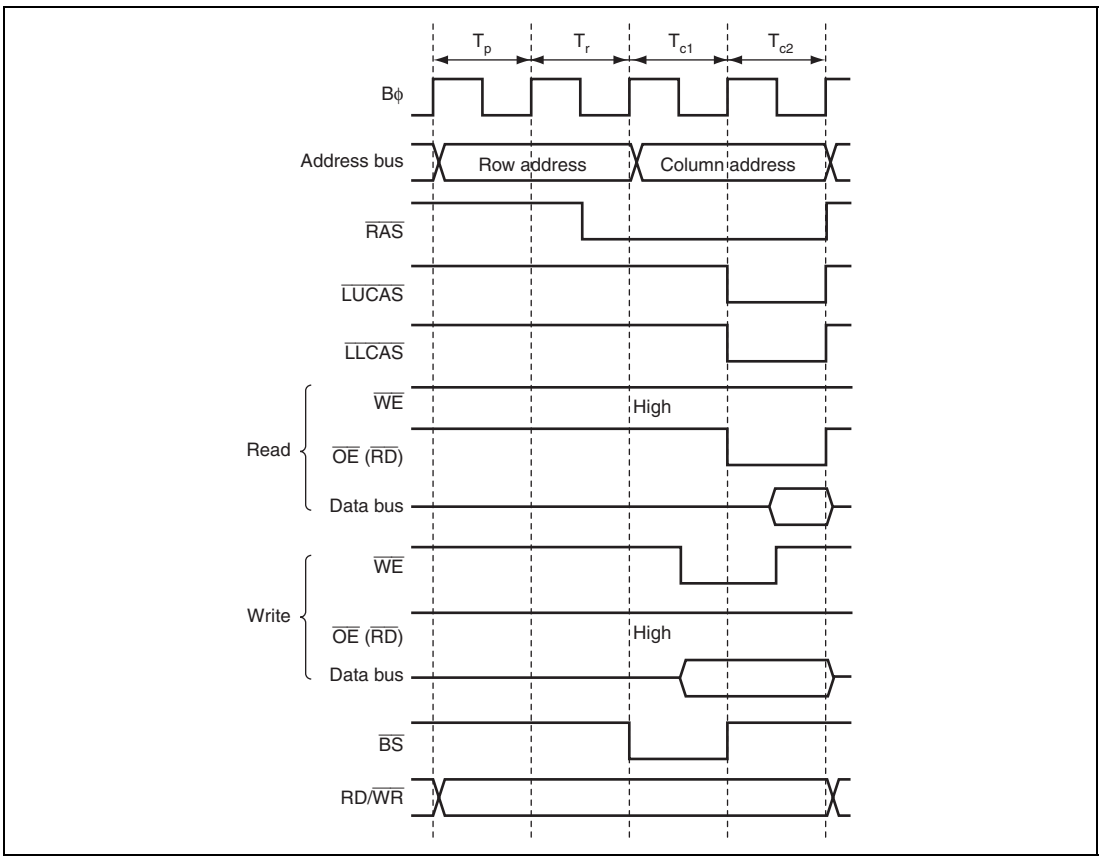


Figure 9.38 DRAM Basic Access Timing (RAS = 0 and CAST = 0)

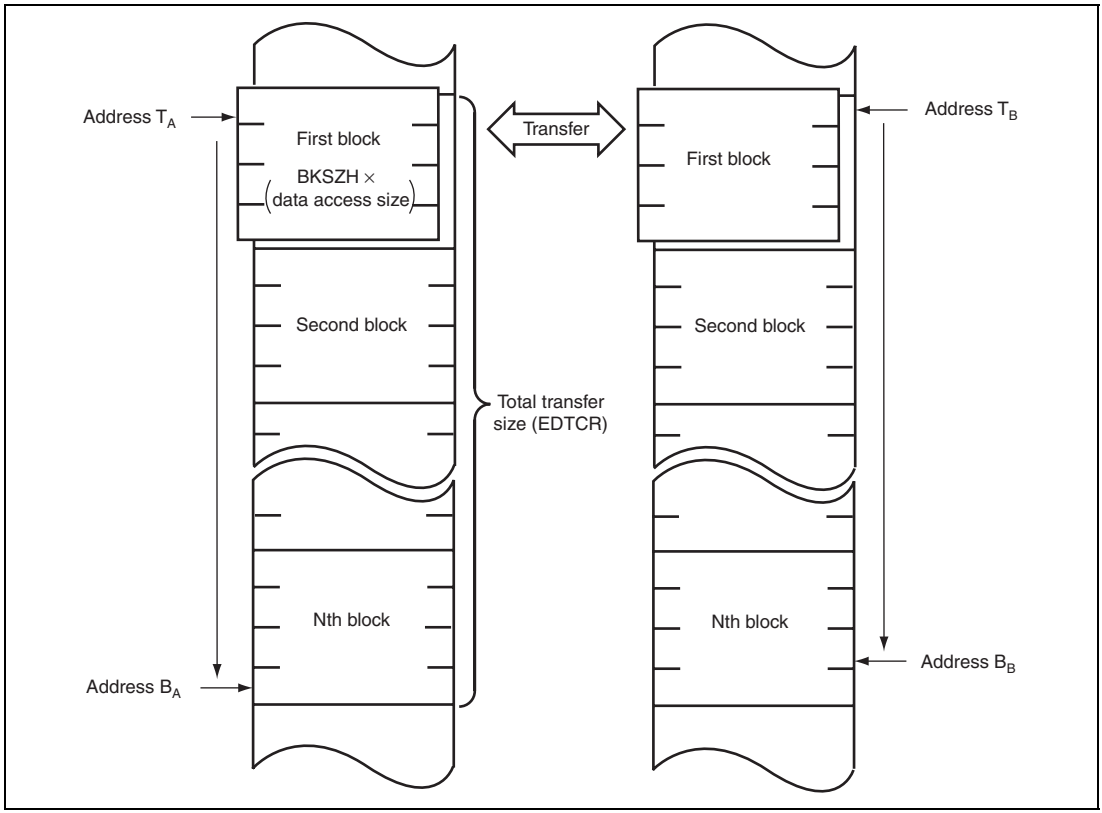


Figure 11.12 Block Transfer Mode Operation in Dual Address Mode (without Block Area Specified)

11.5.3 Activation Sources

The EXDMAC is activated by an auto request or an external request. This activation source is selected by the DTF1 or DTF0 bit in EDMDR.

(1) Activation by Auto-Request

The transfer request signal is automatically generated in EXDMAC with auto-request activation when no transfer request signal is generated from external or peripheral modules, incase of transfer among memory or between memory and peripheral modules that cannot generate the transfer request signal. The transfer starts when the DTE bit in EDMDR is set to 1 with auto-request activation. The bus mode can be selected from cycle steal mode and burst mode with auto-request activation.

(2) Activation by External Request

Transfer is started by the transfer request signal ($\overline{\text{EDREQ}}$) from the external device for activation by an external request. When the EXDMA transfer is enabled (DTE = 1), the EXDMA transfer starts by $\overline{\text{EDREQ}}$ input.

The transfer request signal is accepted by the $\overline{\text{EDREQ}}$ pin. The EDREQS bit in EDMDR selects whether the $\overline{\text{EDREQ}}$ is detected by falling edge sensing or low level sensing.

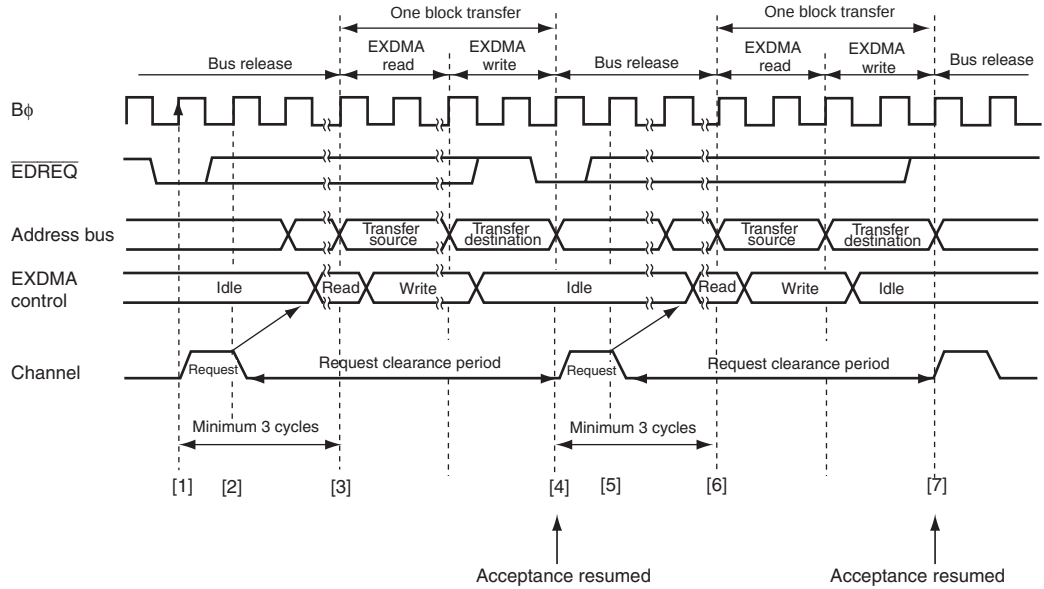
When the EDRAKE bit in EDMDR is set to 1, the signal notifying transfer request acceptance is output from the $\overline{\text{EDRAK}}$ pin. The $\overline{\text{EDRAK}}$ signal is accepted for one external request and is output when transfer processing starts.

When specifying an external request as an activation source, set the DDR bit to 0 and the ICR bit to 1 on the corresponding pin in advance. For details, see section 13, I/O Ports.

Figure 11.30 shows an example of block transfer mode transfer activated by the $\overline{\text{EDREQ}}$ pin falling edge.

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of Bϕ after the end of the DTE bit write cycle.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance of a transfer request via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared, and $\overline{\text{EDREQ}}$ pin high level sampling for edge sensing is started. If $\overline{\text{EDREQ}}$ pin high level sampling is completed by the end of the EXDMA write cycle, acceptance resumes after the end of the write cycle, and $\overline{\text{EDREQ}}$ pin low level sampling is performed again. This sequence of operations is repeated until the end of the transfer.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of Bϕ, and request is held.
[2], [5] Request is cleared at end of next bus cycle, and activation is started in EXDMAC.
[3], [6] EXDMA cycle starts; $\overline{\text{EDREQ}}$ pin high level sampling is started at rise of Bϕ.
[4], [7] When $\overline{\text{EDREQ}}$ pin high level has been sampled, acceptance is resumed after completion of write cycle.
(As in [1], $\overline{\text{EDREQ}}$ pin low level is sampled at rise of Bf, and request is held.)

Figure 11.30 Example of Block Transfer Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Falling Edge

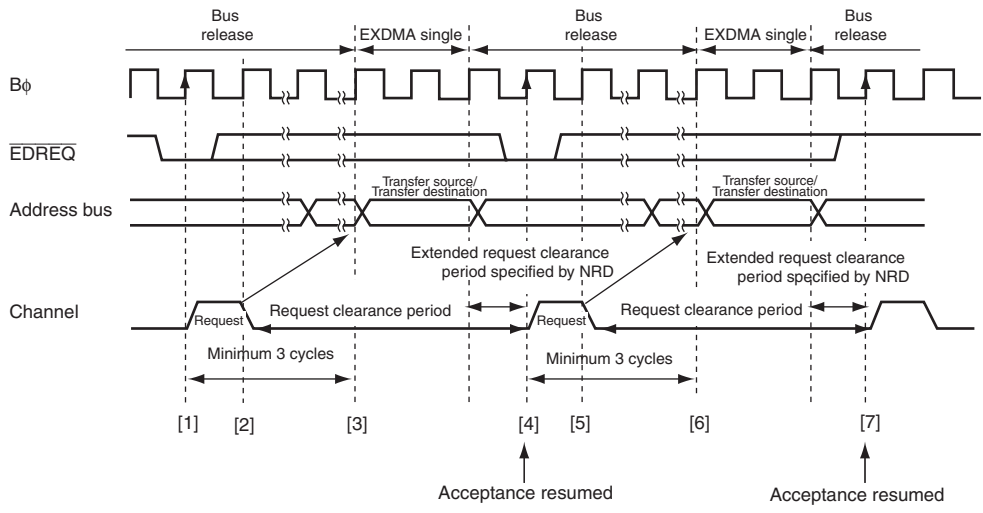
(5) $\overline{\text{EDREQ}}$ Pin Low Level Activation Timing with NRD = 1 Specified

When the NRD bit is set to 1 in EDMDR, the acceptance timing of the next transfer request can be delayed one cycle later.

Figure 11.38 shows an example of single address mode transfer activated by the $\overline{\text{EDREQ}}$ pin low level with NRD = 1 specified.

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of Bϕ after the end of the DTE bit write cycle.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance of a transfer request via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared. After the end of the single cycle, acceptance resumes when one cycle of the request clearance period specified by NRD = 1 expires and $\overline{\text{EDREQ}}$ pin low level sampling is performed again. This sequence of operations is repeated until the end of the transfer.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of Bϕ, and request is held.
[2], [5] Request is cleared at end of next bus cycle, and activation is started in EXDMAC.
[3], [6] EXDMA cycle starts.
[4], [7] Acceptance is resumed after completion of write cycle plus one cycle.
(As in [1], $\overline{\text{EDREQ}}$ pin low level is sampled at rise of Bϕ, and request is held.)

Figure 11.38 Example of Single Address Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Low Level with NRD = 1 Specified

4. Activation Source Acceptance

   At the start of activation source acceptance, low level sensing is used for both falling edge sensing and low level sensing on the $\overline{\text{EDREQ}}$. Therefore, a request is accepted in the case of a low level at the $\overline{\text{EDREQ}}$ pin that occurs before execution of the EDMDR write for setting the transfer-enabled state.

   At EXDMAC activation, low level on the $\overline{\text{EDREQ}}$ pin must not remain at the end of the previous transfer.

5. Conflict in Cluster Transfer

   In cluster transfer mode, the same cluster buffer is used for all channels. When more than one cluster transfer conflicts, the cluster buffer register holds the value of the last cluster transfer. When the transfer between the transfer source/destination and the cluster buffer conflicts with another cluster transfer, the transferred data in the cluster buffer may be overwritten by another channel cluster transfer. Therefore, in the cluster transfer mode (single address mode), do not set the cluster transfer mode for any other channels.

6. Cluster Transfer Mode and Endian

   In cluster transfer mode, only a transfer to the areas in the big endian format is supported. When cluster transfer mode is specified, do not specify the areas in the little endian format for EDSAR and EDDAR. For details on the endian, see section 9, Bus Controller (BSC).

Table 12.1 shows correspondence between the DTC activation source and vector address.

Table 12.1 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*	Priority
External pin	IRQ0	64	H'500	DTCEA15	High
	IRQ1	65	H'504	DTCEA14	
	IRQ2	66	H'508	DTCEA13	
	IRQ3	67	H'50C	DTCEA12	
	IRQ4	68	H'510	DTCEA11	
	IRQ5	69	H'514	DTCEA10	
	IRQ6	70	H'518	DTCEA9	
	IRQ7	71	H'51C	DTCEA8	
	IRQ8	72	H'520	DTCEA7	
	IRQ9	73	H'524	DTCEA6	
	IRQ10	74	H'528	DTCEA5	
	IRQ11	75	H'52C	DTCEA4	
A/D_0	ADI0 (A/D_0 conversion end)	86	H'558	DTCEB15	
TPU_0	TGI0A	88	H'560	DTCEB13	
	TGI0B	89	H'564	DTCEB12	
	TGI0C	90	H'568	DTCEB11	
	TGI0D	91	H'56C	DTCEB10	
TPU_1	TGI1A	93	H'574	DTCEB9	
	TGI1B	94	H'578	DTCEB8	
TPU_2	TGI2A	97	H'584	DTCEB7	
	TGI2B	98	H'588	DTCEB6	Low

Table 12.3 Chain Transfer Conditions

1st Transfer				2nd Transfer				
CHNE	CHNS	DISEL	Transfer Counter*1	CHNE	CHNS	DISEL	Transfer Counter*1	DTC Transfer
0	—	0	Not 0	—	—	—	—	Ends at 1st transfer
0	—	0	0*2	—	—	—	—	Ends at 1st transfer
0	—	1		—	—	—	—	Interrupt request to CPU
1	0	—	—	0	—	0	Not 0	Ends at 2nd transfer
				0	—	0	0*2	Ends at 2nd transfer
				0	—	1	—	Interrupt request to CPU
1	1	0	Not 0	—	—		—	Ends at 1st transfer
1	1	—	0*2	0	—	0	Not 0	Ends at 2nd transfer
				0	—	0	0*2	Ends at 2nd transfer
				0	—	1		Interrupt request to CPU
1	1	1	Not 0	—	—	—	—	Ends at 1st transfer
								Interrupt request to CPU

Notes: 1. CRA in normal mode transfer, CRAL in repeat transfer mode, or CRB in block transfer mode
2. When the contents of the CRAH is written to the CRAL in repeat transfer mode

12.5.1 Bus Cycle Division

When the transfer data size is word and the SAR and DAR values are not a multiple of 2, the bus cycle is divided and the transfer data is read from or written to in bytes. Similarly, when the transfer data size is longword and the SAR and DAR values are not a multiple of 4, the bus cycle is divided and the transfer data is read from or written to in words.

Table 12.4 shows the relationship among, SAR, DAR, transfer data size, bus cycle divisions, and access data size. Figure 12.5 shows the bus cycle division example.

Table 12.4 Number of Bus Cycle Divisions and Access Size

	Specified Data Size		
SAR and DAR Values	Byte (B)	Word (W)	Longword (LW)
Address 4n	1 (B)	1 (W)	1 (LW)
Address 2n + 1	1 (B)	2 (B-B)	3 (B-W-B)
Address 4n + 2	1 (B)	1 (W)	2 (W-W)

14.3.3 Timer I/O Control Register (TIOR)

TIOR controls TGR. The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.

The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTR is cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.

When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

To designate the input capture pin in TIOR, the DDR bit and ICR bit for the corresponding pin should be set to 0 and 1, respectively. For details, see section 13, I/O Ports.

- TIORH_0, TIOR_1, TIOR_2, TIORH_3, TIOR_4, TIOR_5

Bit	7	6	5	4	3	2	1	0
Bit Name	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- TIORL_0, TORL_3

Bit	7	6	5	4	3	2	1	0
Bit Name	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.10.5 Conflict between TCNT Write and Increment Operations

If incrementing occurs in the T2 state of a TCNT write cycle, the TCNT write takes precedence and TCNT is not incremented. Figure 14.48 shows the timing in this case.

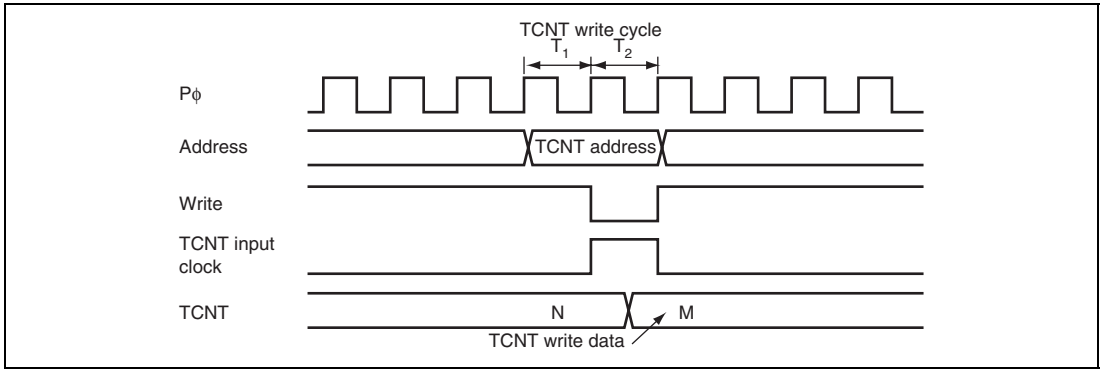


Figure 14.48 Conflict between TCNT Write and Increment Operations

14.10.6 Conflict between TGR Write and Compare Match

If a compare match occurs in the T2 state of a TGR write cycle, the TGR write takes precedence and the compare match signal is disabled. A compare match also does not occur when the same value as before is written.

Figure 14.49 shows the timing in this case.

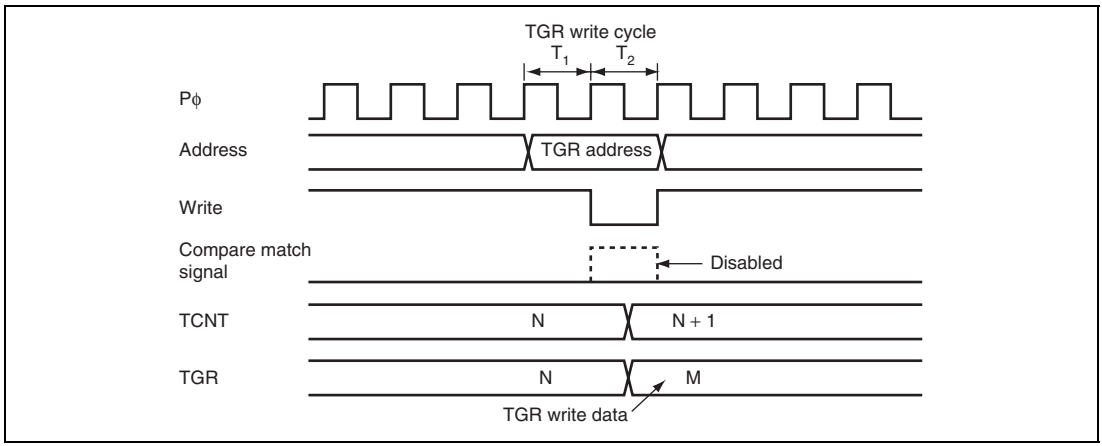


Figure 14.49 Conflict between TGR Write and Compare Match

Section 18 Watchdog Timer (WDT)

The watchdog timer (WDT) is an 8-bit timer that outputs an overflow signal ($\overline{\text{WDTOVF}}$) if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow. At the same time, the WDT can also generate an internal reset signal.

When this watchdog function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows.

Figure 18.1 shows a block diagram of the WDT.

18.1 Features

- Selectable from eight counter input clocks
- Switchable between watchdog timer mode and interval timer mode
  - In watchdog timer mode

    If the counter overflows, the WDT outputs $\overline{\text{WDTOVF}}$. It is possible to select whether or not the entire LSI is reset at the same time.
  - In interval timer mode

    If the counter overflows, the WDT generates an interval timer interrupt (WOVI).

(2) Resume Operation from Up-Stream

If the USB bus enters the non-suspend state from the suspend state by resume signal output from up-stream, perform the operation as shown in figure 20.5.

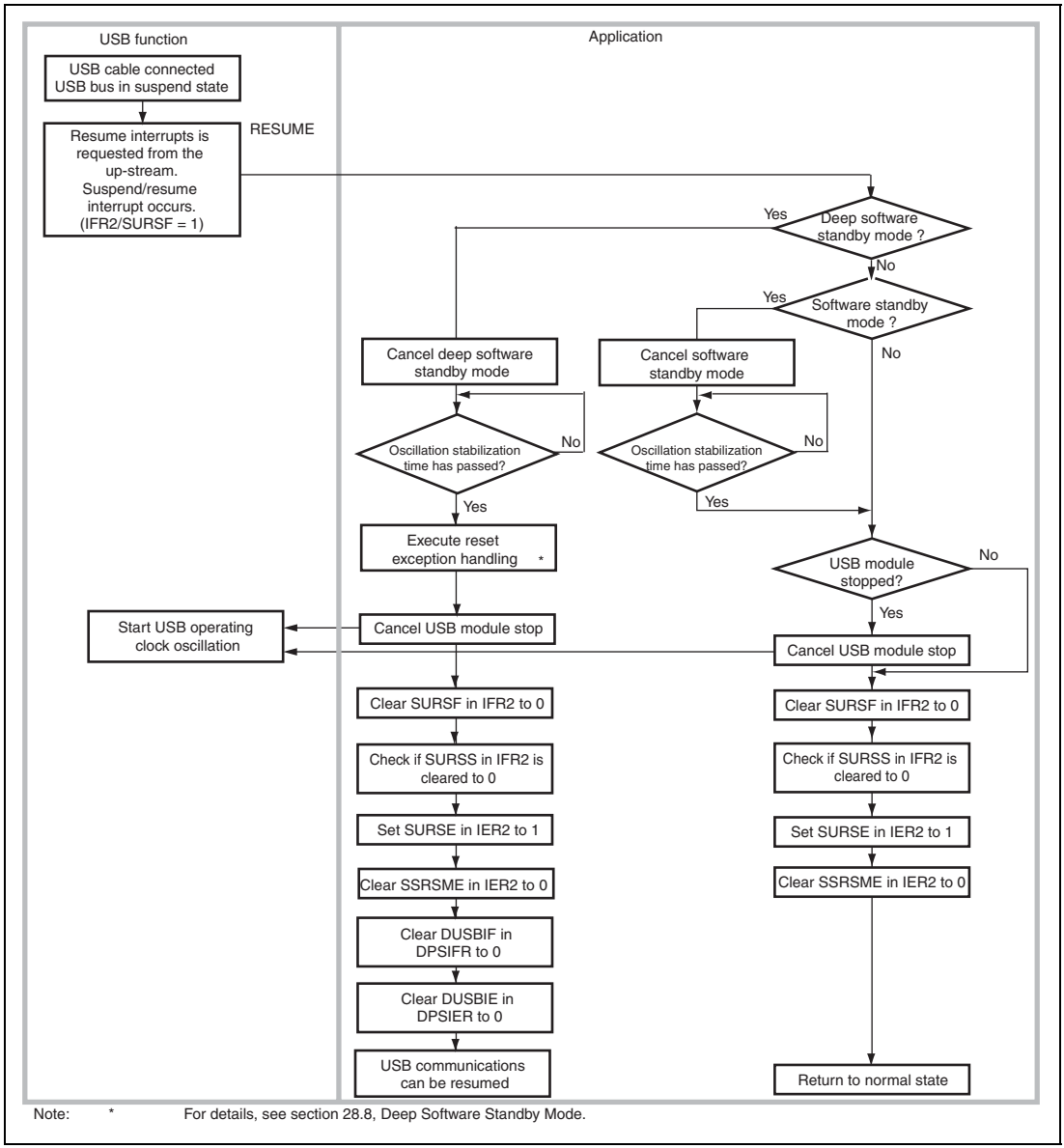
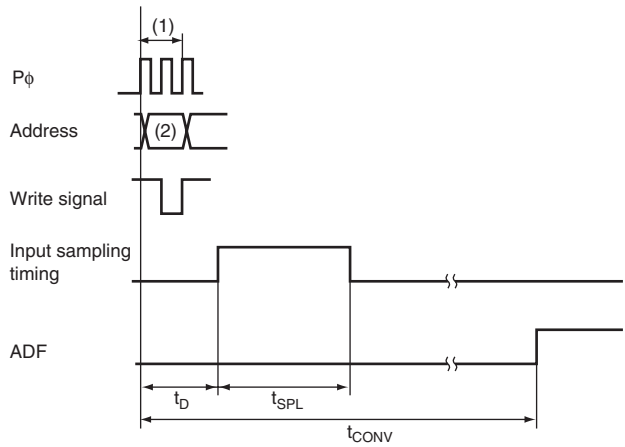


Figure 20.5 Resume Operation from Up-Stream



[Legend]
(1): ADCSR write cycle
(2): ADCSR address
$t_{D:}$ A/D conversion start delay time
t_{SPL}: Input sampling time
t_{CONV}: A/D conversion time

Figure 22.6 Periods of A/D Conversion

Table 22.3 Characteristics of A/D Conversion (Unit 0: when EXCKS* = 0, ICKSEL = 0, and ADSSTR* = H'0F) (1)

Item	Symbol	CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	3	—	14	3	—	10	3	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	517	—	528	261	—	268	133	—	138	69	—	73

Notes: Values in the table are numbers of states.

* The full-spec emulator (E6000H) should not be used, but the on-chip emulator (E10A-USB) is usable.

22.6 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes.
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 22.9).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value B'0000000000 (H'000) to B'0000000001 (H'001) (see figure 22.10).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from B'1111111110 (H'3FE) to B'1111111111 (H'3FF) (see figure 22.10).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristic between the zero voltage and the full-scale voltage. Does not include the offset error, full-scale error, or quantization error (see figure 22.10).
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes the offset error, full-scale error, quantization error, and nonlinearity error.

25.6 Input/Output Pins

The flash memory is controlled through the input/output pins shown in table 25.2.

Table 25.2 Pin Configuration

Abbreviation	I/O	Function
$\overline{\text{RES}}$	Input	Reset
EMLE	Input	On-chip emulator enable pin (EMLE = 0 for flash memory programming/erasure)
MD3 to MD0	Input	Set operating mode of this LSI
PM2	Input	SCI boot mode/USB boot mode setting (for boot mode setting by MD3 to MD0)
TxD4	Output	Serial transmit data output (used in SCI boot mode)
RxD4	Input	Serial receive data input (used in SCI boot mode)
USD+, USD−	I/O	USB data I/O (used in USB boot mode)
VBUS	Input	USB cable connection/disconnection detect (used in USB boot mode)
PM3	Input	USB bus power mode/self power mode setting (used in USB boot mode)
PM4	Output	D+ pull-up control (used in USB boot mode)

(a) User Boot MAT Programming Selection

The boot program will transfer a programming program. The data is programmed to the user boot MATs by the transferred programming program.

Command	H'42

- Command, H'42, (one byte): User boot MAT programming selection

Response	H'06

- Response, H'06, (one byte): Response to user boot MAT programming selection
  When the programming program has been transferred, the boot program will return ACK.

Error Response	H'C2	ERROR

- Error response : H'C2 (1 byte): Error response to user boot MAT programming selection
- ERROR : (1 byte): Error code
  H'54: Selection processing error (transfer error occurs and processing is not completed)

(b) User MAT Programming Selection

The boot program will transfer a program for user MAT programming selection. The data is programmed to the user MATs by the transferred program for programming.

Command	H'43

- Command, H'43, (one byte): User MAT programming selection

Response	H'06

- Response, H'06, (one byte): Response to user MAT programming selection
  When the programming program has been transferred, the boot program will return ACK.

Error Response	H'C3	ERROR

- Error response : H'C3 (1 byte): Error response to user MAT programming selection
- ERROR : (1 byte): Error code
  H'54: Selection processing error (transfer error occurs and processing is not completed)

Pin No				
LQFP-144	LGA-145	Pin Name	Input/Output	Bit Name
81	K12	PI5	Input	104
			Output enable	103
			Output	102
83	J10	PI7	Input	101
			Output enable	100
			Output	99
82	J13	PI6	Input	98
			Output enable	97
			Output	96
84	J11	P10	Input	95
			Output enable	94
			Output	93
85	H11	P11	Input	92
			Output enable	91
			Output	90
86	J12	P12	Input	89
			Output enable	88
			Output	87
87	G11	P13	Input	86
			Output enable	85
			Output	84
93	G10	P14	Input	77
			Output enable	76
			Output	75
94	F11	P15	Input	74
			Output enable	73
			Output	72
100	E11	P16	Input	71
			Output enable	70
			Output	69
101	E10	P17	Input	68
			Output enable	67
			Output	66
105	C12	P36	Input	65
			Output enable	64
			Output	63
104	D11	P35	Input	62
			Output enable	61
			Output	60
107	B13	P60	Input	59
			Output enable	58
			Output	57
106	C13	P37	Input	56
			Output enable	55
			Output	54
108	A13	P61	Input	53
			Output enable	52
			Output	51
115	D10	MD0	Input	50
116	C10	PC2	Input	49
			Output enable	48
			Output	47
117	B10	PC3	Input	46
			Output enable	45
			Output	44
129	B6	MD1	Input	43
130	C7	PB4	Input	42
			Output enable	41
			Output	40

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ISR1	—	—	—	—	—	EP3 TR	EP3 TS	VBUSF	USB
ISR2	—	—	—	SURSE	CFDN	—	SETCE	SETIE	
EPDR0i	D7	D6	D5	D4	D3	D2	D1	D0	
EPDR0o	D7	D6	D5	D4	D3	D2	D1	D0	
EPDR0s	D7	D6	D5	D4	D3	D2	D1	D0	
EPDR1	D7	D6	D5	D4	D3	D2	D1	D0	
EPDR2	D7	D6	D5	D4	D3	D2	D1	D0	
EPDR3	D7	D6	D5	D4	D3	D2	D1	D0	
EPSZ0o	—	—	—	—	—	—	—	—	
EPSZ1	—	—	—	—	—	—	—	—	
DASTS	—	—	EP3 DE	EP2 DE	—	—	—	EP0i DE	
FCLR	—	EP3 CLR	EP1 CLR	EP2 CLR	—	—	EP0o CLR	EP0i CLR	
EPSTL	—	—	—	—	EP3STL	EP2STL	EP1STL	EP0STL	
TRG	—	EP3 PKTE	EP1 RDFN	EP2 PKTE	—	EP0s RDFN	EP0o RDFN	EP0i PKTE	
DMA	—	—	—	—	—	PULLUP_E	EP2DMAE	EP1DMAE	
CVR	CNFV1	CNFV0	INTV1	INTV0	—	ALTV2	ALTV1	ALTV0	
CTLR	—	—	—	RWUPS	RSME	RWMD	ASCE	—	
EPIR	D7	D6	D5	D4	D3	D2	D1	D0	
TRNTREG0	PTSTE	—	—	—	SUSPEND	txenl	txse0	txdata	
TRNTREG1	—	—	—	—	—	xver_data	dpls	dmns	
PMDDR	—	—	—	PM4DDR	PM3DDR	PM2DDR	PM1DDR	PM0DDR	I/O port
PMDR	—	—	—	PM4DR	PM3DR	PM2DR	PM1DR	PM0DR	
PORTM	—	—	—	PM4	PM3	PM2	PM1	PM0	
PMICR	—	—	—	PM4ICR	PM3ICR	PM2ICR	PM1ICR	PM0ICR	
SMR_5*[1]	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_5
	(GM)	(BLK)	(PE)	(O/$\overline{E}$)	(BCP1)	(BCP0)			
BRR_5									
SCR_5*[1]	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_5									