Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SmartCard, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	92
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61665n50fpv

Pin No.		Pin Name		
LQFP-144	LGA-145	Modes 1, 2, and 6	Modes 3 and 7	Modes 4 and 5
124	B7	P54/AN4/$\overline{\text{IRQ4}}$-B	P54/AN4/$\overline{\text{IRQ4}}$-B	P54/AN4/$\overline{\text{IRQ4}}$-B
125	A8	Vref	Vref	Vref
126	D8	P55/AN5/$\overline{\text{IRQ5}}$-B	P55/AN5/$\overline{\text{IRQ5}}$-B	P55/AN5/$\overline{\text{IRQ5}}$-B
127	D7	P56/AN6/DA0/$\overline{\text{IRQ6}}$-B	P56/AN6/DA0/$\overline{\text{IRQ6}}$-B	P56/AN6/DA0/$\overline{\text{IRQ6}}$-B
128	A7	P57/AN7/DA1/$\overline{\text{IRQ7}}$-B	P57/AN7/DA1/$\overline{\text{IRQ7}}$-B	P57/AN7/DA1/$\overline{\text{IRQ7}}$-B
129	B6	MD1	MD1	MD1
130	C7	PB4/$\overline{\text{CS4}}$-B/$\overline{\text{WE}}$	PB4/$\overline{\text{CS4}}$-B/$\overline{\text{WE}}$	PB4/$\overline{\text{CS4}}$-B/$\overline{\text{WE}}$
131	C6	PB5/$\overline{\text{CS5}}$-D/$\overline{\text{OE}}$/CKE	PB5/$\overline{\text{CS5}}$-D/$\overline{\text{OE}}$/CKE	PB5/$\overline{\text{CS5}}$-D/$\overline{\text{OE}}$/CKE
132	A6	PB6/$\overline{\text{CS6}}$-D/(RD/$\overline{\text{WR}}$-B)/$\overline{\text{ADTRG0}}$-B	PB6/$\overline{\text{CS6}}$-D/(RD/$\overline{\text{WR}}$-B)/$\overline{\text{ADTRG0}}$-B	PB6/$\overline{\text{CS6}}$-D/(RD/$\overline{\text{WR}}$-B)/$\overline{\text{ADTRG0}}$-B
133	B5	MD3	MD3	MD3
134	D6	PA0/$\overline{\text{BREQO}}$/$\overline{\text{BS}}$-A	PA0/$\overline{\text{BREQO}}$/$\overline{\text{BS}}$-A	PA0/$\overline{\text{BREQO}}$/$\overline{\text{BS}}$-A
135	A5	PA1/$\overline{\text{BACK}}$/(RD/$\overline{\text{WR}}$-A)	PA1/$\overline{\text{BACK}}$/(RD/$\overline{\text{WR}}$-A)	PA1/$\overline{\text{BACK}}$/(RD/$\overline{\text{WR}}$-A)
136	B4	PA2/$\overline{\text{BREQ}}$/$\overline{\text{WAIT}}$	PA2/$\overline{\text{BREQ}}$/$\overline{\text{WAIT}}$	PA2/$\overline{\text{BREQ}}$/$\overline{\text{WAIT}}$
137	D5	PA3/$\overline{\text{LLWR}}$/$\overline{\text{LLB}}$	PA3/$\overline{\text{LLWR}}$/$\overline{\text{LLB}}$	$\overline{\text{LLWR}}$/$\overline{\text{LLB}}$
138	A4	PA4/$\overline{\text{LHWR}}$/$\overline{\text{LUB}}$	PA4/$\overline{\text{LHWR}}$/$\overline{\text{LUB}}$	PA4/$\overline{\text{LHWR}}$/$\overline{\text{LUB}}$
139	C5	PA5/$\overline{\text{RD}}$	PA5/$\overline{\text{RD}}$	$\overline{\text{RD}}$
140	C4	PA6/$\overline{\text{AS}}$/$\overline{\text{AH}}$/$\overline{\text{BS}}$-B	PA6/$\overline{\text{AS}}$/$\overline{\text{AH}}$/$\overline{\text{BS}}$-B	PA6/$\overline{\text{AS}}$/$\overline{\text{AH}}$/$\overline{\text{BS}}$-B
141	C3	Vss	Vss	Vss
142	A2	PA7/Bφ	PA7/Bφ	PA7/Bφ
143	A3	Vcc	Vcc	Vcc
144	B2	PB0/$\overline{\text{CS0}}$/$\overline{\text{CS4}}$-A/$\overline{\text{CS5}}$-B	PB0/$\overline{\text{CS0}}$/$\overline{\text{CS4}}$-A/$\overline{\text{CS5}}$-B	PB0/$\overline{\text{CS0}}$/$\overline{\text{CS4}}$-A/$\overline{\text{CS5}}$-B
—	E5	NC	NC	NC

Notes: 1. These pins can be used when the PCJKE bit in PFCRD is set to 1 in single-chip mode.
2. Pins TDO, $\overline{\text{TRST}}$, TMS, and TCK are enabled in mode 3.

(2) Priority Determination

The DTC activation source is selected according to the default priority, and the selection is not affected by its mask level or priority level. For respective priority levels, see table 12.1, Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs.

(3) Operation Order

If the same interrupt is selected as both the DTC activation source and CPU interrupt source, the CPU interrupt exception handling is performed after the DTC data transfer. If the same interrupt is selected as the DTC, DMAC or EXDMAC activation source or CPU interrupt source, respective operations are performed independently.

Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERF of the DTC, and the DISEL bit in MRB of the DTC.

Table 7.6 Interrupt Source Selection and Clear Control

Setting					
DMAC	DTC		Interrupt Source Selection/Clear Control		
DTA	DTCE	DISEL	DMAC	DTC	CPU
0	0	*	O	X	√
	1	0	O	√	X
		1	O	O	√
1	*	*	√	X	X

[Legend]

√: The corresponding interrupt is used. The interrupt source is cleared.
(The interrupt source flag must be cleared in the CPU interrupt handling routine.)

O: The corresponding interrupt is used. The interrupt source is not cleared.

X: The corresponding interrupt is not available.

*: Don't care.

(4) Usage Note

The interrupt sources of the SCI, and A/D converter are cleared according to the setting shown in table 7.6, when the DTC or DMAC reads/writes the prescribed register.

To initiate multiple channels for the DTC and DMAC with the same interrupt, the same priority (DTCP = DMAP) should be assigned.

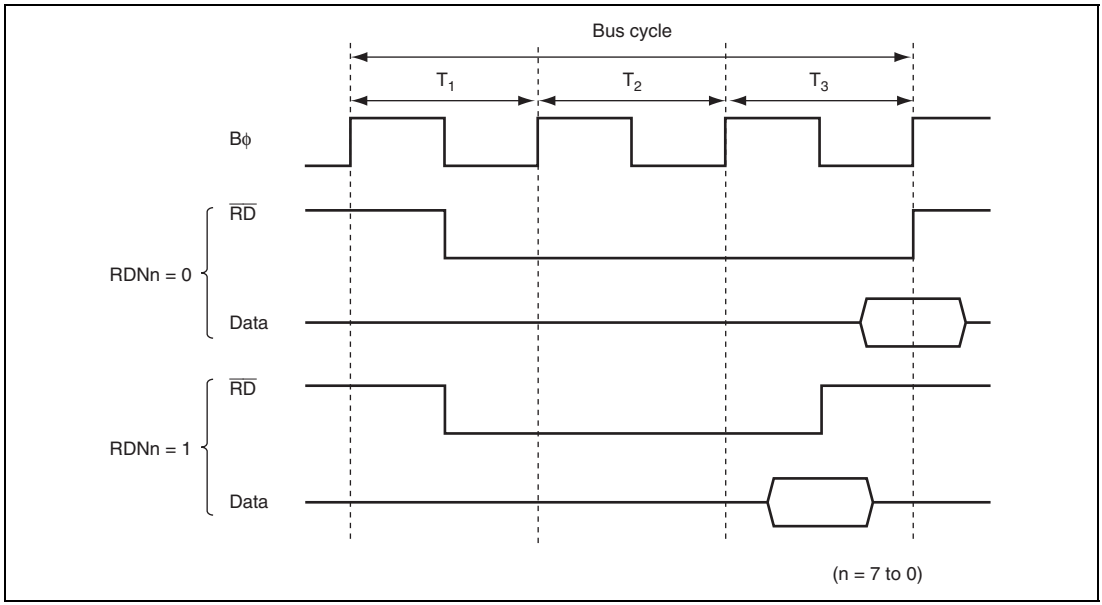

Figure 9.2 Read Strobe Negation Timing (Example of 3-State Access Space)

9.2.5 $\overline{CS}$ Assertion Period Control Registers (CSACR)

CSACR selects whether or not the assertion periods of the chip select signals ($\overline{CSn}$) and address signals for the basic bus, byte-control SRAM, burst ROM, and address/data multiplexed I/O interface are to be extended. Extending the assertion period of the $\overline{CSn}$ and address signals allows the setup time and hold time of read strobe ($\overline{RD}$) and write strobe ($\overline{LHWR}/\overline{LLWR}$) to be assured and to make the write data setup time and hold time for the write strobe become flexible.

Bit	15	14	13	12	11	10	9	8
Bit Name	CSXH7	CSXH6	CSXH5	CSXH4	CSXH3	CSXH2	CSXH1	CSXH0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	CSXT7	CSXT6	CSXT5	CSXT4	CSXT3	CSXT2	CSXT1	CSXT0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.6.4 Wait Control

This LSI can extend the bus cycle by inserting wait cycles (Tw) when the external address space is accessed. There are two ways of inserting wait cycles: program wait (Tpw) insertion and pin wait (Ttw) insertion using the $\overline{\text{WAIT}}$ pin.

(1) Program Wait Insertion

From 0 to 7 wait cycles can be inserted automatically between the T_2 state and T_3 state for 3-state access space, according to the settings in WTCRA and WTCRB.

(2) Pin Wait Insertion

For 3-state access space, when the WAITE bit in BCR1 is set to 1 and the corresponding ICR bit is set to 1, wait input by means of the $\overline{\text{WAIT}}$ pin is enabled. When the external address space is accessed in this state, a program wait (Tpw) is first inserted according to the WTCRA and WTCRB settings. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of Bϕ in the last T2 or Tpw cycle, another Ttw cycle is inserted until the $\overline{\text{WAIT}}$ pin is brought high. The pin wait insertion is effective when the Tw cycles are inserted to seven cycles or more, or when the number of Tw cycles to be inserted is changed according to the external devices. The WAITE bit is common to all areas. For details on ICR, see section 13, I/O Ports.

11.3.2 EXDMA Destination Address Register (EDDAR)

EDDAR is a 32-bit readable/writable register that specifies the transfer destination address. An address update function is provided that updates the register contents to the next transfer destination address each time transfer processing is performed. In single address mode, the EDDAR value is ignored when the address specified by EDSAR is transferred as a source address (DIRS = 0 in EDACR).

EDDAR can be read at all times by the CPU. When reading EDDAR for a channel on which EXDMA transfer processing is in progress, a longword-size read must be executed. Do not write to EDDAR for a channel on which EXDMA transfer is in progress.

Bit	31	30	29	28	27	26	25	24
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

When transfer starts, the offset value is added to the transfer source address and the data is transferred. The data is aligned in the order of transfer in the transfer destination. After up to data 4 is transferred, the EXDMAC assumes that a repeat-size transfer completed, and restores the transfer source address to the transfer start address (address of transfer source data 1). At the same time, a repeat size end interrupt is requested. This interrupt request aborts the transfer temporarily. Overwrite the EDSAR value to the data 5 address by accessing the I/O register via the CPU. (For longword transfer, add 4 to the address of data 1.) When the DTE bit in EDMDR is set to 1, transfer is resumed from the state in which the transfer is aborted. The transfer source data is XY-converted and transferred to the transfer destination by repeating the above processing.

Figure 11.20 shows the XY conversion flow.

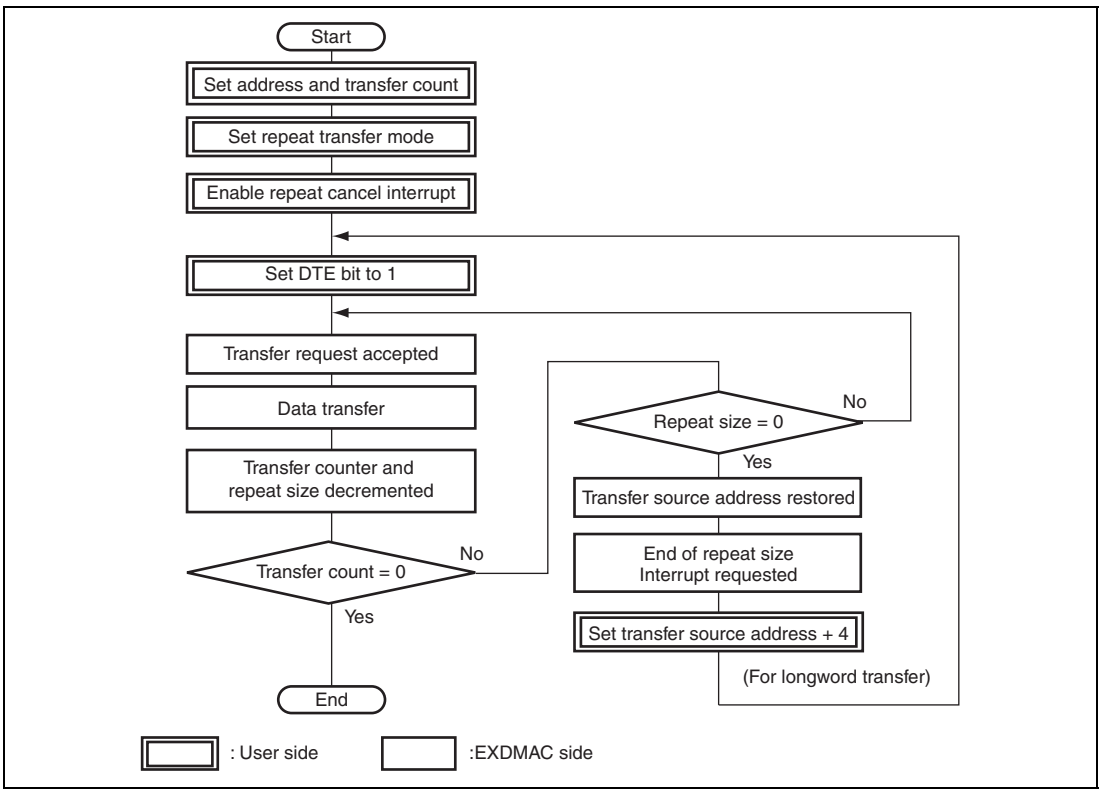

Figure 11.20 Flow of XY Conversion Combining Repeat Transfer Mode and Offset Addition

Table 13.5 Available Output Signals and Settings in Each Port

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
P1	7	$\overline{\text{EDRAK1}}$_OE	$\overline{\text{EDRAK1}}$	PFCR8.EDMAS1[A,B] = 00	SYSCR.EXPE = 1, EDMDR_1.EDRAKE = 1
		SCL0_OE	SCL0		ICCRA.ICE = 1
	6	$\overline{\text{EDACK1A}}$_OE	$\overline{\text{EDACK1}}$	PFCR8.EDMAS1[A,B] = 00	SYSCR.EXPE = 1, EDACR_1.AMS = 1, EDMDR_1.EDACKE = 1
		$\overline{\text{DACK1A}}$_OE	$\overline{\text{DACK1}}$	PFCR7.DMAS1[A,B] = 00	DMAC.DACR_1.AMS = 1, DMDR_1.DACKE = 1
		SDA0_OE	SDA0		ICCRA.ICE = 1
	5	$\overline{\text{ETEND1A}}$_OE	$\overline{\text{ETEND1}}$	PFCR8.EDMAS1[A,B] = 00	SYSCR.EXPE = 1, EDMDR_1.ETENDE = 1
		$\overline{\text{TEND1A}}$_OE	$\overline{\text{TEND1}}$	PFCR7.DMAS1[A,B] = 00	DMDR_1.TENDE = 1
		SCL1_OE	SCL1		ICCRA.ICE = 1
	4	TxD5_OE	TxD5		SCR.TE = 1, IrCR.IrE = 0
		IrTxD_OE	IrTxD		SCR.TE = 1, IrCR.IrE = 1
		SDA1_OE	SDA1		ICCRA.ICE = 1
	3	$\overline{\text{EDRAK0}}$_OE	$\overline{\text{EDRAK0}}$	PFCR8.EDMAS0[A,B] = 00	SYSCR.EXPE = 1, EDMDR_0.EDRAKE = 1
	2	$\overline{\text{EDACK0A}}$_OE	$\overline{\text{EDACK0}}$	PFCR8.EDMAS0[A,B] = 00	SYSCR.EXPE = 1, EDACR_0.AMS = 1, EDMDR_0.EDACKE = 1
		$\overline{\text{DACK0A}}$_OE	$\overline{\text{DACK0}}$	PFCR7.DMAS0[A,B] = 00	DMAC.DACR_0.AMS = 1, DMDR_0.DACKE = 1
		SCK2_OE	SCK2		When SCMR.SMIF = 1: SCR.TE = 1 or SCR.RE = 1 while SMR.GM = 0, SCR.CKE [1, 0] = 01 or while SMR.GM = 1 When SCMR.SMIF = 0: SCR.TE = 1 or SCR.RE = 1 while SMR.C/A = 0, SCR.CKE [1, 0] = 01 or while SMR.C/A = 1, SCR.CKE 1 = 0
	1	$\overline{\text{ETEND0A}}$_OE	$\overline{\text{ETEND0}}$	PFCR8.EDMAS0[A,B] = 00	SYSCR.EXPE = 1, EDMDR_0.ETENDE = 1
		$\overline{\text{TEND0A}}$_OE	$\overline{\text{TEND0}}$	PFCR7.DMAS0[A,B] = 00	DMDR_0.TENDE = 1
	0	TxD2_OE	TxD2		SCR.TE = 1

14.3.2 Timer Mode Register (TMDR)

TMDR sets the operating mode for each channel. The TPU has six TMDR registers, one for each channel. TMDR register settings should be made only while TCNT operation is stopped.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial Value	1	1	0	0	0	0	0	0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
5	BFB	0	R/W	Buffer Operation B Specifies whether TGRB is to normally operate, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare is not generated. In channels 1, 2, 4, and 5, which have no TGRD, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: TGRB operates normally 1: TGRB and TGRD used together for buffer operation
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRA is to normally operate, or TGRA and TGRC are to be used together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare is not generated. In channels 1, 2, 4, and 5, which have no TGRC, bit 4 is reserved. It is always read as 0 and cannot be modified. 0: TGRA operates normally 1: TGRA and TGRC used together for buffer operation
3	MD3	0	R/W	Modes 3 to 0 Set the timer operating mode. MD3 is a reserved bit. The write value should always be 0. See table 14.13 for details.
2	MD2	0	R/W	
1	MD1	0	R/W	
0	MD0	0	R/W	

- Sample Setup Procedure for PPG1

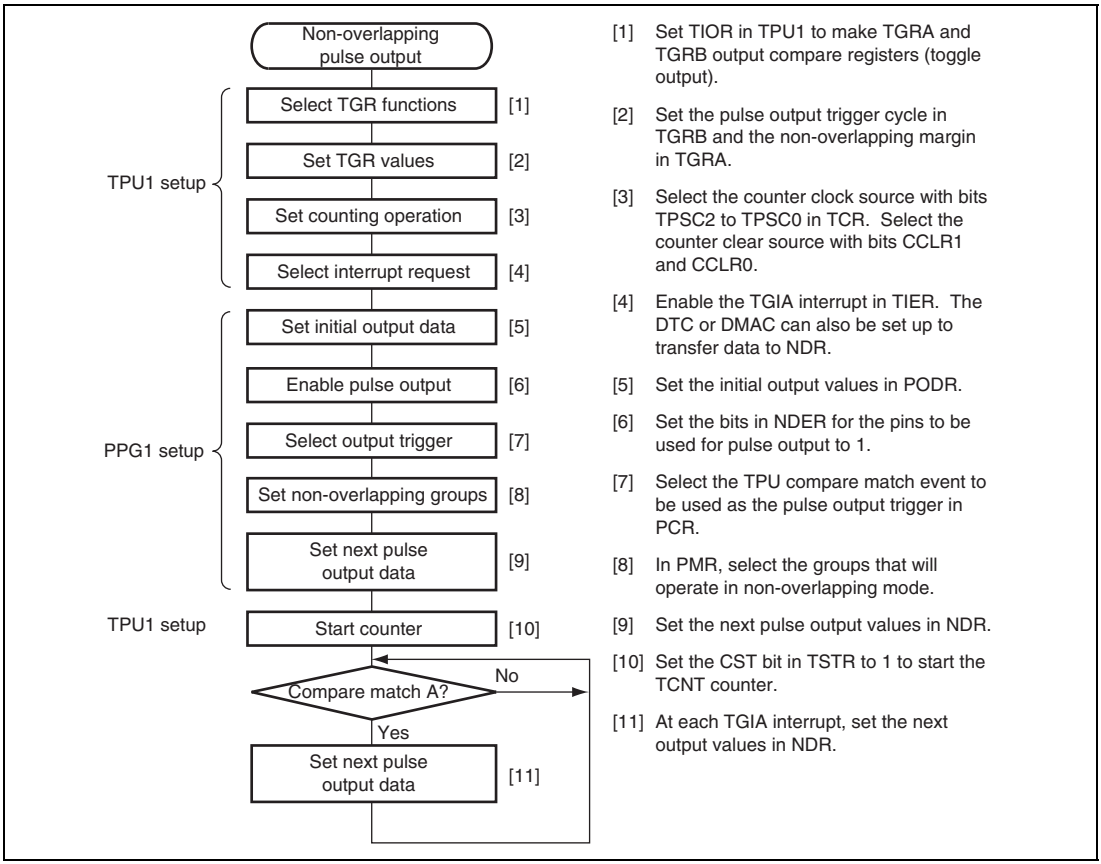

Figure 15.11 Setup Procedure for Non-Overlapping Pulse Output (PPG1)

	Operating Frequency Pϕ (MHz)											
	25			30			33			35		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	110	–0.02	3	132	0.13	3	145	0.33	3	154	0.23
150	3	80	0.47	3	97	–0.35	3	106	0.39	3	113	–0.06
300	2	162	–0.15	2	194	0.16	2	214	–0.07	2	227	–0.06
600	2	80	0.47	2	97	–0.35	2	106	0.39	2	113	–0.06
1200	1	162	–0.15	1	194	0.16	1	214	–0.07	1	227	–0.06
2400	1	80	0.47	1	97	–0.35	1	106	0.39	1	113	–0.06
4800	0	162	–0.15	0	194	0.16	0	214	–0.07	0	227	–0.06
9600	0	80	0.47	0	97	–0.35	0	106	0.39	0	113	–0.06
19200	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	56	–0.06
31250	0	24	0.00	0	29	0	0	32	0	0	34	0.00
38400	0	19	1.73	0	23	1.73	0	26	–0.54	0	27	1.73

Note: In SCI_2, 5, and 6, this is an example when the ABCS bit in SEMR_2, 5, and 6 is 0. When the ABCS bit is set to 1, the bit rate is two times.

Table 19.5 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode)

Pϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	Pϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
8	250000	0	0	17.2032	537600	0	0
9.8304	307200	0	0	18	562500	0	0
10	312500	0	0	19.6608	614400	0	0
12	375000	0	0	20	625000	0	0
12.288	384000	0	0	25	781250	0	0
14	437500	0	0	30	937500	0	0
14.7456	460800	0	0	33	1031250	0	0
16	500000	0	0	35	1093750	0	0

20.3.19 Data Status Register (DASTS)

DASTS indicates whether the transmit FIFO buffers contain valid data. A bit is set when data is written to the corresponding FIFO buffer and the packet enable state is set, and cleared when all data has been transmitted to the host.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	EP3 DE	EP2 DE	—	—	—	EP0i DE
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved
6	—	0	R	These bits are always read as 0. The write value should always be 0.
5	EP3 DE	0	R	EP3 Data Present This bit is set when the endpoint 3 FIFO buffer contains valid data.
4	EP2 DE	0	R	EP2 Data Present This bit is set when the endpoint 2 FIFO buffer contains valid data.
3	—	0	R	Reserved
2	—	0	R	These bits are always read as 0.
1	—	0	R	
0	EP0i DE	0	R	EP0i Data Present This bit is set when the endpoint 0 FIFO buffer contains valid data.

21.6 Bit Synchronous Circuit

This module has a possibility that the high-level period is shortened in the two states described below.

In master mode,

- When SCL is driven low by the slave device
- When the rising speed of SCL is lowered by the load on the SCL line (load capacitance or pull-up resistance)

Therefore, this module monitors SCL and communicates bit by bit in synchronization.

Figure 21.18 shows the timing of the bit synchronous circuit, and table 21.4 shows the time when SCL output changes from low to Hi-Z and the period which SCL is monitored.

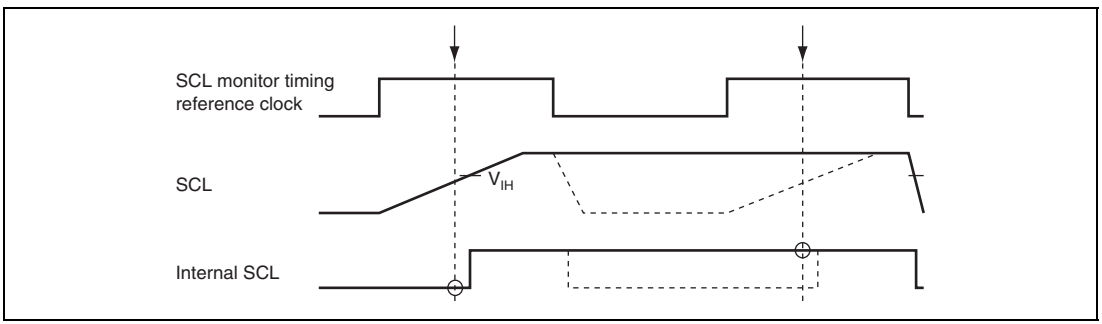

Figure 21.18 Timing of the Bit Synchronous Circuit

Table 21.4 Time for Monitoring SCL

CKS3	CKS2	Time for Monitoring SCL
0	0	7.5 tcyc
	1	19.5 tcyc
1	0	17.5 tcyc
	1	41.5 tcyc

22.5 Interrupt Source

The A/D converter generates an A/D conversion end interrupt (ADI) at the end of A/D conversion. Setting the ADIE bit to 1 when the ADF bit in ADCSR is set to 1 after A/D conversion is completed enables ADI interrupt requests. The data transfer controller (DTC)* and DMA controller (DMAC) can be activated by an ADI interrupt. Having the converted data read by the DTC* or DMAC in response to an ADI interrupt enables continuous conversion to be achieved without imposing a load on software.

Note: * Only possible in unit 0.

Table 22.7 A/D Converter Interrupt Source

Name	Interrupt Source	Interrupt Flag	DTC Activation	DMAC Activation
ADI	A/D conversion end	ADF	Possible*	Possible

Note: * Only possible in unit 0.

25.4.2 Block Diagram of H8SX/1665

Figure 25.4 (2) shows the block structure of the 512-Kbyte user MAT. The heavy-line frames indicate the erase blocks. The thin-line frames indicate the programming units and the values inside the frames stand for the addresses. The user MAT is divided into seven 64-Kbyte blocks, one 32-Kbyte block, and eight 4-Kbyte blocks. The user MAT can be erased in these divided block units. Programming is done in 128-byte units starting from where the lower address is H'00 or H'80. RAM emulation can be performed in the eight 4-Kbyte blocks.

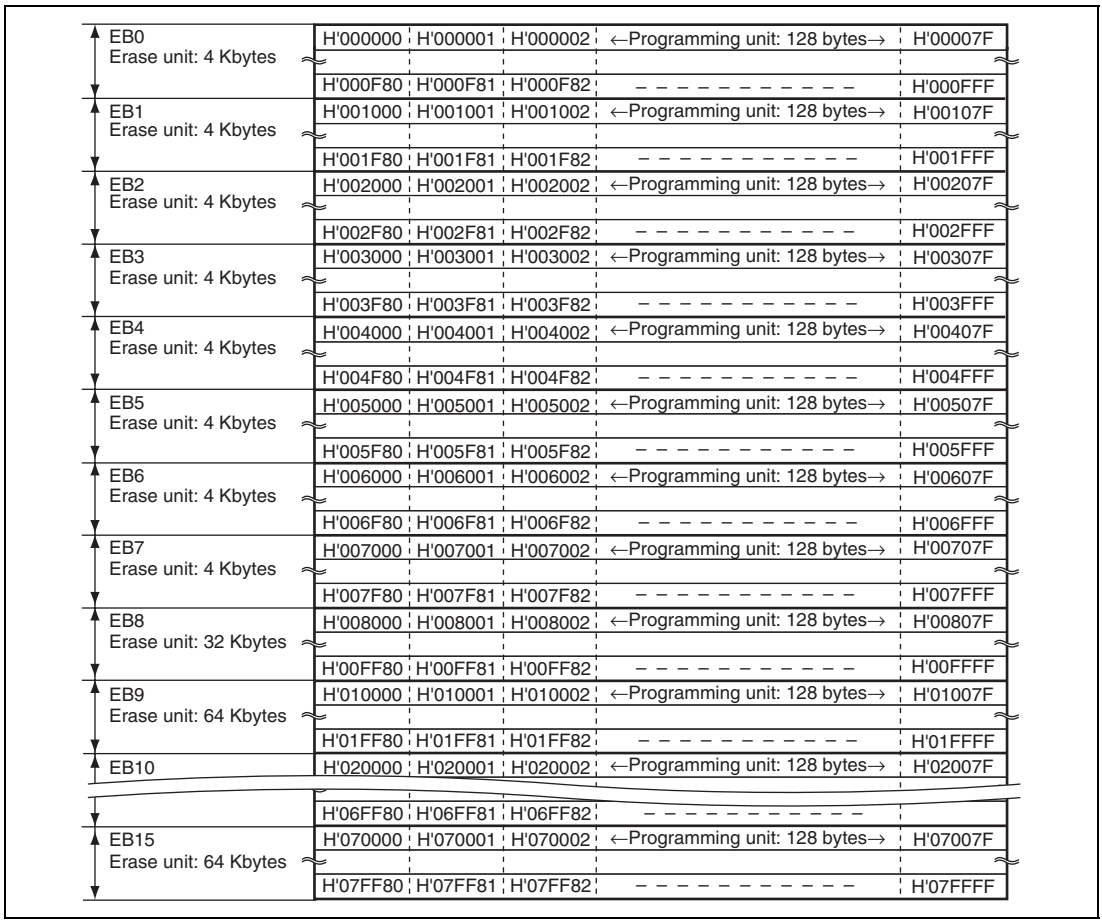

Figure 25.4 (2) User MAT Block Structure of H8SX/1665

(2) Flash Program Code Select Register (FPCS)

FPCS selects the programming program to be downloaded.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	—	—	—	—	PPVS
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These are read-only bits and cannot be modified.
0	PPVS	0	R/W	Program Pulse Verify Selects the programming program to be downloaded. 0: Programming program is not selected. [Clearing condition] When transfer is completed 1: Programming program is selected.

(3) Flash Erase Code Select Register (FECS)

FECS selects the erasing program to be downloaded.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	—	—	—	—	EPVB
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These are read-only bits and cannot be modified.
0	EPVB	0	R/W	Erase Pulse Verify Block Selects the erasing program to be downloaded. 0: Erasing program is not selected. [Clearing condition] When transfer is completed 1: Erasing program is selected.

(2) State Transition Diagram

The state transition after USB boot mode is initiated is shown in figure 25.10.

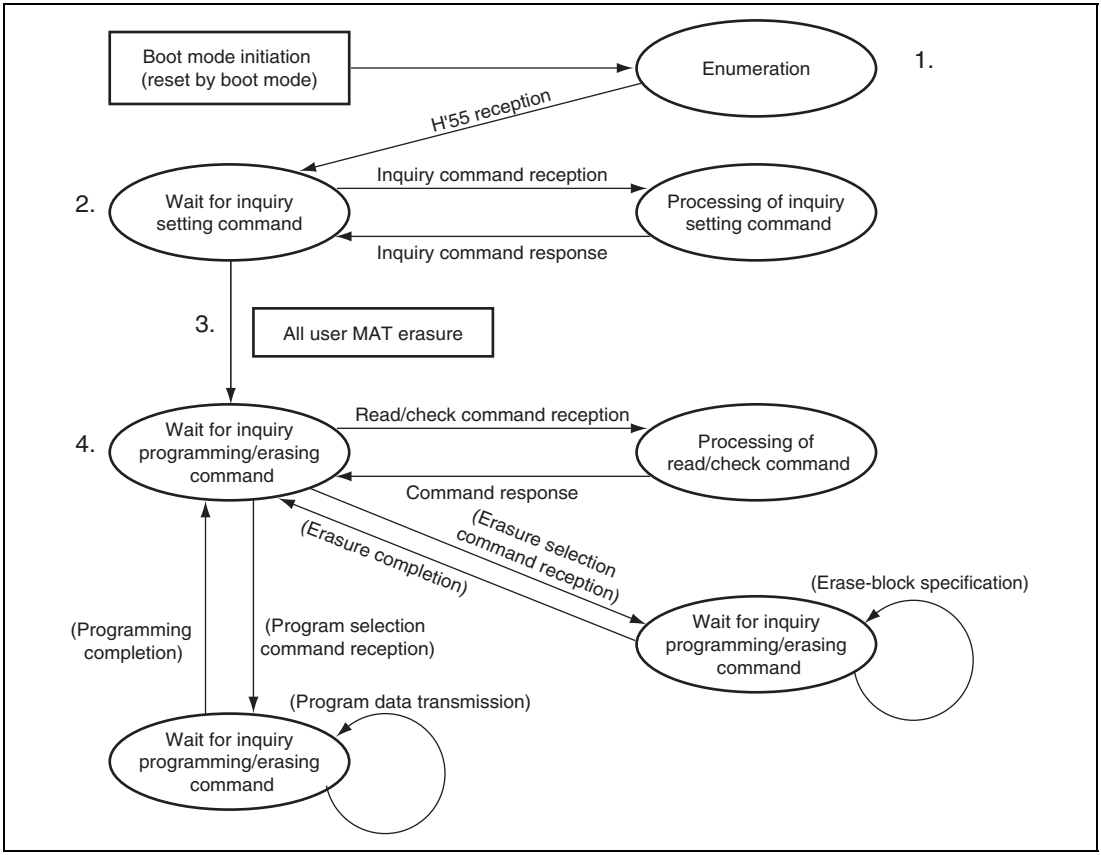

Figure 25.10 USB Boot Mode State Transition Diagram

1. After a transition to the USB boot mode is made, the boot program embedded in this LSI is initialized. This LSI performs enumeration to the host after the USB boot program is initialized.
2. Inquiry information about the size, configuration, start address, and support status of the user MAT is transmitted to the host.
3. After inquiries have finished, all user MAT are automatically erased.

(1) Bit-Rate-Adjustment State

The bit rate is calculated by measuring the period of transfer of a low-level byte (H'00) from the host. The bit rate can be changed by the command for a new bit rate selection. After the bit rate has been adjusted, the boot program enters the inquiry and selection state. The bit-rate-adjustment sequence is shown in figure 25.24.

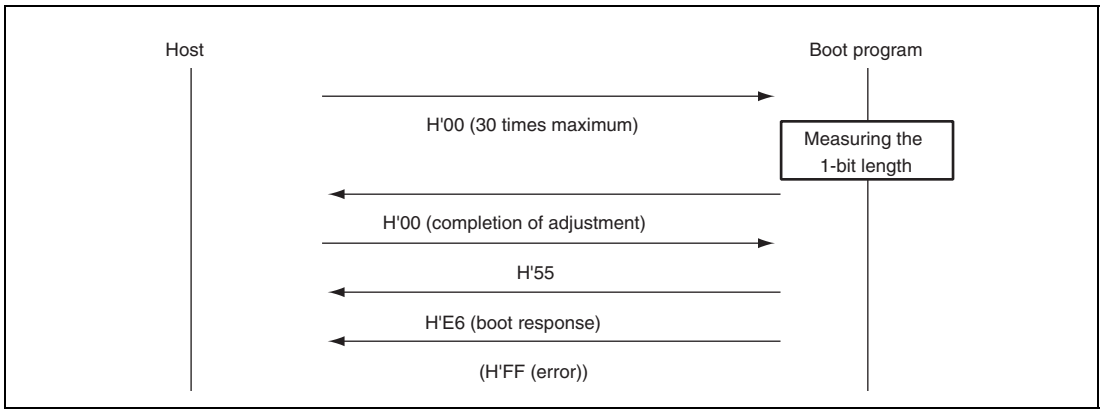

Figure 25.24 Bit-Rate-Adjustment Sequence

(2) Communications Protocol

After adjustment of the bit rate, the protocol for serial communications between the host and the boot program is as shown below.

1. One-byte commands and one-byte responses

   These one-byte commands and one-byte responses consist of the inquiries and the ACK for successful completion.
2. n-byte commands or n-byte responses

   These commands and responses are comprised of n bytes of data. These are selections and responses to inquiries.

   The program data size is not included under this heading because it is determined in another command.
3. Error response

   The error response is a response to inquiries. It consists of an error response and an error code and comes two bytes.
4. Programming of 128 bytes

   The size is not specified in commands. The size of n is indicated in response to the programming unit inquiry.

28.10 Sleep Instruction Exception Handling

A sleep instruction exception handling is generated by executing a SLEEP instruction. The sleep instruction exception handling is always accepted in the program execution state.

When the SLPIE bit is set to 0, sleep-instruction exception handling does not follow execution of the SLEEP instruction. In this case, the CPU is placed in the power-down state. After exit from the power-down state has been initiated by an exception, the CPU starts handling of the exception. When the SLPIE bit is set to 1, sleep-instruction exception handling follows execution of the SLEEP instruction. The CPU immediately starts sleep-instruction exception handling, which blocks the transition to the power-down state is prevented by.

When a SLEEP instruction is executed while the SLPIE bit is cleared to 0, a transition is made to the power-down state. Exit from the power-down state is initiated by an exit-initiating interrupt source (see figure 28.10).

When an interrupt that causes exit from the power-down state is generated immediately before the execution of a SLEEP instruction, exception handling for the interrupt starts. On return from the exception service routine, the SLEEP instruction is executed to enter the power-down state. In this case, exit from the power-down state will not take place until the next time an exit-initiating interrupt is generated (see figure 28.11).

As stated above, setting the SLPIE bit to 1 causes sleep-instruction exception handling to follow the execution of the SLEEP instruction. If this setting is made in the exception service routine for an interrupt that initiates exit from the power-down state, handling of the sleep-instruction exception due to the execution of a SLEEP instruction will proceed even if the interrupt was generated immediately beforehand (see figure 28.12). Consequently, the CPU will execute the instruction that follows the SLEEP instruction, after handling of the sleep-instruction exception and exception service routine, and will not enter the power-down state.

Thus, when the SLPIE bit is set to 1 to enable the sleep exception handling, clear the SSBY bit in SBYCR to 0.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ADCSR_0	ADF	ADIE	ADST	—	CH3	CH2	CH1	CH0	A/D_0
ADCR_0	TRGS1	TRGS0	SCANE	SCANS	CKS1	CKS0	—	EXTRGS	
ADMOSEL_0	—	—	—	—	—	—	ICKSEL	—	
TCSR	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT
TCNT									
RSTCSR	WOVF	RSTE	—	—	—	—	—	—	
TCR_0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_0
TCR_1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_1
TCSR_0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0	TMR_0
TCSR_1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	TMR_1
TCORA_0									TMR_0
TCORA_1									TMR_1
TCORB_0									TMR_0
TCORB_1									TMR_1
TCNT_0									TMR_0
TCNT_1									TMR_1
TCCR_0	—	—	—	—	TMRIS	—	ICKS1	ICKS0	TMR_0
TCCR_1	—	—	—	—	TMRIS	—	ICKS1	ICKS0	TMR_1
TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU
TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	
TCR_0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_0
TMDR_0	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
TIORH_0	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIORL_0	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TIER_0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TSR_0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	

Port Name	MCU Operating Mode	Reset	Hardware Standby Mode	Deep Software Standby Mode IOKEEP = 1/0		Software Standby Mode		Bus Released State
				OPE = 1	OPE = 0	OPE = 1	OPE = 0	
PB6/ $\overline{\text{CS6}}$-D/ (RD/$\overline{\text{WR}}$-B)/ $\overline{\text{ADTRG0}}$-B	All	Hi-Z	Hi-Z	[$\overline{\text{CS}}$ output]	[$\overline{\text{CS}}$ output]	[$\overline{\text{CS}}$ output]	[$\overline{\text{CS}}$ output]	[$\overline{\text{CS}}$ output]
				H	Hi-Z	H	Hi-Z	Hi-Z
				[RD/ $\overline{\text{WR}}$-B output]	[RD/ $\overline{\text{WR}}$-B output]	[RD/ $\overline{\text{WR}}$-B output]	[RD/ $\overline{\text{WR}}$-B output]	[Other than above]
				Keep	Hi-Z	Keep	Hi-Z	Keep
				[Other than above]	[Other than above]	[Other than above]	[Other than above]	
				Keep	Keep	Keep	Keep	
PB7/SDϕ	SDRAM mode	SDϕ output	Hi-Z	[SDϕ output]	[SDϕ output]	[SDϕ output]	[SDϕ output]	[SDϕ output]
				H	H	H	H	SDϕ output
	Other than SDRAM mode	H	Hi-Z	[Other than above]	[Other than above]	[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep	Keep	Keep
PC2 to PC3	All	Hi-Z	Hi-Z	Keep		Keep		